IOSR Journal of Computer Engineering (IOSR-JCE)
e-ISSN: 2278-0661, p-ISSN: 2278-8727
PP 20-28
www.iosrjournals.org

Hardware Implementation Of Ecg Qrs Complex Detection Using Fpga

Mahalakshmi M[1], Mrs.Vaijayanthi N[2]
Department of ECE, Indra Ganesan College of Engineering, Trichy

Abstract: *Medical imaging equipment is taking on an increasingly critical role in healthcare as the industry strives to lower patient costs and achieve earlier disease prediction. Due to complexity of their mathematical calculation, many QRS detectors are implemented in software and cannot operate in real time. This project presents a real-time hardware based solution for this task. Several techniques have been proposed in literature survey to achieve high speed implementation and detection of QRS complex. The mathematical morphological technology extracts the effective information with low SNR by removal of baseline wandering and background noise from original ECG image. The multi pixel modulus accumulation employs to act as a low-pass filter to determine the maximum value of QRS. Finally threshold decided the accurate range of QRS. The proposed new hardware architecture is designed in an alter a embedded system image processing framework with NIOS II RISC processor. The ECG image waveform stored in flash memory and algorithms, manipulations are done in NIOS II processor. The proposed hardware architecture utilizes the area and it dissipates power at least few milliwatts. It achieves excellent sensitivity, detection rate.*

Keywords**:** *Electrocardiogram (ECG), Field programmable gate array (FPGA), Mathematical morphology, QRS detection, Very large scale integration (VLSI) architecture.*

I. INTRODUCTION

Medical imaging equipment is taking on an increasingly critical role in healthcare as the industry strives to lower patient costs and achieve earlier disease prediction. Electrocardiogram (ECG) is a diagnosis tool that reported the electrical activity of heart recorded by skin electrode.

In ECG processing, all the extensive analysis need the information of QRS positions as a basic [1]. Within the last decade many new approaches to QRS detection have been proposed; for example, algorithms from the field of non-natural neural, genetic algorithms, wavelet transforms as well as heuristic methods mostly based on nonlinear transforms.

Among the noises plaguing the ECG is the power-line interference: 50/60 Hz pickup and harmonics from the power cord; electrode contact noise: baseline drift due to variable contact between the electrode and the skin; motion artifacts: shifts in the baseline caused by changes in the electrode-skin impedance; muscle contraction: electromyogram - type signals (EMG); respiration causing drift in the baseline;Electromagnetic interference and noise coupled from other electronic equipment. For meaningful and exact detection, steps have to be taken to filter out or discard all these noise sources. Hence, a reliable QRS detection method with low hardware cost, high sensitivity is of urgent need.

Much effort have been given to the frequency-based ECG filtering algorithms for QRS detection [2], i.e., a band-pass filter with a center frequency in the range of 10–17 Hz. After passing the filter, the signal can be squared or averaged over a number of samples to obtain the place of QRS waves. But these techniques affect from the fact that frequency bands of the noise/other components such as P/T waves overlap with that of QRS complex. In addition, in order to exactly detect the QRS.Here, we utilize two most fundamental morphological operators (erosion and dilation) [4], [5] in mathematical morphology technology to reduce the computational complexity for wearable ECG QRS detector. An area efficient very-large-scale integration (VLSI) architecture is designed and implemented on field-programmable gate array (FPGA) to verify the method.

Field Programmable Gate Array (FPGA) is a kind of reprogrammable integrated circuit, other than processor unit, for data [3]. The difficulty of using FPGA is significant, because of many reasons. First, FPGA is a kind of hardware circuit. Thus the aspects of algorithm, parallel processing method and hardware architecture of the system are all needed to be considered in design. However, FPGA has many advantages including low price, inherent parallelism, flexible for design and testing.

This remainder of paper is organized as follows. In this Section II, a brief introduction of mathematical morphology filtering, which serves as a basis for the proposed algorithm. Section III presents the novel algorithm and discusses the details of the algorithm. Section IV describes about the VLSI architecture design

and implementation. The experimental result describes in Section V. A brief set of conclusions and future work is provided in Section VI.

II. THEORY OF MATHEMATICAL MORPHOLOGY

Mathematical morphology is a set-theoretic method of image analysis providing a quantitative description of geometrical structures. A morphological operation is actually the interaction of a set or function representing the object or shape of interest with another set or function of simpler shape called structure element. The shape of the structure element determines the shape information of the signal that is extracted under such an operation. Such operators serve two uses, i.e., extracting the useful signal and eliminating the artifacts. There are two basic morphological set transformation operators: dilation and erosion. The operators for 1-D signal f(n) and structure element g(n) are listed below,

$$\text{Dilation: } f \oplus g(n) = \max_i [(f(n-i) + g(i))] \quad (1)$$

$$\text{Erosion: } f \ominus g(n) = \min_i [(f(n+i) - g(i))] \quad (2)$$

Where i- represents the i th element in a length L structure element, and g(n) is a predefined structure element.

Opening and closing are two extended morphological operators based on dilation and erosion. In mathematical morphology, an opening is the dilation of the erosion of a set by a structuring element; the closing of a set by a structuring element is the erosion of the dilation of that set. Opening and closing operations can also work as morphology filters with clipping effects.

$$\text{Opening: } f \circ g(n) = (f \ominus g) \oplus g(n) \quad (3)$$

$$\text{Closing: } f * g(n) = (f \oplus g) \ominus g(n) \quad (4)$$

III. PROPOSED QRS DETECTION ALGORITHM

The diagram of the proposed algorithm is shown in Fig. 1. The input ECG grayscale image is 160*120 which is loaded into 4 MB FLASH memory. The loaded image is read and processed by NIOS II processor which is designed in FPGA. Then the morphology operators play the most critical role in the proposed algorithm which removes the noise and baseline drift in ECG image. After that, the dilated and eroded outputs are displayed in a VGA monitor by using VGA controller. Then the multipixel modulus accumulation is used to determine the maximum of QRS complex. Finally, the threshold is applied to decide the heart rate. The detailed discussions on each section in subsections.Fig.1 are presented in the following.

1. Memory

An input ECG grayscale image (.png) is loaded into 4MB FLASH memory of the FPGA. The loaded image is processed by NIOS II processor which is designed in FPGA.

2. Morphological Filter

Dilation expands an image object and Erosion shrinks it. The result of dilated and eroded output is stored into a multiplexer, based on the selection of switch the dilated and eroded output will be displayed on a VGA monitor. Here, in order to detect QRS complex accurately and speedily, a peak extractor is defined only based on basic dilation and erosion morphological operators. It can be written as,

$$h(n) = 1/2 \ [D_{i,j} + E_{i,j}] \quad (5)$$

$$v(n) = I - h(n) \quad (6)$$

where h(n) is a averaged output and v(n) is the output of morphology operation.

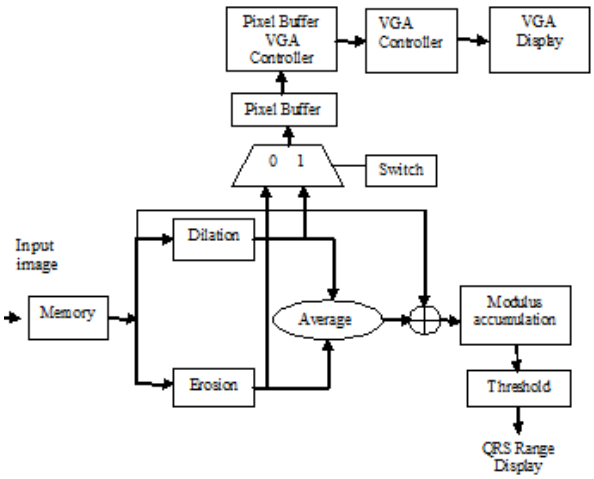


Fig 1. Proposed block diagram

3. Modulus Accumulation

An image enhancement is used to improve the visibility of ECG image. The modulus accumulation determined the maximum range of QRS. The absolute value of the above output v(n) is then combined by multiple-frame accumulation. It is expressed as follows,

$$s(n) = \sum_{i=n-[\frac{q}{2}]}^{n+[\frac{q}{2}]} |v(i)| \qquad (7)$$

Where i indicates the i^{th} element in v(n).The value of q should correspond to the possible maximum duration of normal QRS complex.

4. Threshold and Decision

An adaptive threshold is used as the decision function in connection with the proposed transformation for QRS detection. By experiment, it is found that the required threshold is a function of the maximum of the transformed ECG waveform s(n). The selection of threshold (T) is given by

$$T = \begin{cases} 0.1Max, & Max < 3 \\ 0.3Max, & 3 \le Max \le 7 \\ 0.13Max, & Max > 7 \end{cases} \qquad (8)$$

Where Max is determined from the current QRS segment.

5. VGA Monitor Controller

The VGA monitor is connected to the FPGA board through a VGA port. It allows the user to display an image via the VGA output port. Video Graphics Array monitor screen contains 640 columns by 480 rows of pixels. But the ECG input image contains 160 columns by 120 rows of pixels. Therefore the pixel buffer VGA translated the image size 160*120 into 2*2 pixels of 160*120. VGA monitor uses a clock that can be operated at the VGA specified frequency of 25 MHz. The 25 MHz clock can be generated from a VGA controller with the 50 MHz clock on the DE1 board as an input clock. Finally the processed dilated and eroded images are displayed on a VGA monitor by the selection of switch. If the switch is ON (Dilation-1), dilated output is displayed on a VGA monitor. In the same way if the switch is OFF (Erosion - 0), eroded output is displayed on a VGA monitor.

IV. VLSI HARDWARE ARCHITECTURE AND IMPLEMENTATION

The main function of the PDEU (programmable dilation erosion unit) is to execute dilation and erosion operations, as shown in figure 2. It does so by computing the maximum or minimum value that is the

convolution of image I by a structuring element of size 4x8. The PDEU must extract each element from the SE and then use those elements to determine the maximum or minimum value. The architecture of the PDEU contains two data registers of FIFO unit (First In First Out) and one SR unit (shift register) for retrieving the data from the structuring elements. In addition, there is a CN unit (compared network) that selects the maximum value or minimum value from the shift registers. The two outputs from the CN and the shift register are ODE and OBuf, respectively.

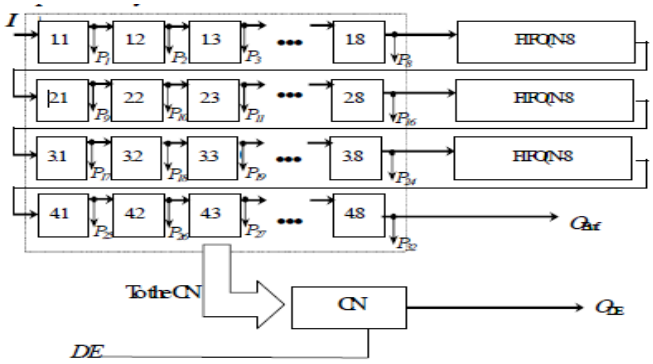


Fig 2. The FIFO array for PDEU, where the numbered rectangles represent shift registers (SR)

For gray-level images, the intensity of every pixel I x,y is passed from the input ***I***, through a chain of shift registers where the intensity of every element is extracted and passed to the CN via the P wire. Before sending the raw image pixel to the CN, its value must first be sent to the SSE for preprocessing, as shown in figure 3, where every data line to the CN from the PDEU in figure 2 has its corresponding SSE. If the control signal S is set to 1, MUX will select *P*i to be *P*OUT. This occurs when the user requires its structuring element to perform dilation or erosion. On the other hand, if the control signal *S* is set to 0, the user chooses not to utilize the structuring element. Meanwhile, the control signal D/E from the PDEU chooses D for the dilation 2 result of the dilation will become 0 after passing through the inverter.

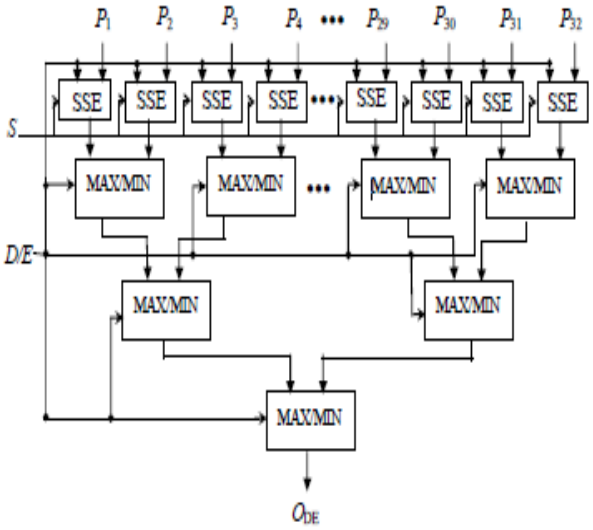


Fig 3. The architecture of CN.

The CN is composed of MAX/MIN units that are used to compute the magnitude value based on the tree-based architecture, as shown in figure 4. If the control signal D/E is set to 1, CN will be the maximum value of the 32 raw image pixels. However, if the control signal of D/E is 0, CN will output the minimum value.

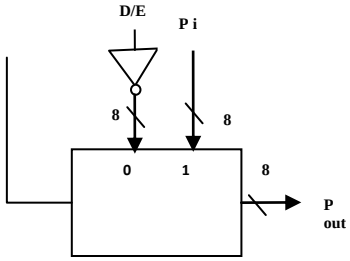


Fig 4. The circuit for SSE.

The MAX/MIN component of figure 4 is composed of one multiplexer and one comparator, as shown in figure 5. If input D/E is set to 1, the dilation operation will be performed and the result of comparator becomes A>B, whereby the multiplexer will output A. In the same way, if input D/E is set to 0, the erosion operation will be performed, and the result of comparator becomes B>A, whereby the multiplexer will output B.

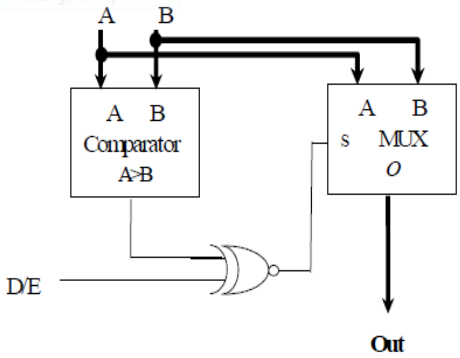


Fig 5. The circuit of Max/Min.

V. Results and Analysis

1. Simulation Result of Proposed System

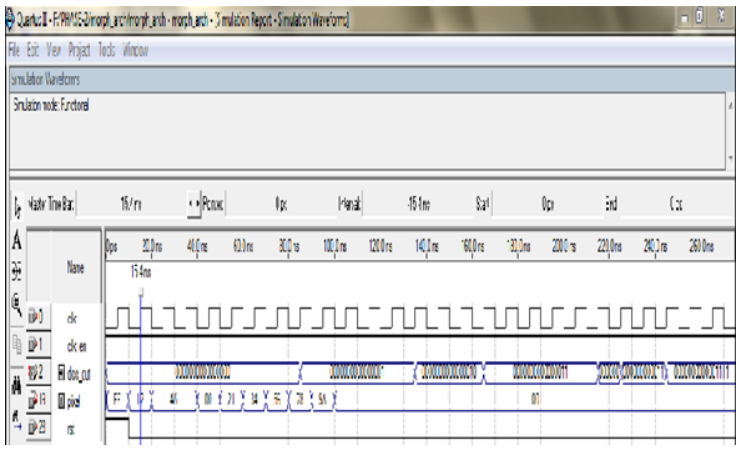


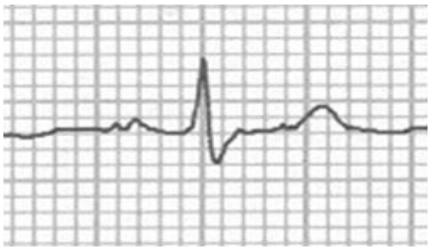
Fig 6. Simulated Waveform of Proposed Architecture

2. Hardware Implementation Results

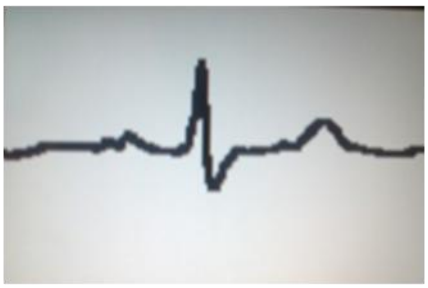
The hardware implementation has been carried out for the ECG QRS waveform images. The detection of a proposed algorithm consists of morphology operation (dilation and erosion), modulus accumulation and threshold. Dilation is used to expand an ECG image waveform and Erosion shrinks the ECG image waveform.

The modulus accumulation determined the maximum value of QRS. Finally threshold is applied to that maximum value of QRS, to decide the QRS range. The overall hardware implementation of this algorithm is verified using the Altera FPGA DE 1 board. The proposed QRS detection algorithm results are shown in figure 7 and 8 .

i. Input ECG image waveform



ii. Dilated output ECG image waveform



iii. Eroded output ECG image waveform

vi. Maximum Peak value after thresholding : 42

Figure 8 QRS Detection of ECG test image 2

Image size taken: 160x120
Image format: PNG

3. PERFORMANCE ANALYSIS

To fully evaluate the performance of detection algorithm, several values are introduced including false negative (FN) which means failing to detect a true beat, and false positive (FP) which represents a false beat detection and true positive (TP) is the total number of QRS correctly detected by the algorithm. By using FN and FP, the sensitivity (Se), positive prediction (+P) and detection error rate (DER) can be calculated using the following equations.

Sensitivity (Se): The percentage of heartbeats correctly identified by the algorithm.

$$\text{Se}\ (\%) = \frac{\text{TP}}{\text{TP} + \text{FN}} \qquad (4.1)$$

Positive Prediction (+P): The detection rate given by the algorithm corresponding to marks made by the specialist.

$$+\text{P}(\%) = \frac{\text{TP}}{\text{TP} + \text{FP}} \qquad (4.2)$$

Detection Error Rate (DER): The percentage of false detections over the total number of detected heartbeats.

$$\text{DER}\ (\%) = \frac{\text{FP} + \text{FN}}{\text{TP}} \qquad (4.3)$$

S.NO	PARAMETERS	TP	FP	FN	%
1.	Sensitivity (Se)	3	0	0	100 %
2.	Positive Prediction (+P)	3	0	0	100 %
3.	Detection Error Rate (DER)	3	0	0	0 %

Table 1 Performance Analysis

1. POWER DISSIPATION AND AREA

The performance parameters such as power and area estimation are reported by using Quartus II software.

Power Dissipation

The ultra low power consumption is essential for ECG applications. In this proposed architecture, the power consumption is much lower than the other FPGA implementations, which dissipated 80.73 mill watts. The ultra low power feature of the proposed QRS detection algorithm helps to expand the battery life of wearable ECG devices.

PARAMETERS	PROPOSED SYSTEM
Dynamic Thermal power dissipation	**8.36 mw**
Static Power dissipation	**47.37 mw**
I/O power Dissipation	**25 mw**
Total power dissipation	**80.73 mw**

Table 2: Various Power Dissipation

Area

The dilation and erosion operations are sharing the same hardware architecture. Therefore, the number of logic elements and registers are reduced.

PARAMETER	PROPOSED METHOD	PERCENTAGE
Total logic elements	39 / 18,752	<1 %
No of Registers	15	<1 %
Total pins	27/315	9 %
Total memory bits	384/239.616	<1 %

Table 3 Area Estimation

2. Comparison with Existing Method

Table 4 compares the existing system with the proposed system. It can be seen, from the comparisons with the other existing methods in [2], [3].Here we used only 3 test ECG images for analysis. So it provides 100% sensitivity, positive prediction and 0% detection error rate. If we take more ECG test images, the results will be decreased in to 0.1%.

S.NO	PARAMETERS	EXISTING SYSTEM	PROPOSED SYSTEM
1.	Sensitivity (%)	99.76%	99.96%
2.	Positive Prediction (%)	99.82%	99.96%
3.	Detection Error Rate (%)	1.63%	0.066%
4.	Area (LUT)	259	24
5.	Power Dissipation (mw)	266.84mw	80.73mw

Table 4 Comparison with Existing Method

VI. CONCLUSION

This project has presented a Hardware implementation of ECG QRS detection based on mathematical morphology and modulus accumulation. A new power and size efficient hardware architecture designed for morphological operation, which has been successfully implemented on DE 1 FPGA board by using SOPC (System on programmable Chip) builder. The proposed method correctly detected the QRS of ECG, even under the presence of severe noise, baseline drift and large P/T waves. And also it achieves 100% accuracy.

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