

## Review on Design and Performance Analysis of Low Power Transceiver Circuit in Wireless Sensor Network

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**Abstract:** WSN is wireless sensor network which consist of numbers of nodes. Transceiver has main role in WSN node. Transceiver consists of both transmitter as well as receiver. Power amplifier, low noise amplifier, mixer, voltage control oscillator are the main block of Transceiver. Power amplifiers are a key part of RF transmitters. 2.4 GHz RF CMOS power amplifier implemented with SMIC 0.13 $\mu$ m is proposed. After power amplifier low power 2.4 GHz RF CMOS mixer with SMIC 0.13 $\mu$ m is proposed. The main aim is to improve the gain, increase the linearity and figure of merit.

**Keywords:** power amplifier; mixer; RF CMOS; WSN; operating frequency; Transceiver.

### I. Introduction

WSN is wireless sensor network, which is specially distributed sensor to monitor physical or environmental condition such as temperature, sound, pressure and passes the data through the network. Wireless sensor network become more attractive because of decreasing size and cost. WSN consist of number of nodes from few to several hundreds or thousands where each node is connected to one or more nodes. Each node size is different. It combines various kinds of technologies including sensors, low power, communication and MEMS. Because of increasing technology today demand for low-power, small size and low-cost products. So the long battery life time and small size with high data rate are the main requirements of these networks. The modern wireless sensor networks are bidirectional and also enabling control of sensor activity. WSN widely used in industrial and consumer applications.

#### Transceiver circuit

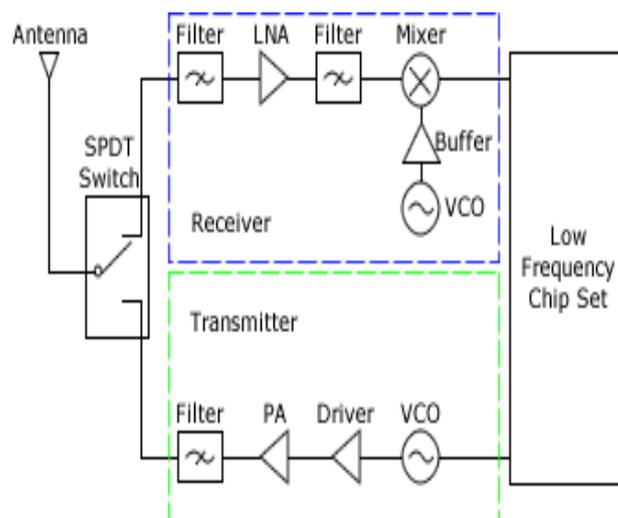


Fig 1. Block diagram of Transceiver.

Transceiver consists of various elements such as low noise amplifier, mixer, power amplifier, filter, voltage control oscillator as shown in fig 1. Transceiver has important role in WSN node.

#### A) About Power Amplifier

Radio Frequency Integrated Circuits (RFIC) are integrated circuits operated in radio frequency range. RF Power Amplifiers are part of the transmitter front-end, and are used to amplify the input signal to be transmitted. The main important parameter for power amplifier is level of output power which depends on the targeted applications, linearity and efficiency. There are two main definitions for efficiency of power amplifier. Power added efficiency (PAE) which is the ratio between difference of RF output power and the RF input power

to the dc power dissipated. Second is the drain efficiency (DE) which is the ratio between RF output power to the dc power dissipated. Power added efficiency is responsible for power gain of amplifier. As power gain decrease more stages will required. Power efficiency is one of the important issue for power amplifier. Drain efficiency and power added efficiency is given as

$$DE = \frac{P_{out}(RF)}{P_{dc}}$$
$$PAE = \frac{P_{out}(RF) - P_{in}(RF)}{P_{dc}}$$

Radio frequency integrated circuit are fabricated using CMOS, GaAs, Hetero-Junction Bipolar Transistor (HBT), High Electron Mobility Transistor (HEMT), Bi CMOS technology. The GaAs technology work at high frequency and high output power, but it is quite expensive because of process variation and device structure is not uniform. Power dissipation is also more in GaAs technology.

CMOS power amplifier also work at high frequency and using some technique output power can be increased. CMOS power amplifier shows more linearity as compared with GaAs and GaN technology. CMOS power amplifier works on little power supply and decrease in overall power dissipation and hence better PAE can be expected. CMOS power amplifiers required less area for Fabrication and also cost effective. There are some issues related to the designing of power amplifier. It includes-

#### A) Low breakdown voltage of deep submicron technologies

Due to break down voltage the device will operated at lower voltage which leads to lower output power. Multiple stages will required for increase in output power.

#### B) Reduce performance

Power amplifiers deliver large output power for obtaining the required power at the output. The current which is high enough that electro migration and parasitic in the circuit reduce the circuit performance.

## II. Literature Review

The first reported CMOS power amplifier operated in the 900MHz ISM band delivering output power from 20 $\mu$ W to 20 mW using a 3V supply, and was implemented in 1 $\mu$ m technology. The measured drain efficiency of the power amplifier with the de-feed inductors of the output stage implemented on chip is 25%, compared to 40% with the inductors off-chip [1]. There has been many researches on power amplifiers based on Gallium Arsenide, BiCMOS and Gallium Nitride technology. In a paper published by Ravinder Kumar, Munish Kumar, Balraj titled "Design and Implementation of a High Efficiency CMOS Power Amplifier for Wireless Communication at 2.45 GHz" design and implementation of power amplifier based on GaAs HEMT at 2.45 GHz is presented. The proposed method is to optimize power efficiency while maintaining good input and output matching. The design simulation process is using Advance Design System (ADS) software. Power Added Efficiency achieved by this amplifier is 34% at DC supply of 3.5 V and providing output power 26 dBm with power gain of 23.4 dB. Input return loss and output return loss are 13 dB and 11 dB respectively [4]. Wenyuan Li, Yulong Tan in their publication "2.4GHz Power Amplifier with Adaptive Bias Circuit" present a 2.4 GHz SiGe BiCMOS power amplifier using an adaptive bias circuit. The pseudo differential structure and adaptive bias control technique are used to improve the performance. The output power observed here is 27dBm with power gain of 24 dB and PAE of 27 % at 3.3 V of operating voltage. The PA can be used in IEEE 802.11b/g WLAN, Wi-Fi Systems, ISM Band Systems, etc. This amplifier leads to high power dissipation [5]. G.Monprasert, P. Suebsombut, et al. in their publication "2.45 GHz GaN HEMT Class-AB RF Power Amplifier Design for Wireless Communication Systems" discuss a GaN HEMT 2.45 GHz Class-AB RF power amplifier for wireless communication systems. The power device used is Gallium Nitride High Electron Mobility Transistor (GaN HEMT) with Silicon as a substrate material. This device achieves maximum output power up to 2.9W and PAE of 42.5 % at dc supply of 20 V. The device mentioned in this paper has large change in the value of PAE for a small change in the applied dc voltage. If the supply is changed to 28 V the PAE observed is 20.8 %. Hence this limitation is an important issue in use of this technology [6]. Even with the advantages of the above mentioned technologies researchers never lost interests in CMOS power amplifiers. In the research paper "2.4-GHz 0.18- $\mu$ m CMOS Highly Linear Power Amplifier" by Yongbing Qian, Wenyuan Li, Zhigong Wang, a 2.4 GHz class AB power amplifier in SMIC 0.18  $\mu$ m RF CMOS process is designed. Maximum output power of 26.2 dBm is observed and Power added efficiency at the 1dB compression point is 21.2%. Operating voltage is 3.3 V.

### III. Proposed Methodology

The block diagram of a proposed power amplifier shown in figure 2 consists of an input matching network, output matching network and inter stage matching network for impedance matching purposes. Inter stage matching network is used as it will be a two stage power amplifier.

The main blocks of the power amplifier are driver stage and power stage. Inter stage network is used for impedance matching between these two networks. Biasing techniques may be used along with the supply network for the driver stage and the power stage. For biasing current mirror circuits may be used.

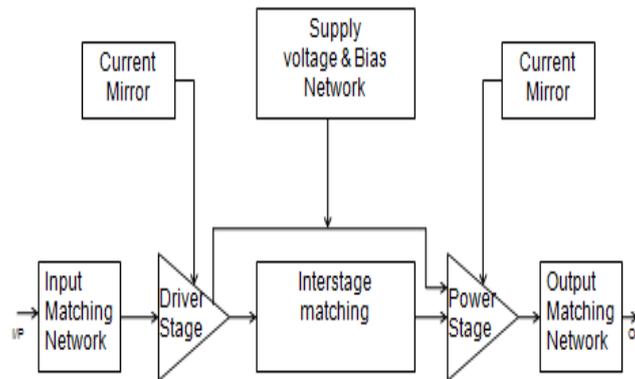


Fig. 2. Block Diagram of proposed CMOS power amplifier.

In literature review it has been observed that power amplifiers designed in GaAs, GaN and BiCMOS technology have its own advantages but CMOS technology edges out on some design parameters such as low power dissipation which leads to high PAE, low chip area and its cost effectiveness. Also CMOS has its own design related issues. A power amplifier is needed to be designed providing considerable amount of output power operating at low voltage supplies. Tradeoff between output power and power added efficiency is required for successful design of a power amplifier in CMOS technology. Implementation of power amplifiers in CMOS Tech-nology is considered a major step towards the realization of a complete transceiver on-chip. A high level of integration, and low cost can be achieved using CMOS technology.

#### B) About mixer

Mixer is a nonlinear device which takes the baseband signal as the input and output is a RF modulated signal. At the transmitter side up conversion takes place and at receiver side down conversion takes place. RF mixer provides one of the one of the key building block in RF design. RF mixing enables signal to be converted to different frequency and thereby allowing signals to be processed more efficiently.

Mixer is a three port device in which it multiplies two signal in time domain. It assume that both incoming signals are sinusoidal and the output of the multiplier can get sum frequency component and difference frequency component, which can be express as-

$$(A \cos w_1 t)(B \cos w_2 t) = \frac{AB}{2} [\cos(w_1 - w_2) t + \cos(w_1 + w_2)]$$

We can get a difference frequency component (frequency  $w_1-w_2$ ) and sum frequency component (frequency  $w_1 +w_2$ ). One input sinusoidal signals having fix rate provided by a local oscillator, and the other is the received RF signal or the transmitted low-frequency signal. The band-pass filter is selected for required frequency.

There are two types of mixer circuit as active and passive mixer. Passive mixer generally used because passive mixer does not requires extra power supply as compared with the active type of mixer. A 2.4 GHz frequency is a well regulated frequency which is used for wide band channel, also used for long communication. In Industrial, scientific, medical radio bands and in many application 2.4 GHz frequency is used. For example Wi-Fi is also operated at 2.4GHz frequency.

Gilbert cell is nothing but cascade circuit used as an analog multiplier. Gilbert cell is an active mixer circuit. It is basically an amplifier followed by phase reversing switch. Passive mixers are generally used because of it having high bandwidth, good inter modulation distortion. RF mixer provides one of the key building block in RF design. Mixer is a non linear device.

#### IV. Literature Review

Literature [1] an ultra-low power (ULP) self oscillating mixer (SOM) using moderate inversion operation is presented in this paper. It made up of voltage controlled oscillator stacked on a single balanced current commuting mixer which is led by an RF transistor stage. At last SOM exhibit a minimum SSB noise figure of 17.5 dB and a voltage conversion gain of 10 dB. It is operating under 1V supply, the chip has a power consumption of 600 uW and an occupying area of 1.2 mm<sup>2</sup> including pads & it is measured in 65 nm technology[10].

Literature [2] A 1.8-V I/Q down mixer operating in 2.4GHz band for the Wireless Sensor Network application using 0.18- $\mu$ m RF CMOS process is presented in this paper. The double-balanced mixer is modified based on the conventional Gilbert cell. The mixer achieves a conversion gain of 13.84 dB with an input 1-dB compression point (IP1dB) of -3.66 dBm. It also achieves a single side band (SSB) noise figure (NF) of 11.55 dB. & it consumes 1.96 mA of current from a 1.8-V power supply. The presented design uses an active mixer with gain co working with the LNA in order to reduce the total power consumption of the front-end. The presented folded Gilbert cell mixer is a solution for low voltage and low power consumption design[11].

Literature [3] in this paper A 60 GHz down-conversion mixer used in the unlicensed 60 GHz band system in 65-nm CMOS technology is presented. Based on the double-balanced Gilbert cell, the mixer comprises a cross-coupled pair to rise conversion gain and two series LCR network resonating at IF frequency to enhance bandwidth. As a result, both high gain and broad bandwidth are achieved. From the simulation results, the conversion gain exceeds 10 dB and 3-dB IF bandwidth is from 8 GHz to 16 GHz. The noise figure is less than 12 dB and the output 1dB compression point is - 6dBm and the chip area is 1 $\times$ 0.75 mm<sup>2</sup> with pads[12].

Literature [4] In this paper A low-voltage RF CMOS receiver front-end for energy harvesting Wireless Sensor Node (WSN) is presented. A MOSFET-only wideband balun, LNA, with noise and distortion cancelling, is designed to work at 0.6 V supply voltage, with a passive mixer. The passive mixer works in current mode, allowing a minimal introduction of noise and a good linearity. This receiver does not include simple inductor architecture, resulting in a reduced area and also reduced circuit cost. The proposed receiver presents a good solution for a Wireless Sensor Actuator Node (WSAN) receiver whose power is supplied by an Energy Harvesting solution, mainly due to its low-power consumption. The total power consumption achieved is 1.95 mW[13].

Literature [5] In this paper A 2.4 GHz RF CMOS Up-Conversion Mixer for Wireless Sensor Networks is presented. Nodes Mixer is one of the main modules of a transmitter system, and its performance will heavily impact the functionality of the entire transmitter. Gilbert cell structure can achieve high degree of RF (Radio Frequency) and LO (Local Oscillator) isolation, thus loosening filtering output requirements. This design employs a resonant LC network as the load to improve gain, increase the output voltage swing, and inhibit the high-order harmonic generation. It uses feedback to improve the linearity of the mixer. The current-reuse bleeding double-balanced mixer operates at 2.4GHz. And the up-conversion mixer uses an intermediate frequency (IF) input frequency of 1.2MHz, a local oscillator (LO) of frequency of 2.4GHz and a RF output frequency of 2.4012 GHz[14].

Literature [6] In this paper an up-conversion mixer for 2.4GHz wireless sensor networks (WSN) in 0.18 $\mu$ m RF CMOS technology is presented. The simulation results indicated that under 1.8V power supply the conversion gain was 16.2dB. Operational amplifiers are used to improve conversion gain in low power consuming, and resistor negative feedback is used to improve linearity. This proposed mixer was post simulated and its results are good enough to apply in the transceiver for WSN system[15].

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