

## Design of Counter Using SRAM

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**Abstract:** In digital logic and computing, a counter is a device which stores the number of times a particular event or process has occurred, often in relationship to a clock signal. CMOS devices are designed for high noise immunity and low static power consumption. CMOS accomplishes current reduction by complementing every nMOSFET with a pMOSFET and connecting both gates and both drains together. A high voltage on the gates will cause the nMOSFET to conduct and the pMOSFET to not conduct, while a low voltage on the gate causes the reverse. This arrangement greatly reduces power consumption and heat generation. Finally we proposed counter using SRAM model, provides the best resolution, high output current and good output-input current linearity.

**Keywords:** CMOS(Complementary Metal Oxide Semiconductor),MOSFET(Metal Oxide Semiconductor Field Effect Transistor), SRAM(Static Random Access Memory), TTL(Transistor Transistor Logic),VLSI(Very Large Scale Integrated Circuits).

### I. Introduction To Counter

Counter used in electronics, computing and mechanical counting devices. In digital logic a counter is a device which stores the number of times a particular event or process has occurred, often in relationship to a clock signal. The most common type is sequential digital logic circuit with an input line called the "clock" and multiple output lines. The values on the output lines represent a number in the binary or BCD number system. Each pulse applied to the clock input increments or decrements the number in the counter. A counter circuit is usually constructed of a number of flip flops connected in cascade. Counters are a very widely-used component in digital circuits, and are manufactured as separate integrated circuits and also incorporated as parts of larger integrated circuits.

#### A. Types of Counter

There are seven types of electronic counters are as follows.

- Asynchronous (ripple) counter – changing state bits are used as clocks to subsequent state flip-flops.
- Synchronous counter – all state bits change under control of a single clock.
- Decade counter – counts through ten states per stage.
- Up/down counter – counts both up and down, under command of a control input.
- Ring counter – formed by a shift register with feedback connection in a ring.
- Johnson counter – a twisted ring counter.
- Cascaded counter.

Each is useful for different applications. Usually, counter circuits are digital in nature, and counting natural binary. Many types of counter circuits are available as digital building blocks, for example a number of chips in the 4000 series implement different counters. Occasionally there are advantages to using a counting sequence other than the natural binary sequence such as the binary coded decimal counter, a linear feedback shift register counter, or a Gray-code counter.

#### B. Asynchronous Counter

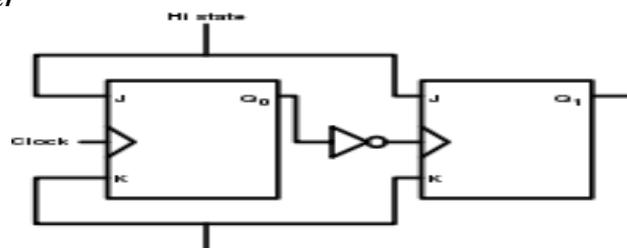


Fig.1 Asynchronous Counter

To add additional flip-flops, always inverting the output to its own input, and using the output from the previous flip-flop as the clock signal. The result is called a ripple counter, which can count to  $2^n - 1$  where  $n$  is the number of bits (flip-flop stages) in the counter. Ripple counters suffer from unstable outputs as the overflows "ripple" from stage to stage, but they do find frequent application as dividers for clock signals, where the instantaneous count is unimportant, but the division ratio overall is (to clarify this, a 1-bit counter is exactly equivalent to a divide by two circuit; the output frequency is exactly half that of the input when fed with a regular train of clock pulses). The use of flip-flop outputs as clocks leads to timing skew between the count data bits, making this ripple technique incompatible with normal synchronous circuit design styles.

## II. Existing System

### A. Conventional Counter

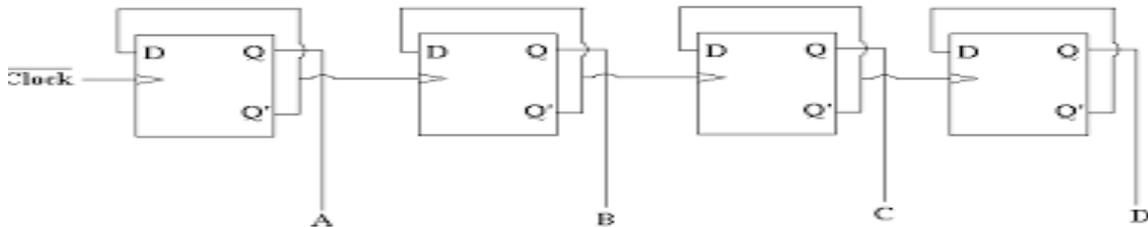


Fig.2 Conventional Counter

Counter built from four positive edge triggered d type flip flops connected in series. Clock pulses are fed into CLK input of FF0 whose output ,Q0 provides  $2^0$  output for flip flop 1 after 1 clock pulse the rising edge of the q bar output of each flip flop triggers the clock input of next flip flop at half the frequency of the clock pulses applied to its input. The Q outputs then represents a four bit binary count with Q0 to Q3 representing  $2^0(1)$  to  $2^3(8)$  respectively.

Assuming that the four Q outputs are initially at 0000 ,the rising edge of the first clock pulse applied will cause the output Q0 to go to logic 1.the next clock pulse will make Q0 output return to logic 0,and at the same time Q0bar go from 0 to As Q0bar (and the clock input o flip flop 1 goes high ) this will now make Q1 high , indicating a value of  $2^1$  on the Q outputs .

The next (third clock pulse will cause Q0 to go to logic 1 again, so both Q0 and Q1 will now be high , making the four bit output 1100.the fourth clock pulse will make both Q0and Q1 return to 0 and as Q1bar will go high at this time, this will toggle flip flop 2,making Q2 high and indicating 0010 at the outputs. Reading the output word from right to left ,the Q outputs therefore continue to represent a binary number equaling the number of input pulses received at the clock input of flip flop 0.as this is a four stage counter the flip flop will continue to toggle in sequence and the four Q outputs will output a sequence of binary values from 0000 to 1111, before the output returns to 0000. CMOS is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states.

Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor–transistor logic (TTL) or NMOS logic, which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips. CMOS circuits use a combination of p-type and n-type metal– oxide–semiconductor field-effect transistor (MOSFETs) to can be implemented with discrete devices for demonstrations, commercial CMOS products are integrated circuits composed of up to billions implement logic gates and other digital circuits. Although CMOS logic of transistors of both types, on a rectangular piece of silicon of between 10 and 400 mm<sup>2</sup> .

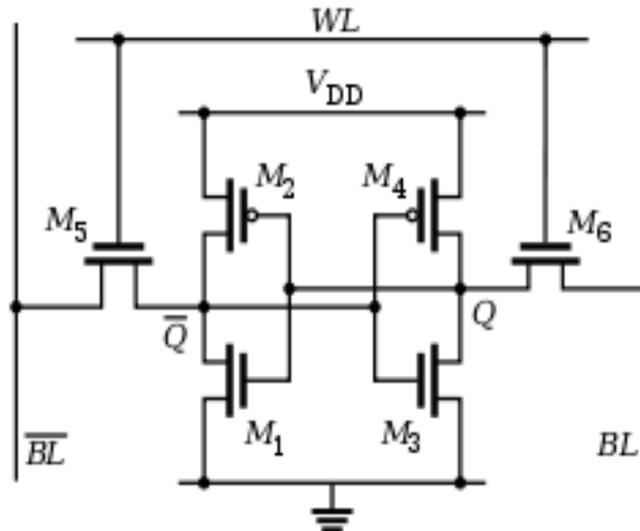
## III. Proposed System

Static CMOS circuits are constructed in such a way that all PMOS transistors must have either an input from the voltage source or from another PMOS transistor. Similarly, all NMOS transistors must have either an input from ground or from another NMOS transistor. The composition of a PMOS transistor creates low resistance between its source and drain contacts when a low gate voltage is applied and high resistance when a high gate voltage is applied. On the other hand, the composition of an NMOS transistor creates high

resistance between source and drain when a low gate voltage is applied and low resistance when a high gate voltage is applied. CMOS accomplishes current reduction by complementing every nMOSFET with a pMOSFET and connecting both gates and both drains together. A high voltage on the gates will cause the nMOSFET to conduct and the pMOSFET to not conduct, while a low voltage on the gates causes the reverse. This arrangement greatly reduces power consumption and heat generation. However, during the switching time, both MOSFETs conduct briefly as the gate voltage goes from one state to another. This induces a brief spike in power consumption and becomes a serious issue at high frequencies.

In short, the outputs of the PMOS and NMOS transistors are complementary such that when the input is low, the output is high, and when the input is high, the output is low. Because of this behavior of input and output, the CMOS circuit's output is the inverse of the input.

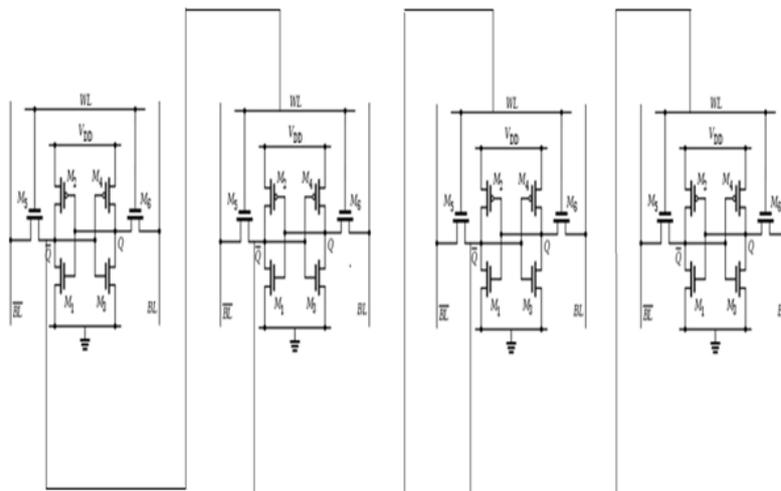
**A. Counter using SRAM**



**Fig.3** Counter using SRAM

- In the above diagram there are totally 4 NMOS and 2 PMOS used. WL act as the reference line, BL and BL bar are the inputs. If BL=0 BL bar=1 whereas BL acts as the Vdd and BL bar act as the ground and vice versa as required. Q and Q bar are the outputs.
- Q is given as the input to M1 and M2, for which the output is obtained at Q bar which should be the complement of Q (Input).
- Similarly, Q bar is given as the input to M3 and M4 for which the output is taken from Q, which should be the complement of Q bar (input).

**B. Four Bit Counter Using SRAM**

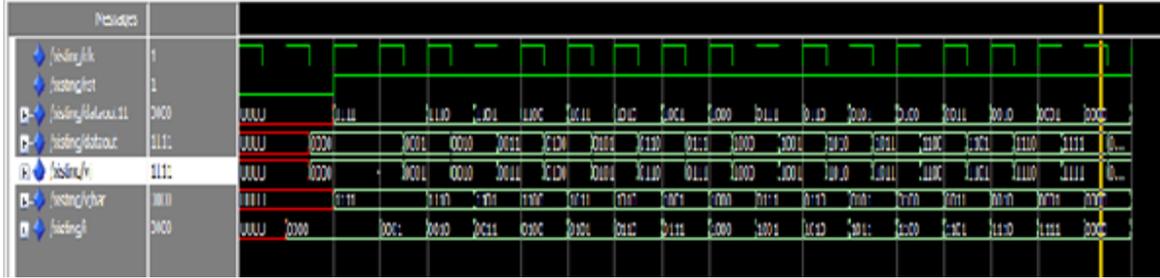


**Fig.4** 4-bit Counter using SRAM

The above diagram is the cascaded four bit counter using SRAM ,Where Q bar of one counter is given as input to the next counter. The principle of the matrix circuit is that if value of the pixel is higher than the value of reference of tension ( $V_r$ ),the exit of the comparator is in a high state (5V). On the other hand, if value of the pixel is less than the value of the tension  $V_r$ , the exit of the comparator is in a low state (0V). After the comparison, the exits of the comparator are entered to the logical gating circuit AND. In the logical gating circuit AND, if signal comparator from line and row are 5V and corresponding LED is active.

### IV. Simulation Results And Discussions

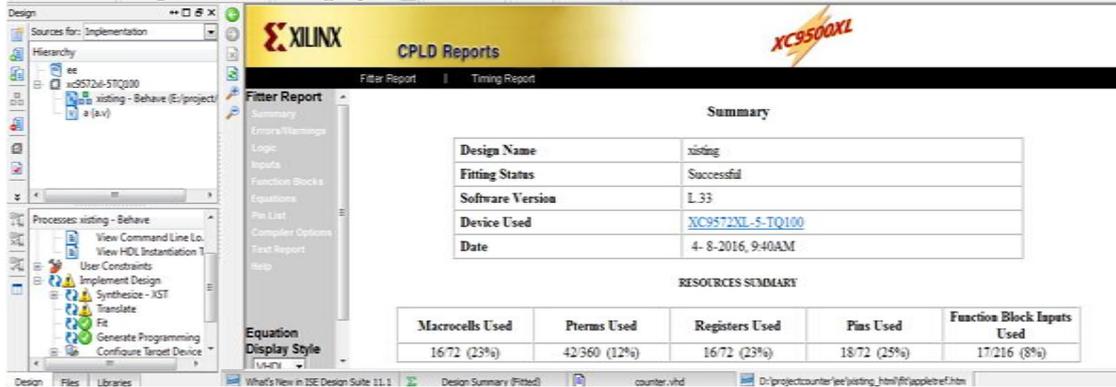
#### 4.1 Counter Using CMOS



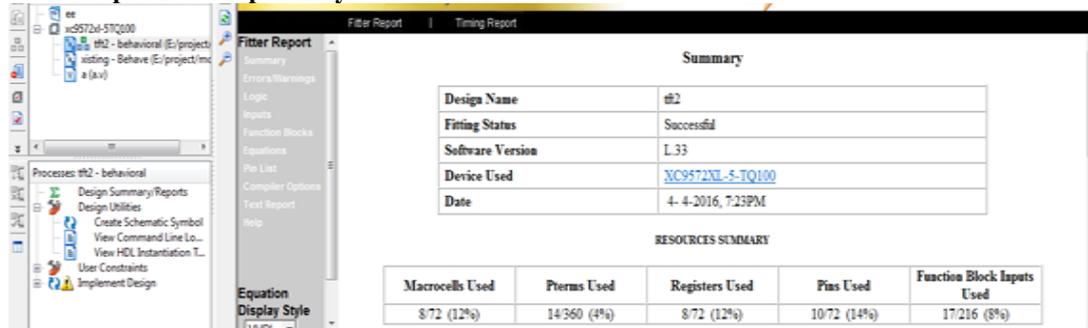
#### 4.2 Counter Using SRAM



#### 4.3. Power Output for Existing System



#### 4.4.Power output for Proposed System



## **V. Conclusion**

In this paper we have designed a counter using a SRAM whereas previously the counter was designed using a D flip flop and CMOS in the existing system. In the proposed system the counter SRAM has a reduced power consumption when compared to that of the existing system ,since the transistors used in this system are connected in series, the power applied for the first transistor is used by all the succeeding transistors in the system .Also the use SRAM has many advantages such as Low hardware complexity, low cost for fabrication, mechanical flexibility, Strong optical absorption and efficient emission.

## **References**

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