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Dual Edge Triggered Flip-Flops Based On C-Element Using Dual Sleep and Dual Slack Techniques

I. Pavani Akhila Sree[1], D.Murali Krishna[2]
[1]*M.Tech(VLSID) Student, Department of ECE, SVECW, Bhimavaram, India*
[2]*Sr. Assistant Professor, Department of ECE, SVECW, Bhimavaram, India*
Corresponding Author: I. Pavani Akhila Sree[1]

Abstract: *In Modern digital electronics the low power circuits plays a vital role. As the Flip-flops are basics storage elements used in many of digital circuits, so they have to be designed with optimized power consumption. This paper presents the design of the Dual edge triggered(DET) Flip-flops based on C-element using Dual Sleep and Dual Slack techniques. As the technology is scaling from micron technology to deep sub-micron technology the leakage power is one of the parameter which is effects the circuit performance by using these dual sleep and slack techniques the leakage power is reduced in the DET Flip-flops. The designs presented in this paper were simulated in CMOS 45nm technology using Cadence tool, observed to have superior characteristics such as power consumption and power-delay-product(PDP) when compared to existing DET Flip-flops.*

Keywords: *Dual-edge-triggered, C-element, Dual sleep, Dual slack, Cadence.*

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I. Introduction

Low power very large scale integrated (VLSI) circuits have a great potential in the digital electronics. One of the primitives mostly used for storage are Flip-flops. Dual-edge triggered(DET) flip-flops came into existence replacing the single edge triggered(SET) flip-flops. As the DET flip-flops achieve the same data rate as of the SET flip-flops at half the clock frequency resulting in low power dissipation in the synchronous logic circuits [1],[2]. Latch-MUX DET flip-flop design is the basic design of the DET flip-flop, which consists of two latches at input where the latches are level-triggered by opposite clocks , Output of these latches are multiplexed to the final output stage through a multiplexer. One of the latches is transparent to the output for every change at the output, In the presence of the glitches at the input the power consumption of the flip-flops will be greatly effected by these glitches. The Conditional toggle (CT_C) C-element flip-flop is one of the alternative DET flip-flop design that can reduce the adverse effect of input glitches at the output. Leakage power is one the primitive to considered during the design of VLSI circuits in deep sub-micron technology, there are many techniques such as Dual sleep and Dual slack techniques forreduction of leakage power.

This paper consists of five sections. Section I is introduction that presents the basic knowledge of DET flip-flops. Section II presents the DET flip-flop designs that uses the C-element. CT_C flip-flop using dual sleep technique and CT_C flip-flop using dual slack technique are included in this section. Section III presents previously existing flip-flops and comparison of existing flip-flops with the proposed flip-flops. Section IV concludes the paper.

II. Ciruit Description

A C-element introduced by Muller C in [3] is three terminal device with two input terminals and one output terminal. The operation of C-element is as follows, when both the inputs are same then the output switches to the input value, the previous value is retained at the output in remaining cases. The transistor level schematic diagram of the weak-feedback C-element and dynamic C-element in [4] are as shown in the figure and the operational waveforms of the C-element are as shown in the figure 1 & 2 respectively. Latch-MUX DET flip-flop presented in [5] is a common dual edge triggered in which both the latches re level triggered by opposite clocks as shown in figure .The power consumption is high in this Latch-MUX design ,So the design is improved to conditional toggle (CT_C) c-element based flip-flop for better results in power consumption. The transistor level schematic of the CT_C flip-flop is as shown in figure 3, It is having only 20 transistors for input output and clock buffering, inputs to CT_C flip-flop are D and CK and the output is Q. The operation of the CT_C flip-flop is clearly depicted in the operational waveforms shown in the figure 4. As the circuits are designed in sub-micron technology the leakage power consumption is high so in order to reduce the leakage power extra circuitry is added to this CT_C flip-flop.

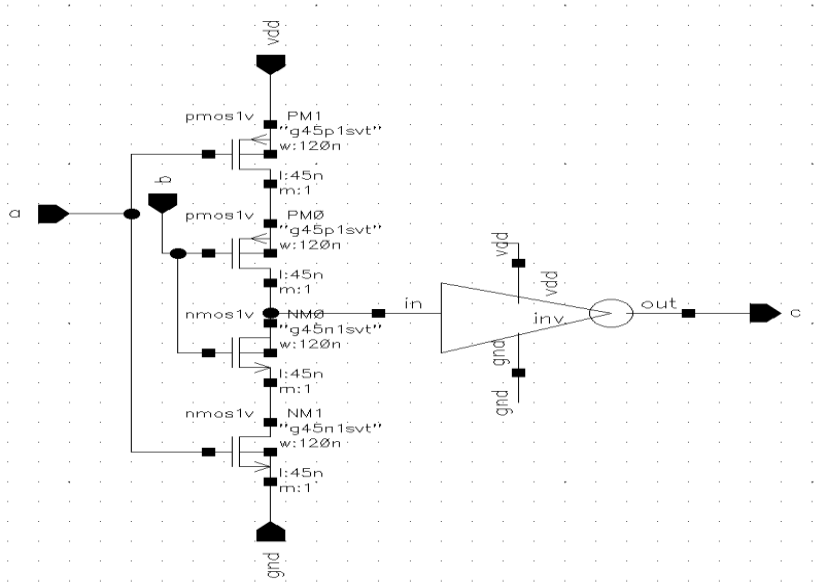

Figure 1: The transistor level schematic of the Dynamic C-element

i. CT_C flip-flop using Dual Sleep technique :

The CT_C flip-flop is improved by adding extra circuity with one NMOS and one PMOS transistor which are connected in parallel at both VDD and GND as shown in figure for creating virtual VDD and virtual GND for by passing the leakage current. The transistor level schematic diagram of the CT_C using dual sleep technique is as shown in the figure 5. The Sleep transistor are driven by opposite clocks CK1 and CK1B.When D becomes equal to CK and CKB the internal nodes A and B switches to CKB and CK respectively. At least one the node A or B should be DB in between the clock transitions.

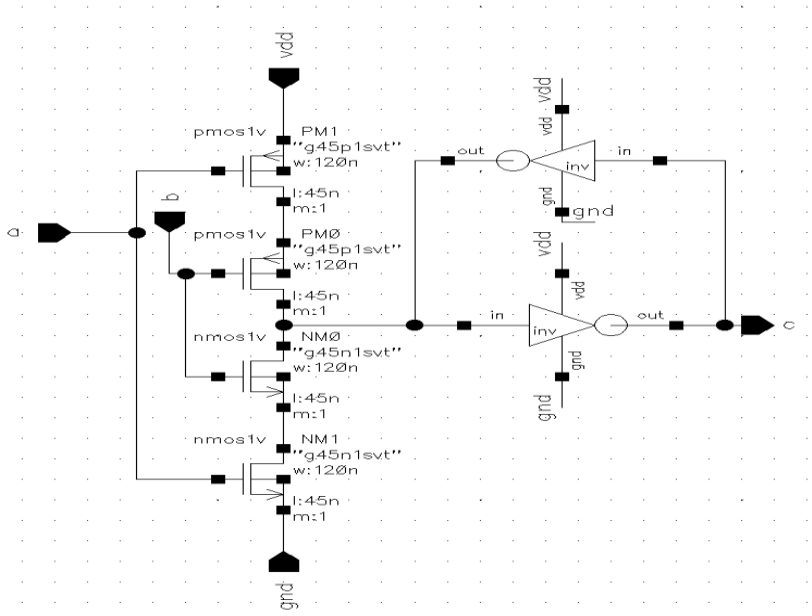

Figure 2:The transistor level schematic of the weak feedback C-element

The D input is only responsible for timing of the inversions of the nodes A and B, whenever the clock changes one of the A or B that is not at DB changes to DB(i.e. both A and B are at DB for while after every clock transition).The output Q switches to D after every clock transition when both A and B are equal to QB. The operational wave forms depicted in figure 6 clearly shows the operation of the CT_C flip-flop using dual sleep technique. Although the number of transistors are increased (4 transistors are addition added) when compared to CT_C flip-flop the power dissipation has reduced considerably.

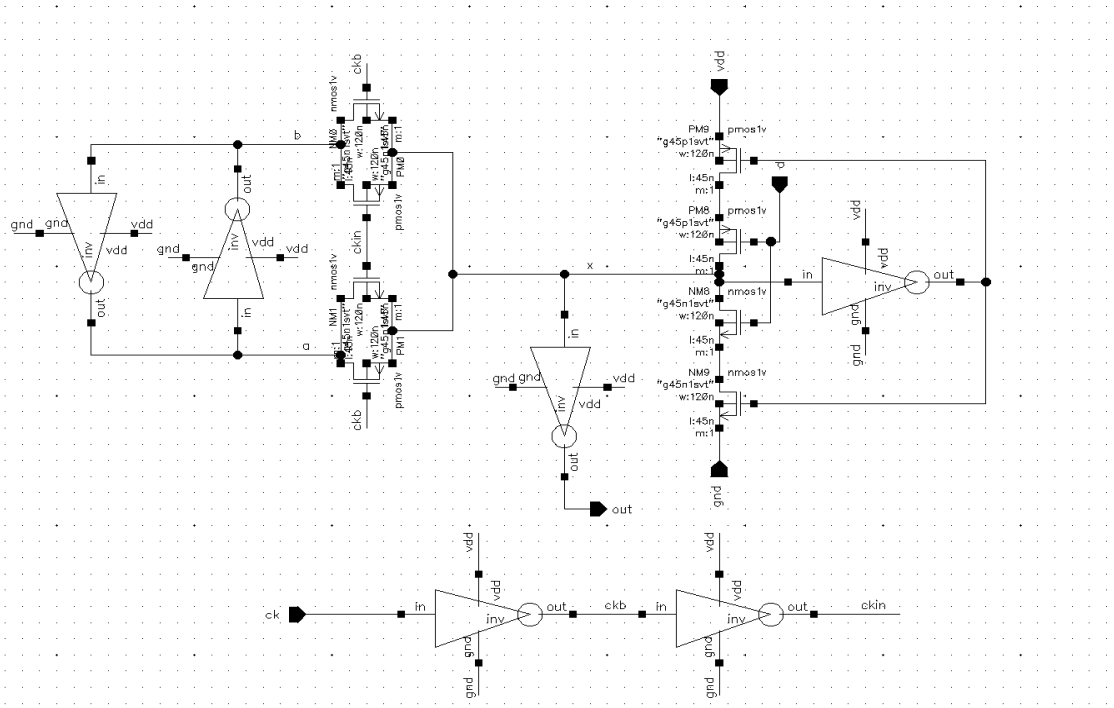

Figure 3: The transistor level schematic of the CT_C flip-flop.

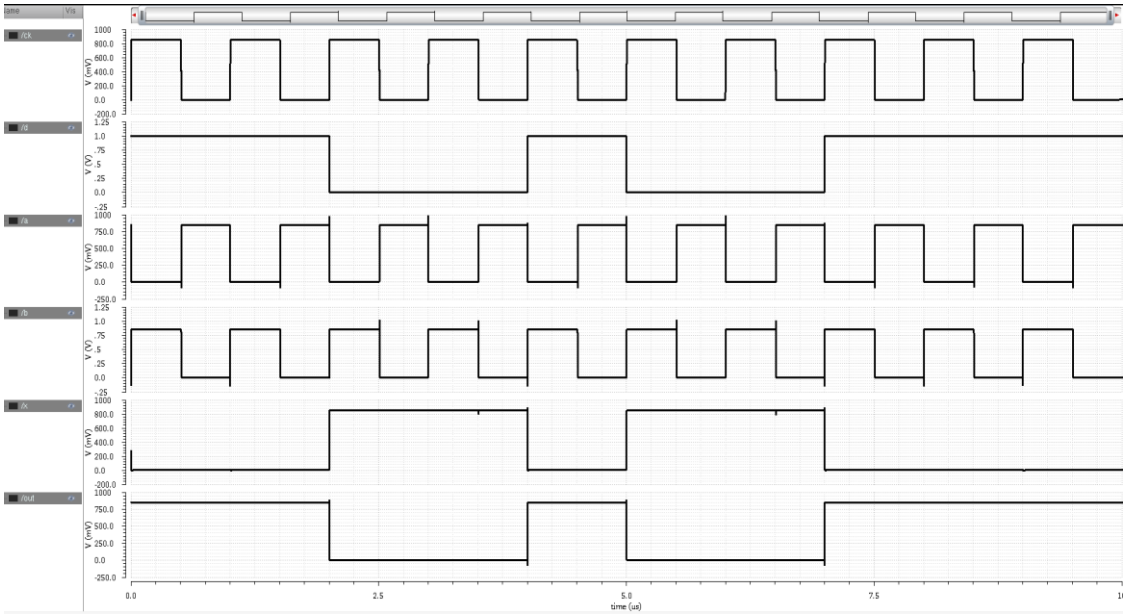

Figure 4: Operational waveforms of the CT_C flip-flop.

ii. CT_C flip-flop using Dual Slack technique :

The transistor level schematic of dual slack technique is as shown in the figure 7, a common circuity is attached to logic circuitry with two slack transistors connected in series with one sleep transistor parallel at the VDD and GND. The circuitry at VDD comprises of one PMOS sleep transistor in parallel with two NMOS slack transistors connected in series.The circuitry at GND comprises of one NMOS sleep transistor in parallel with two PMOS slack transistors connected in series. The operation of CT_C flip-flop using dual slack technique is same as the CT_C flip-flop using dual sleep technique.

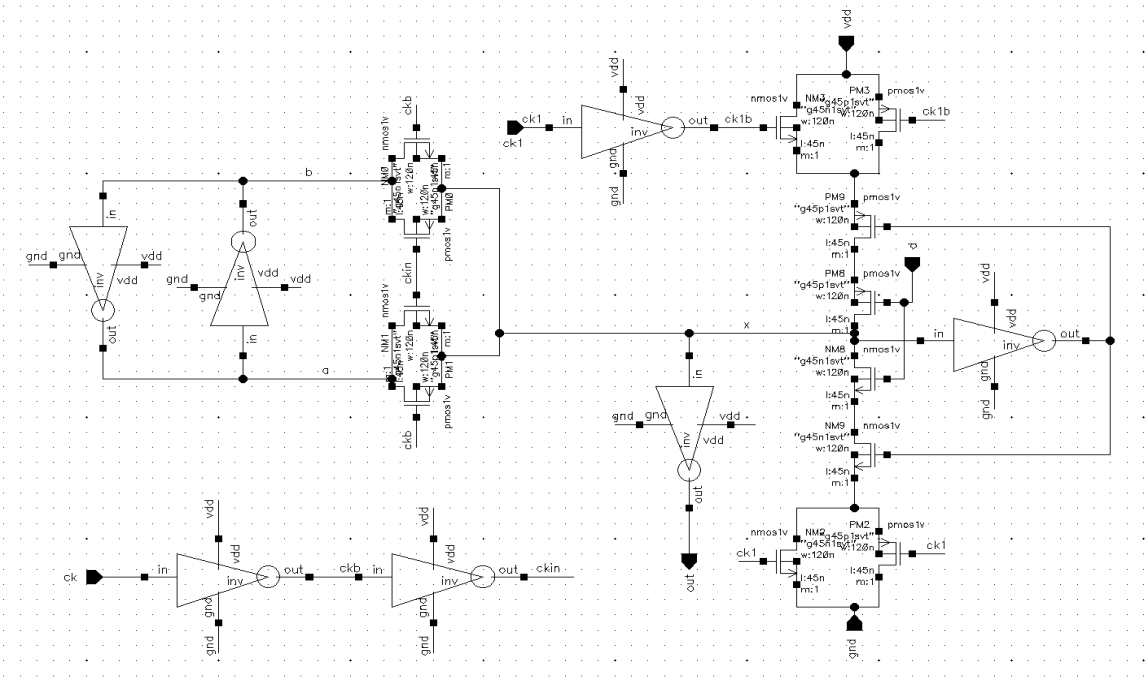

Figure 5: The transistor level schematic of the CT_C flip-flop using dual sleep technique.

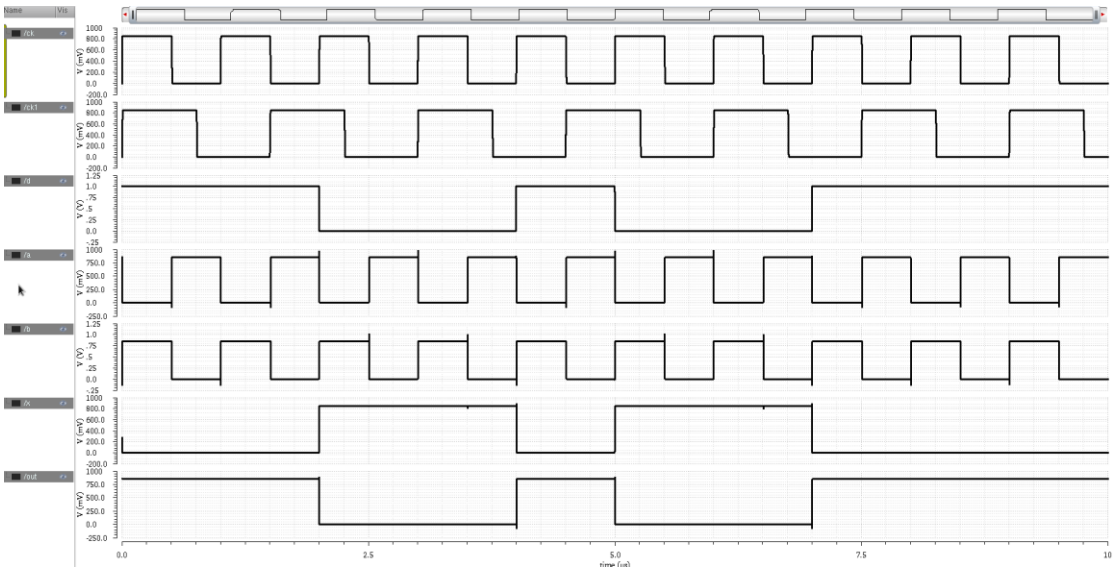

Figure 6: Operational waveforms of the CT_C flip-flop using dual sleep technique.

The two sleep transistors are driven by the opposite clocks CK1 and CK1B respectively. The clock signal CK1 is only responsible for operating the sleep transistors, It does not effect the original operation of the CT_C flip-flop. The input to the two slack transistors at the VDD is high voltage and the input to the slack transistors at GND is low voltage in all the cases. The operational waveforms of CT_C flip-flop using dual slack technique is as shown figure 8. The drain induced barrier lowering which occurs in the deep sub-micron technology reduces by using this dual slack techniques and results in low leakage power and average power dissipation is reduced for CT_C flip-flop using dual slack technique when to the other flip-flops , Is having higher performance.

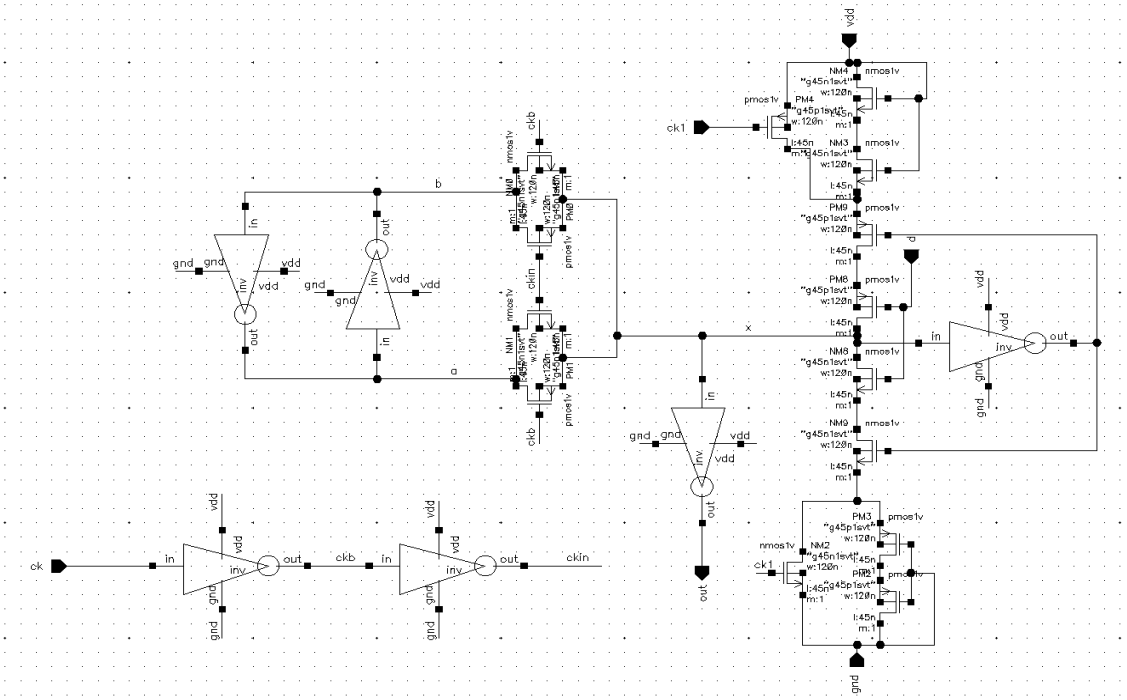

Figure 7:The transistor level schematic of the CT_C flip-flop using dual slack technique.

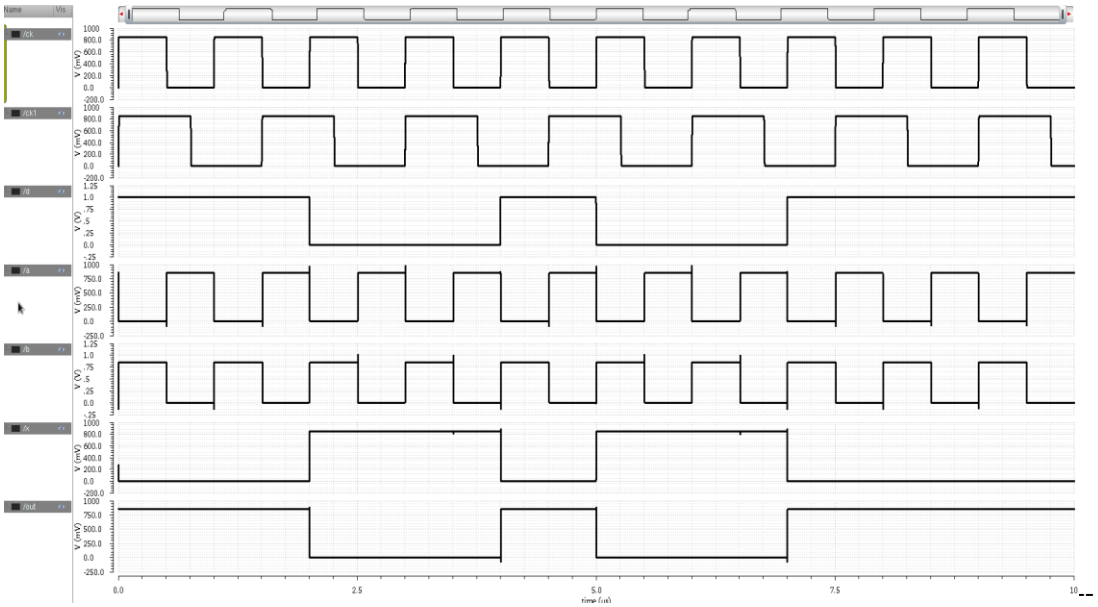

Figure 8: Operational waveforms of the CT_C flip-flop using dual slack technique.

III. Simulation Results

The DET flip-flops which were presented in this paper,Existing DET flip-flop were simulated in 45nm technology. The tool used for simulation, average power dissipation and delay calculation is cadence virtuoso software. The latch-MUX design is basic design of the DET flip-flop. The latch-MUX C-element LM_C flip-flop presented in [6] is an improved design of latch-MUX design (LM), where the MUX in LM flip-flop is replaced by a C-element whereas the operation of this improved design does not change and will retain same as LM flip-flop. The LG_C, IP_C, FN_C, CT_C, CTF_C flip-flops are C-element based designs which were presented in [7] are having superior characteristics such as power dissipation and power delay product. CT_C flip-flop is taken for further improvement and added dual sleep and dual lack techniques presented in [8] for reducing the power dissipation and achieved the superior results than the existing flip-flops. The comparison of power dissipation, number of transistors, delay and power delay product are tabulated in the table 1. The operating frequency at which all the circuits are simulated is 1GHz and supply voltage is 0.85v for all the simulated circuits.

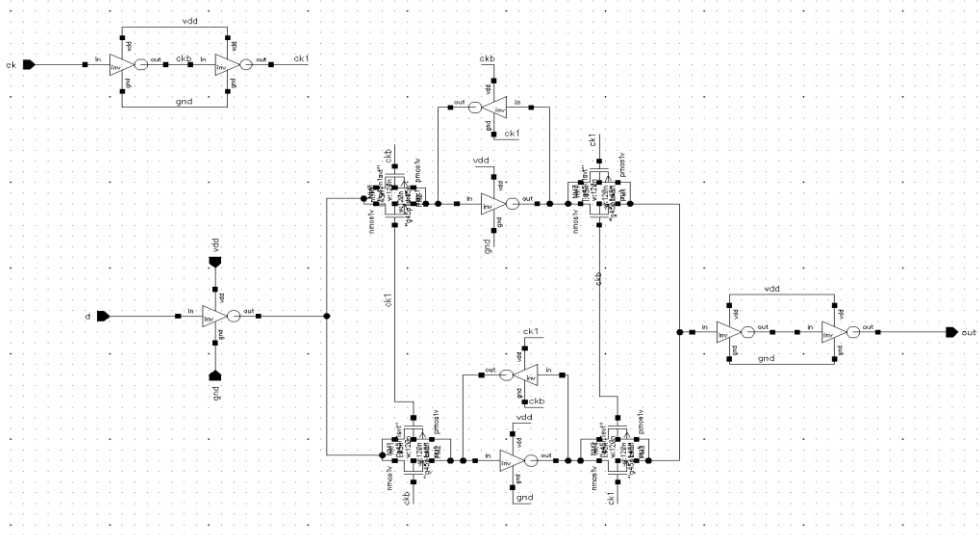

Figure 9:The transistor level schematic of the Latch-MUX flip-flop

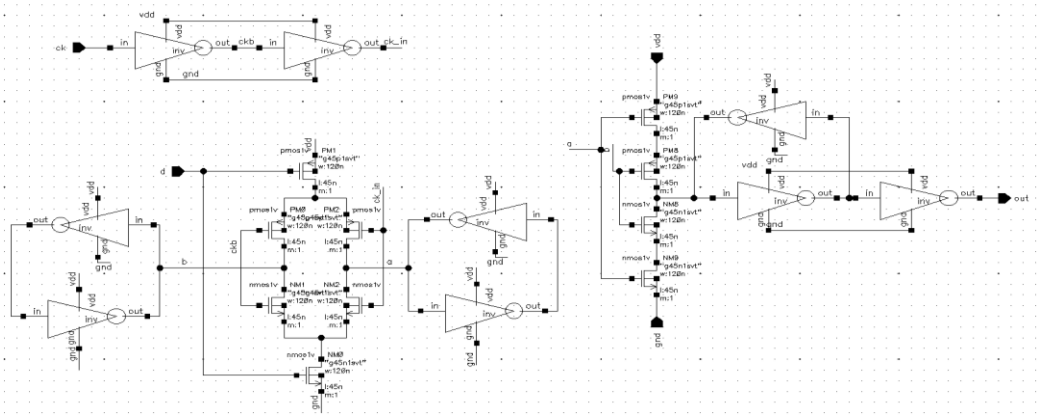

Figure 10:The transistor level schematic of the LG_C flip-flop.

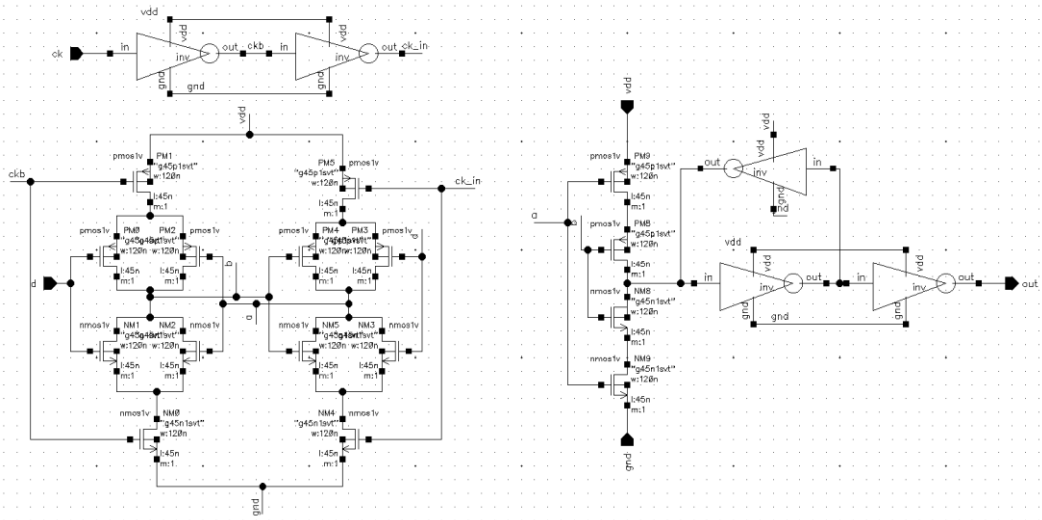

Figure 11:The transistor level schematic of the IP_C flip-flop.

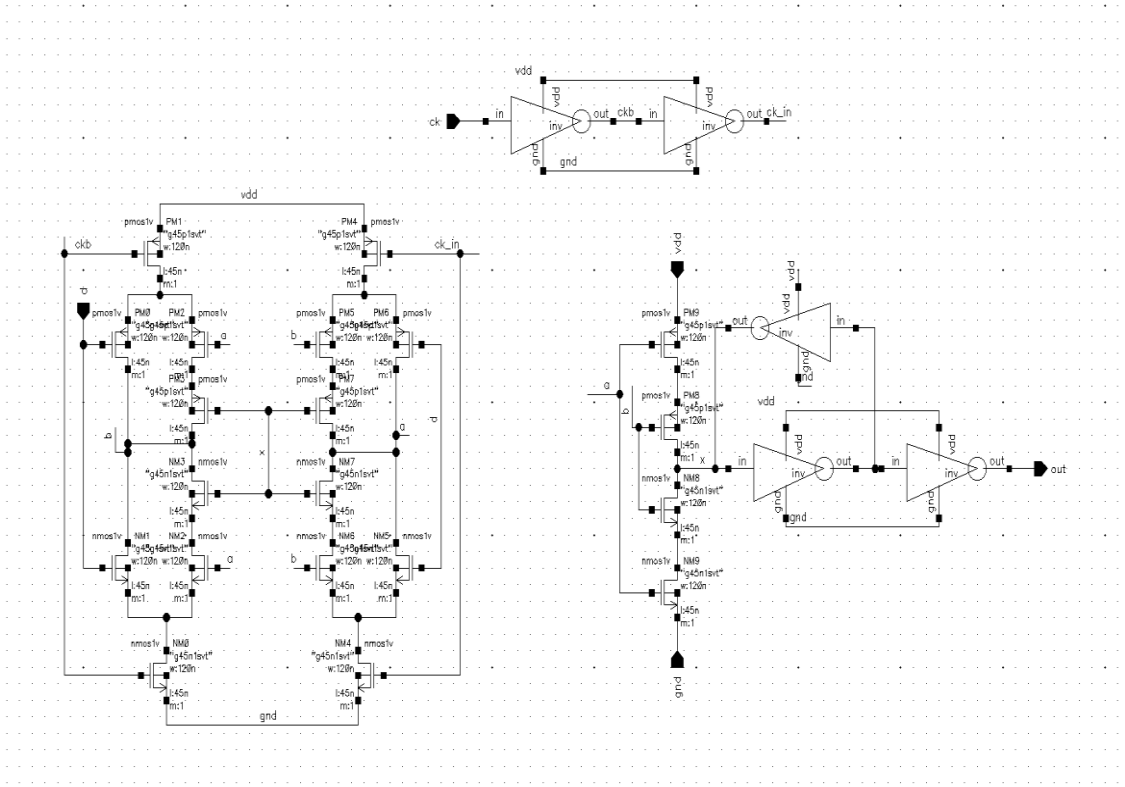

Figure 12:The transistor level schematic of the FN_C flip-flop.

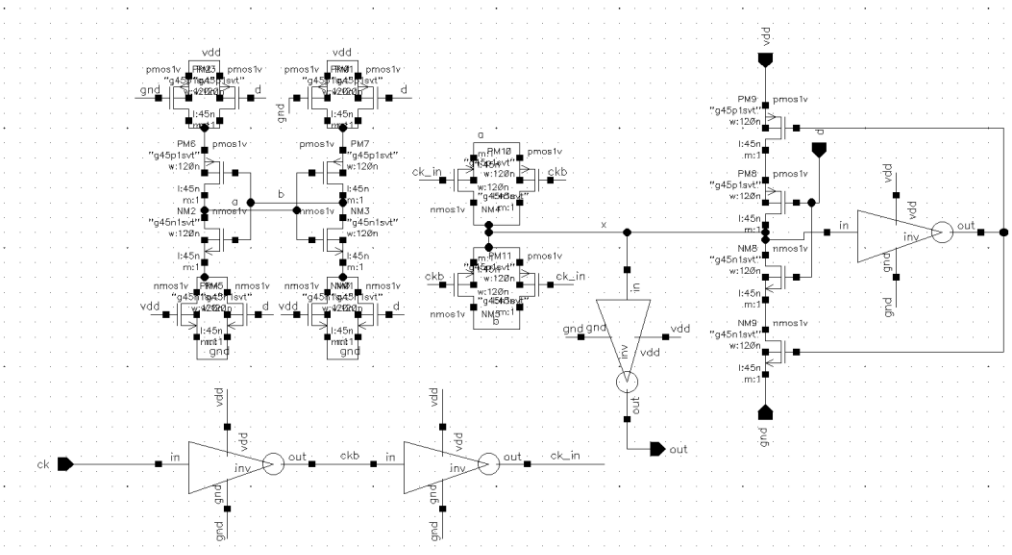

Figure 13:The transistor level schematic of the CTF_C flip-flop.

Table1: Comparison of delay and power of different DET flip-flops in 45nm CMOS Technology

Name of flip-flop	# of T	Power(uw)	Delay(ps)	PDP(fJ)
Latch-MUX Flip-flop [5]	26	2.187	389.0	0.850
LM_C Flip-flop [6]	28	2.812	494.8	1.319
LG_C DET Flip-flop[7]	28	2.894	533.7	1.544
IP_C DET Flip-flop[7]	26	2.115	405.3	0.857
FN_C DET Flip-flop[7]	30	1.778	438.4	0.779
CT_C DET Flip-flop[7]	20	1.259	416.5	0.524
CTF_C DET Flip-flop[7]	28	1.373	342.3	0.469
CT_C DET Flip-flop using dual sleep technique	24	0.933	424.1	0.395
CT_C DET Flip-flop using dual slack technique	26	0.845	430.3	0.363

IV. Conclusion

Sub threshold leakage power consumption is great challenge in nanometer (Scale) CMOS technology, So reducing the effect of leakage power in this paper we are using dal sleep and dual slack techniques and obtaining the reduced power consumption. As the Low power VLSI circuits are having a great demand in digital electronics, The DET flip-flops presented in this paper have a wide range of applications and can be used further for designing shift registers , counters and memories. Cadence is one of the best platform for working on analog and digital circuits. The CT_C flip-flop using both dual sleep technique and dual slack technique are having high performance when compared to existing flip-flop. The circuits further can be designed and simulated using Finfet technology which would be more advantageous.

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