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Design And Implementation of Pulse-Based Low Power 5-Bit Flash Adc In Time-Domain

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Abstract : *Analog-to-Digital Converter (ADC) is implemented using the concept of time-based ADCs (T-ADCs) where the voltage-to-time conveter (VTC) and time-to-digital converter (TDC) blocks are used. The input analog signal is transformed into timing stamps depending on the level trigger of input voltage in VTC block. Then time is transformed into digital output by using the TDC block. The main advantage of T-ADC is, it resists the use of pre-amplifier stages, operates at low supply voltage, and it supports both low-speed and high-speed applications. Here, a new concept of digital ladder is been proposed where, only digital circuits are used for implementing of complete reference ladder and further a Flash ADC(FADC) is proposed and implemented using sample-and-ramp, comparator and digital circuits in CMOS 130nm technology.*

Keywords: *Flash ADC, T-ADC, Pulse-based, VTC, TDC*

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I Introduction

Now-a-days electronic circuits are being used more often than their analog counterpart because they are less sensitive to noise. The main benefit of preferring digital over analog is, they operate in rail-to-rail, and hence there's no need to rely on signal linearity. Also in digital circuits, the error correction process can be finished efficiently. Due to this reason digital calibration necessity is made in both high, medium and even in low resolution ADCs. The T-ADC concept is proposed in this paper. The main benefit of time- domain converters is the signal linearity can be increased. In T-ADCs, the input signal, Vin is transformed into time (pulses) by using VTC block. Now by using a TDC block, the pulses were been converted into digital output. Fig.1 shows the block diagram of pulse based Flash ADC. The paper is arranged as follows. The full circuit implementation of the paper is explained in Section.2. Section.3 is discussed about the decoding scheme of ADCs. The simulation results were been discussed in Section.4 and the conclusion of the paper is provided in Section.5.

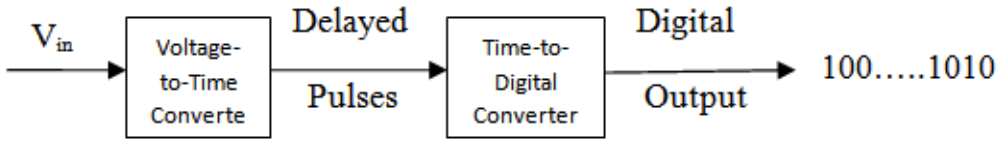

Fig.1 Block Diagram of time based Flash ADC

II Circuit Implementation

A. Voltage-to-Time Converter

The VTC circuit is used to transform the analog signal into delayed time samples. The circuit of proposed VTC circuit is seen in Fig.2 which comprises of sample and ramp circuit along with a comparator. The input analog voltage is given to the gate terminal of PMOS transistor whose source terminal is connected to the transmission gate switch which will turn on when the pulse signal is given to it. Also a current source which is tunable and typically equal to 70µA was used. The main focus is to use a transistor in place of a capacitor [1]. By connecting the source terminal and gate of a normal NMOS transistor, the transistor will act as a capacitor [2]. Due to the replacement of capacitor with transistor, power consumption of the circuit will be reduced. Also a low power comparator is used in this paper which dissipates less power than the proposed model. The schematic of comparator is seen in Fig.3. The comparator will differentiate the output signal of sample and ramp signal with reference signal and gives the output to falling edge pulse generator, where the Vin signal is obtained. The circuit of falling edge pulse generator (PG) from [1] is seen in Fig.4.

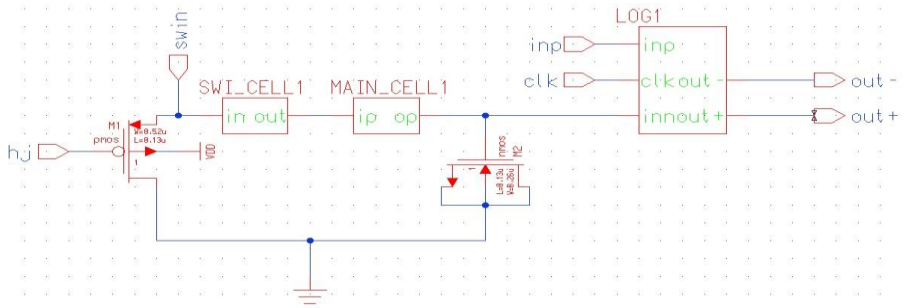

Fig. 2 Schematic of VTC

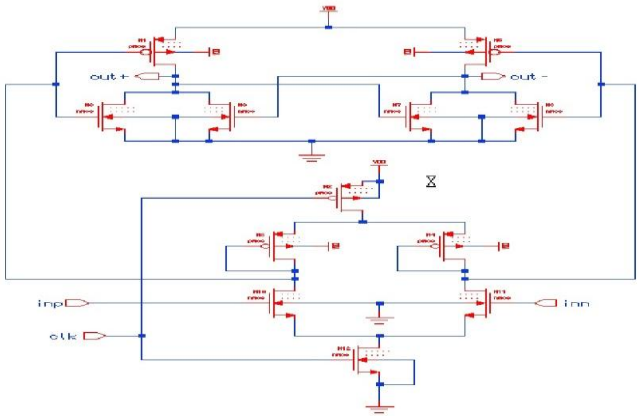

Fig. 3 Schematic of Comparator

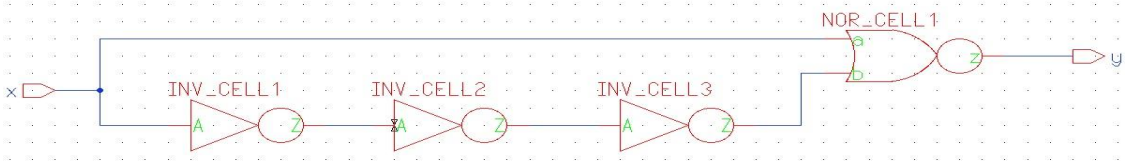

Fig.4 Schematic of falling-edge pulse generator

The layout of the VTC circuit is seen in Fig.5.

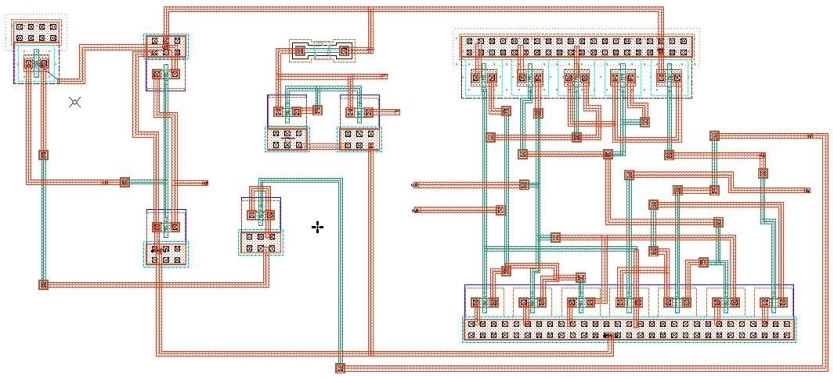

Fig. 5 Layout of VTC circuit

B. Time-to-Digital Converter

The technique of TDC circuit is used to transform the timing pulses into digital code. In this concept, resistor reference ladder of FADC is replaced with digital ladder by using only electronic circuits. This paper mainly focuses on the concept of digital ladder.

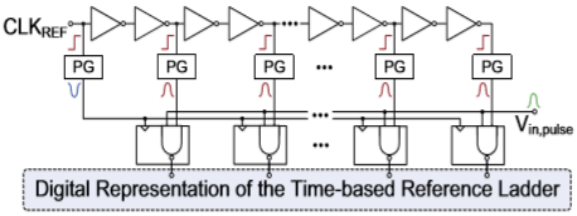

Fig. 6 Schematic of TDC

As seen in Fig.6 [1], the delayed sampling clock signal is given to digital ladder as reference clock signal [1]. This signal used to initiate the digital ladder network of 32 inverters chain. After every even inverter a rising pulse generator circuit is placed which produces a pulse by taking the distinction between clock reference signal and even inverters. The gate-level representation of the rising time PG is seen in Fig.7. The signals from the PG and the input pulses were been given to nand latches (time-domain comparator) as seen in Fig.6. For every individual bit there will be individual PG circuit and individual nand latch.

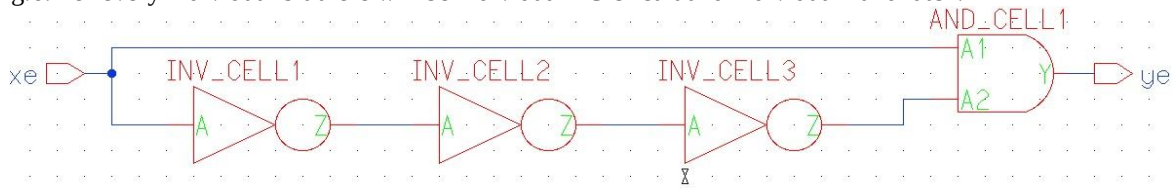

Fig. 7 Schematic of rising-edge Pulse Generator

The transistor level representation of the nand latch [1] is displayed in Fig.8. In nand latch the V_{in} signal is given to the M_3 transistor and the reference signals which are generated from the reference ladder were given to M_4 transistor. Also $CLK_{REF,pulse}$ signal is given to M_1 transistor which indicates the one clock cycle. The operation of latch is as follows. Initially the nand latch was precharged when the reference clock pulse drives the M_3 transistor gate voltage low. Therefore, node X is precharged from low to V_{dd} via transistor M_3, and correspondingly node Y is discharged to ground. After the precharge phase is completed, the reference signal equals V_{dd}, where M_1 turns off and M_6 turns on indicating the latch entering sensing phase. Each latch receives

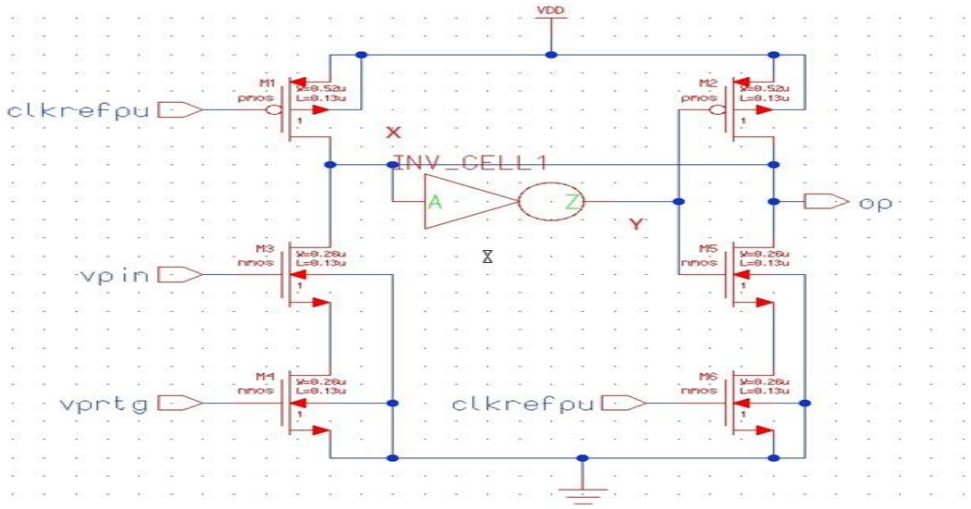

Fig. 8 Schematic of Nand latch

an input pulse whose timing corresponds to applied input voltage (output of VTC), along with the corresponding reference signal. The nand latch output will change only if V_{in} signal and the corresponding reference pulse delivered simultaneously. Finally, transistors M_4 and M_5 drive output V_{out} low. In this way a set of 16 latch outputs were been given before the latch is precharge for next conversion cycle. The execution of TDC circuit in the mentor graphics tool is seen in Fig.9 and its layout in Fig.10. It consists of inverters, PGs and nand latches.

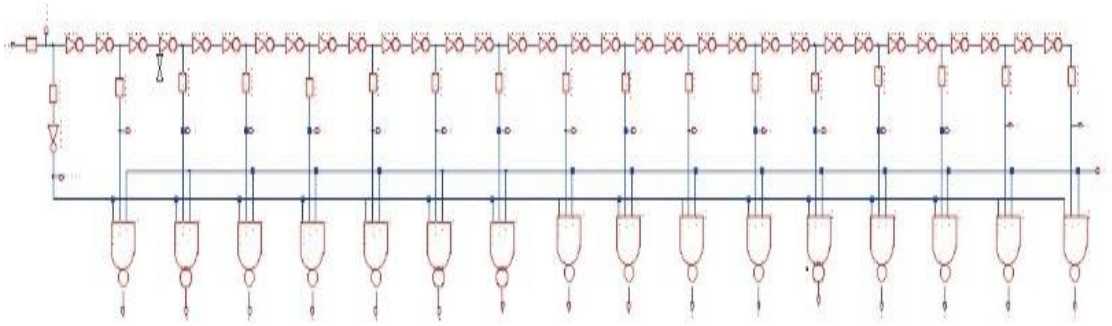

Fig. 9 Implementation of TDC in mentor graphics

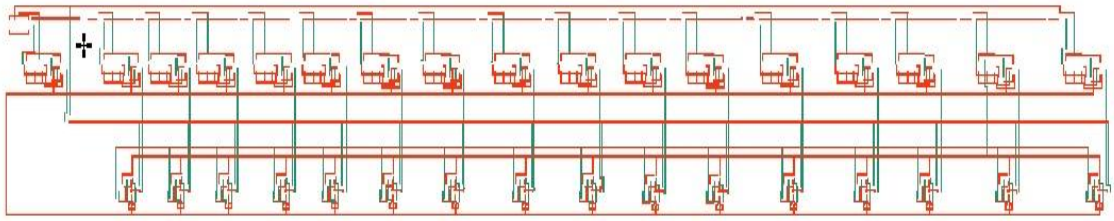

Fig. 10 Layout of TDC

III Decoding Scheme For Adc

The 16 reference signals can result in a resolution of 4-bit ADC by using thermometer coding. These reference signals can be treated as reference pulses or levels. To increase the quantization levels, a special decoding method is proposed. Here, the V_{in} signal is made to design slightly wider to the reference signals. Due to that, there will be a situation occurring where the V_{in} signal will be overlapping with multiple reference pulses. Therefore equivalent latch outputs will be zero at the end of the clock cycle. As seen in Figure 11, the V_{in} signal is overlapped with the reference signal P_{10} therefore the equivalent latch output will be discharged to zero and the final output at nand latches will be "1111111110111111". By using the traditional thermometer to binary coding these 16 bits can transformed into 5 bit digital code as seen in Table 1 [1]. To increase the number of levels, the V_{in} signal is made to design slightly wider to the reference signals. So, that the input pulse will be overlapped with two reference pulses. Due to this scheme, the levels will be doubled and results in clear output. If the V_{in} signal is made to be narrow than the referral pulses, and then there will be a chance that the V_{in} signal will not overlap with any of the referral signals. Therefore, nand latches produce output as "1111111111111111".

Table 1 Decoding look-up table

Latch Output	Final Output	Digital	Decimal value
1111111111111111	00000		0
1111111111111110	00001		1
1111111111111100	00010		2
1111111111111101	00011		3
……	…		..
1111111111001111	01010		10
1111111111011111	01011		11
……	…		..
1011111111111111	11101		29
0011111111111111	11110		30
0111111111111111	11111		31

IV Simulation Results

VTC circuit simulation results are shown in Fig.11, which shows the VTC circuit output in the last wave (VPIN). Now, the VPIN signal is estimated with the 16 reference signals from the TDC schematic as seen in Fig.12, where the V_{in} signal is overlapping with the reference signal P_{10}, and the equivalent output of O_{10} is

lowered to zero, resembling the change in nand latches as "111111111011111". By using this coding scheme, the device mismatches could be minimized and leads to less conversion errors.

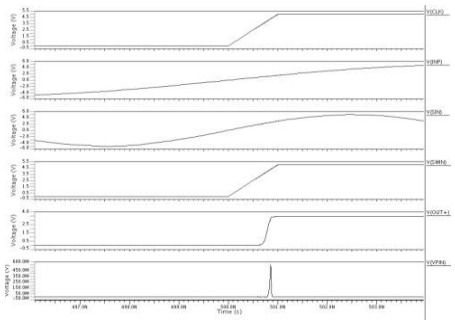

Fig. 11 Simulation result of VTC Circuit

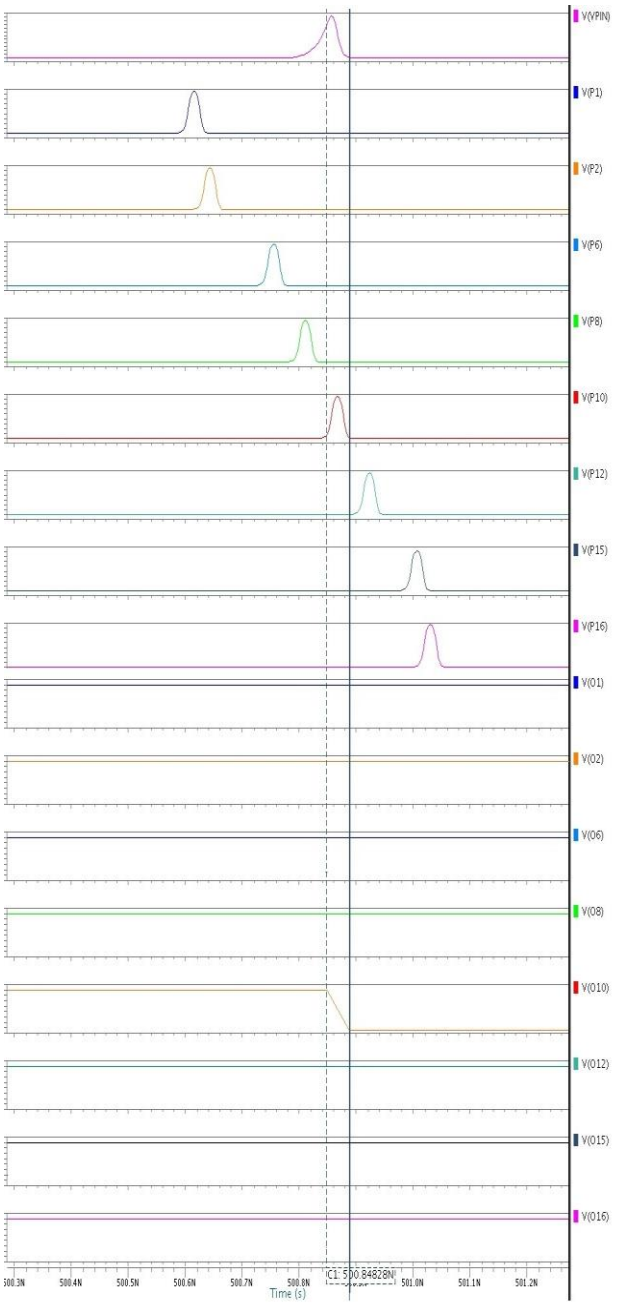

Fig. 12 Simulation result of FADC

Table 2 shows the comparison of power dissipations between the base paper [1] and the implemented work.

Table 2 Comparison between base paper and proposed paper

	Power Dissipation
Reference Paper [1]	1.7801 milli watts
Extension Work	0.07645 milli watts

V Conclusion

A concept of time-domain ADC is presented in this paper. Based on this concept, a fully-digital pulse based FADC prototype was proposed. The voltage-to-time converter is based on the sample and ramp circuit and comparator. The time to digital conversion is performed within a single clock cycle. The prototype ADC is developed in a standard CMOS 130nm technology and the power dissipated by this proposed model is 76.45µW.

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