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Design and implementation of low power, area efficient, multiple output voltage level shifter using 45nm design technology

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Abstract: *To ensure intercommunication between circuit modules which are working in different voltage domains voltage level shifters are used. The improving VLSI technologies reduce the silicon area of the circuit, increases circuit performance. The power consumption should be reduced in order to enhance the life of the batteries used in hand held devices. Thus an advanced design for multiple output high voltage level shifters is proposed in this project.*

Keywords – *Multiple outputs, high voltage shifter, VLSI Analog Design, Cadence Virtuoso, 45nm Technology.*

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I. Introduction

With the growing demand of hand-held devices like cellular phones, transmission devices, multimedia devices etc., low power consumption has become major style thought for VLSI circuits and system. The growing market for IoT (Internet of things) has pushed the requirement of embedded non-volatile memories like EEPROMs with the low amount of memory requirement which are typically up to 10kb [1],[2]. To make possible intercommunication between two or more circuit blocks working in different voltage ranges, Voltage level shifters are used. Level shifter (LS) is a circuit which converts the signal level from one voltage to another, thus helping in the interaction of the circuits operating at different supply voltages. An advanced design for multiple output high voltage level shifters is proposed in this project concentrating on silicon area and power consumption management.

II. Literature review

Voltage level shifter is required when the chip is operating at multiple voltage domains. A signal in one voltage domain may have a voltage range which is different to the signal in another voltage domain. For example if one block works with 1.8V as logic high and 0V as logic low, cannot be directly communicate with another block which has 5v as logic high and 0V as logic low. Circuits close to the memory core are operative at high voltages i.e. EEPROM cell needs high voltages for memory write and erase operations but the signals returning from digital controller or microcontroller unit are standard low voltage signals . Thus these circuit blocks require voltage level shifters for intercommunication. This difference in the voltage range may cause unreliable functioning of the destination domain. Hence Level shifter cells are inserted in the voltage domain crossings and its block diagram representation is shown in Fig.1.

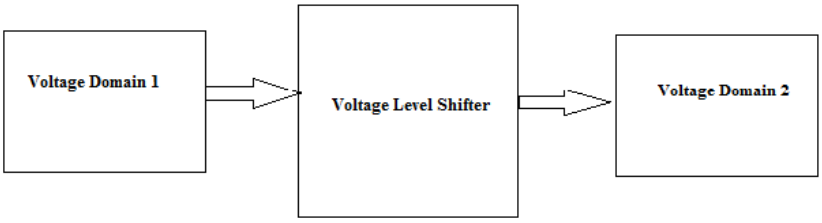

Fig.1: Block diagram of voltage level shifter.

In large embedded systems consisting number of circuit blocks with different voltage domains, if one block needs to communicate with many blocks then it requires multiple output level shifter. Fig.2 shows the block diagram of a unidirectional multiple output level shifter. Using unidirectional shifter one block can send data to other block but cannot receive from other. For the two way communication bi-directional shifters are used.

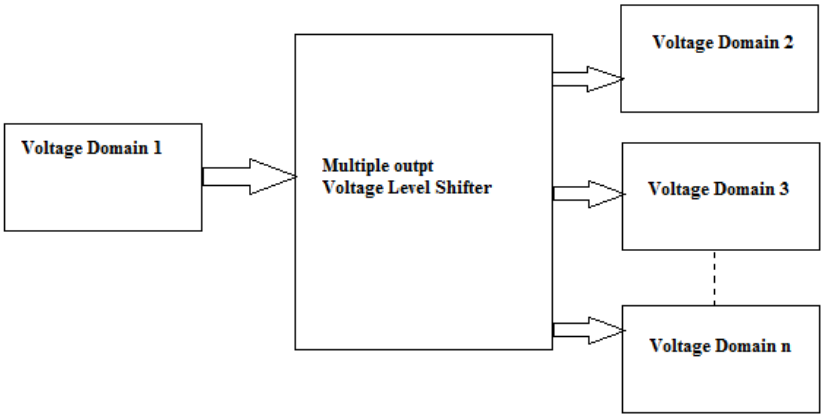

Fig.2: Block diagram of a unidirectional multiple output voltage level shifter.

Conventional unidirectional multiple output circuits are shown below. Fig.3 shows the conventional high voltage multiple level shifter and Fig.4 shows the conventional high voltage level shifter with diode clamping. These circuits have the demerits of unstable nodes and poorly driven output levels if one of the outputs drops due to coupling or charge loss. The Fig.5 shows the advanced design for the high voltage level shifters. They have introduced half latch [1] circuits in order to pull the node voltages and to maintain the stability.

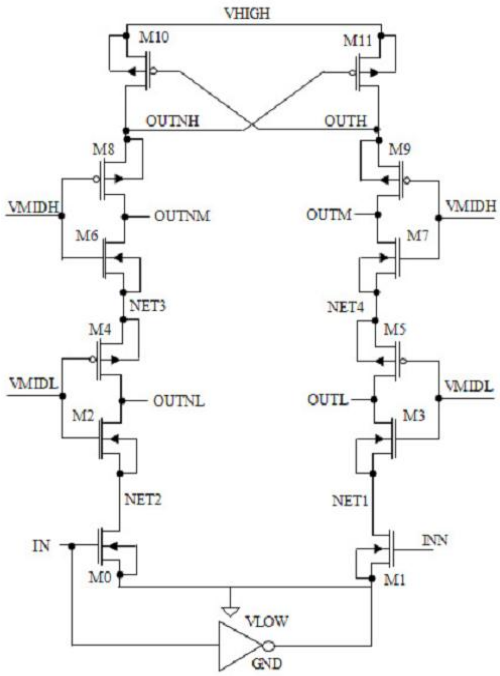

Fig.3: Conventional high voltage multiple level shifter.

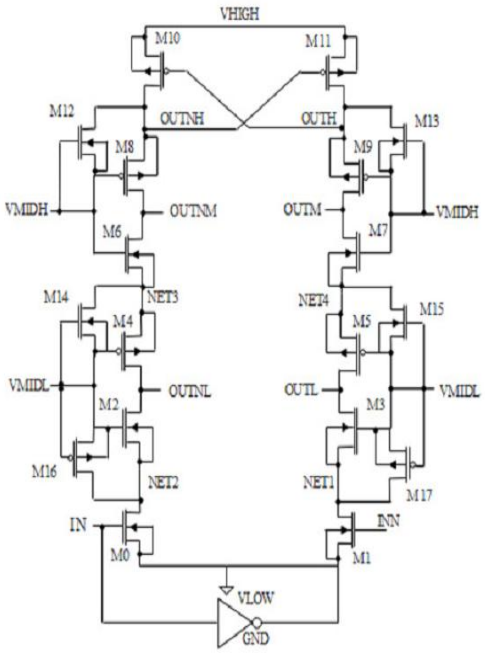

Fig.4: Diode clamped high voltage level shifter

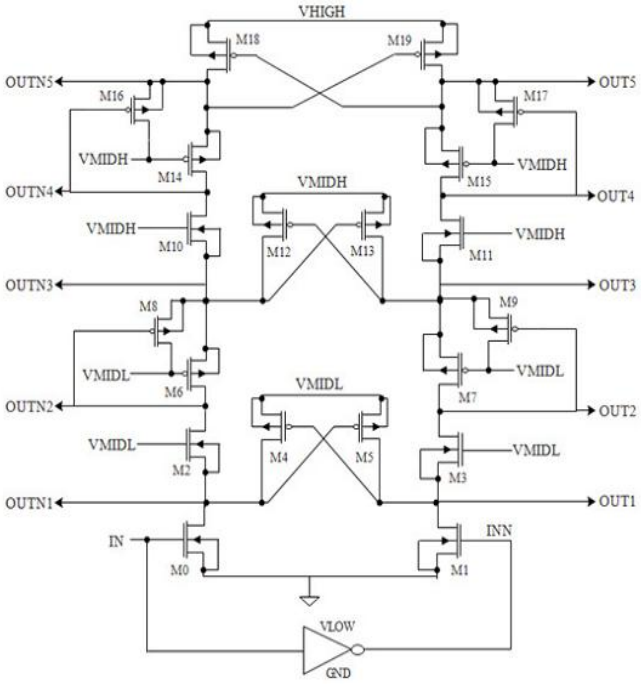

Fig.5: Stress relaxed multiple output voltage level shifters [1]

The half latch coupled multiple output voltage level shifter circuit is taken as the base paper and the design proposed is having four supply voltages namely, V-high = 13.5V, V-midh = 9V, V-midl = 4.5V and V-low = 1.8V. Out5, Out4, Out3, Out2 and Out1 are the converted outputs and Outn5, Outn4, Outn3, Outn2, outn1 are the corresponding inverted outputs respectively. Additional input named as "mode" using which the circuit can work in two modes in order to reduce the power consumption. Mode input acts as an enable signal to disconnect high voltage power supply (V-high and V-midh). Two input multiplexers or simply a signal enabled switches can be used. When mode signal is fed with logic high the circuit acts like normal half latch coupled multiple output high voltage level shifter and gives all the 5 outputs. Circuit can be worked in mode-2 by applying 0v to the mode input. In the mode-2 it will give 3 low level outputs. The proposed design is shown in Fig.6.

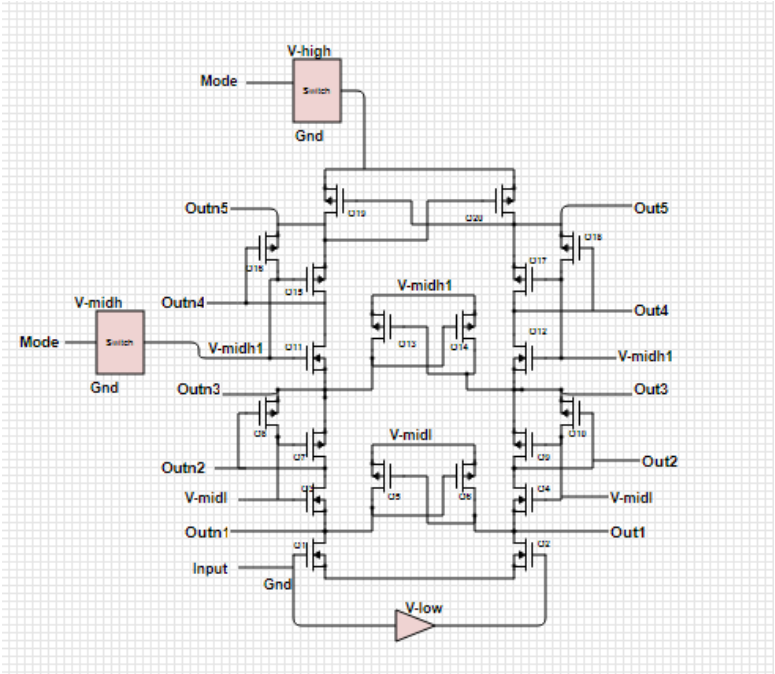

Fig.6: Proposed design for multilevel shifter.

III. Implementation

The circuit Schematic is designed using 45nm technology Cadence Virtuoso software tool. Stress Relaxed Multiple Output High-Voltage Level Shifter is taken as the base paper [1]. The circuit is further modified by introducing additional input named as Mode signal. Designed circuit schematic is shown in the Fig.7 below. The circuit can be operated in 2 modes namely mode-1 (5 outputs) and mode-2 (3 outputs). When mode signal is set to high (i.e. mode = 1.8V) the shifter operates in mode-1. In this mode all the 5 outputs are active and will shift output voltage as Out1 = 0 to 4.5V, Out2 = 0 to 9V, Out3 = 4.5V to 9V, Out4 = 4.5V to 13.5V and Out5 = 9V to 13.5 V. When high output voltages are not necessary then active low signal (0V) is applied to mode input in order to operate circuit in mode-2. In this mode it will disconnect high voltage power supply and give 3 outputs as Out1 = 0 to 4.5V, Out2 = 0 to 9V, Out3 = 4.5V to 9V. Transient response of the schematic designed obtained by ADE (Analog Design Environment) is shown in the Fig.8.

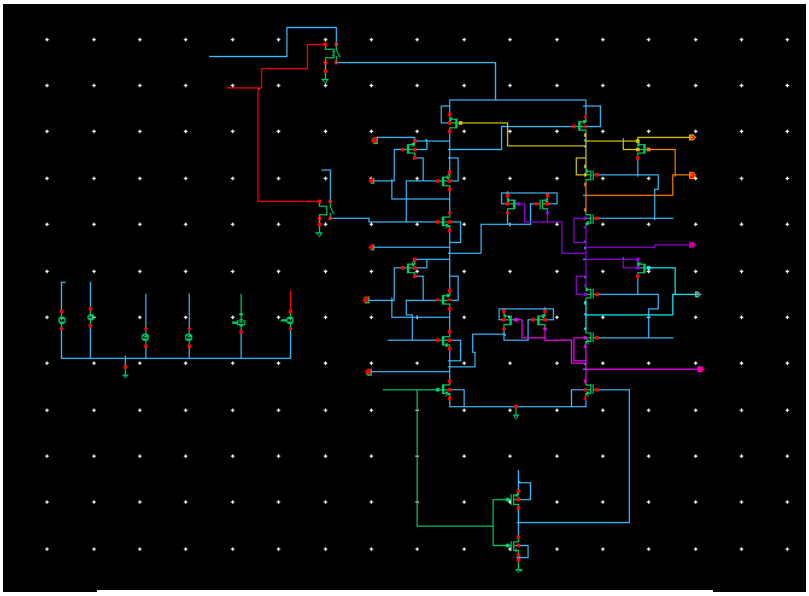

Fig.7: Circuit schematic in 45nm Cadence Virtuoso tool.

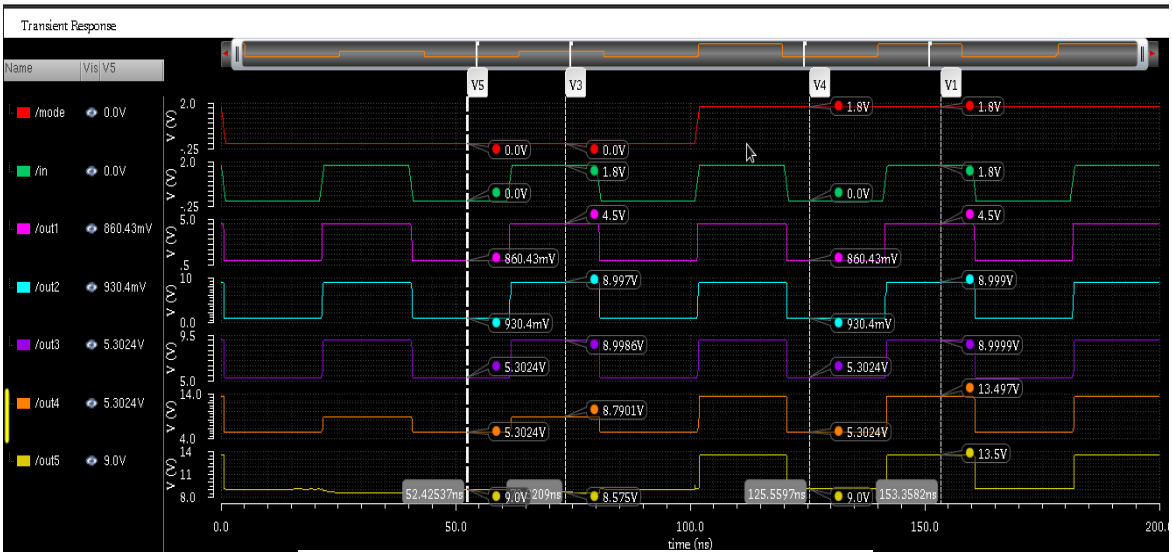

Fig.8: Transient Response of the proposed schematic.

The layout is designed for the proposed schematic using virtuoso Layout XL tool. Symbol creation for a half latch unit and repetitive usage of same block in the circuit schematic reduces the complexity in designing the layout. Layout is designed with no DRC errors and Layout versus schematic is matched properly. Since 45nm technology tool is used, the layout designed is having very less area of 16.19µm^2 is shown in fig 9.

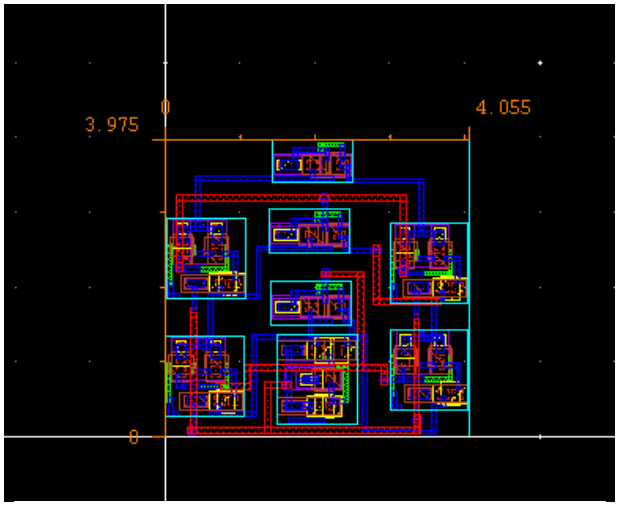

Fig.9: Layout design of the proposed circuit schematic.

IV. Outcome

Existing approach had single mode of operation where as in proposed design can be worked in two modes i.e when it needs only lower output voltages it is worked in Multiple mode 2 by giving reset signal to mode input. The comparisons between existing and proposed design are shown in the Table.1. In mode-1it gives 5 outputs and in mode-2 it gives 3 outputs. Thus mode-2 operation consumes less power. Average power consumed by proposed design over a period of 200ns is listed in Table.2. It is observed that average power consumed by circuit in mode-1 is 392.8µW and that in mode-2 is 267.4 µW.

Table 1: Comparisons between existing and proposed design.

	Existing work (Paper [1])	Proposed work	
		Mode-1	Mode-2
No.of Outputs	5 outputs	5 outputs	3 outputs
o/p voltage	0 to (4.5- 13.5)V	0 to (4.5- 13.5)V	0 to (4.5- 9)V
i/p voltage	0-1.8V	0-1.8V	0-1.8V
Technology	110nm HVCMOS	45nm CMOS (Cadence virtuoso tool)	
Area	870µm^2	16.19µm^2	

Table 2: average power consumption over a period of 200ns.

	Mode-1	Mode-2
Average Power consumed (for a period of 200ns)	392.8 µW	267.4 µW

V. Conclusion

The proposed multiple output high voltage level shifter circuit designed using 45nm technology has efficient layout area, low power consumption technique and works in two modes of operation. It converts input signal to 5 different output domains in mode-1 and 3 output domains mode-2.

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