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Design & Implementation of Squarer Circuit for Trans-linear Based CMOS Analog Multiplier.

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Abstract: *This paper deals with a advanced method to design CMOS analog multiplier which operates in four quadrants. Main core of analog multiplier is two common pairs of squarer circuits which are based on translinerar principle. This makes the symmetrical configuration for the multiplier circuit and also minimizes error, because the resulted error in two squarer circuits are subtracted from each other. Also, both squarer circuits use single bias branch instead of two which causes to consume low power in comparison with previous multiplier structures. The designing of squarer circuit and simulation is carried out by cadence virtuoso schematic entry tool, with 90nm CMOS technology, supply voltage 1.2V and bias current is 10uA.*

Keywords: Analog multiplier, Translinear loop,

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I. Introduction

In analog-signal processing always there is need of circuit that takes two analog inputs and produces an output proportional to their product. Such circuits are termed analog multipliers. It has many applications in automatic gain controlling, modulation, detection, frequency translation, phase locked loop, square rooting of signals, neural networks and fuzzy integrated systems [1]. In ideal conditions, the output of analog multiplier is defined as the linear product of two input signals X and Y, which results in Z = K x X x Y at the output (K is a constant with a suitable dimension). One of the important class of multipliers is based on translinear loop principle wherein the sum of the currents in a circuit flowing in clockwise direction is equal to that flowing in anticlockwise direction. This paper discusses an implementation of a major block of such multiplier circuit viz. a squarer circuit, using a basic algebraic equation for the product XY as $(X + Y)^2 – (X – Y)^2$. The details of this along with simulation results are presented in this paper.

1.1 Translinear Principle:

Translinear Principle Provide simple and neat method of implementing mathematical functions. This principle is based on current mode since all the inputs and outputs are in the current form. The operation of translinear principle is based on the relationship between current and junction voltage. Since in transistorized circuits implementing translinear function as shown in Fig.1, the junction capacitance does not have to be significantly charged or discharged, the junction voltage swings are limited. This results into circuits which can work at high speeds. This further avoids the problem of slew rate limiting. This justifies the choice of current mode to process the signals. Secondly, translinear principle is basically insensitive to temperature and process parameters.

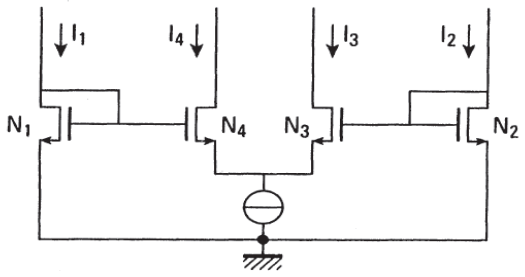

Fig.1 Translinear Loop Circuit

The translinear principle always applied to the circuit in which the number of PN junctions are connected in a continuous loop [3]. Transistors connected in a loop can be identified as clockwise (CW) and anticlockwise (ACW) depending on the direction of current flow through the junction. The loop should follow the conditions as follows:

1. All transistors are in saturation.
2. The number of ACW NMOS devices is equal to number of CW NMOS devices.
3. The number of ACW PMOS devices is equal to number of CW PMOS devices.

In the work of this paper, translinear principle is used for the implementation of squarer circuit, which is having two Translinear loops. The implementation details about squarer circuit and the results thereof are presented in this paper.

II. Design of Experimentation.

2.1 Current Mode Squarer Circuit

Fig. 2 displays the squarer circuit in which the inputs are in current form. The main core of this circuit consists of two dual Translinear Loops (TL); the first loop consists of transistors M_1, M_2, M_3 and M_4, and the second loop consists of transistors M_1, M_2, M_5 and M_6. For the MOS transistor operating in saturation region, the current voltage relationship is expressed as:

$$I_{DS} = K(V_{GS} - V_T)^2 \tag{1}$$

$$V_{GS} = V_t + \sqrt{\frac{I_{DS}}{K}} \tag{2}$$

where, $K=0.5\mu_0 COX(W/L)$ the tran-conductance of the transistor and COX is the oxide gate capacitance in unit area μ_0 is the electron mobility, W/L is the ratio of width to length, V_{GS} is the gate-source voltage and Vt is the threshold voltage of the MOS transistor.

Considering the dual TL, which includes transistor M_1, M_2, M_3 and M_4 (Fig 2), apply the Kirchhoff's voltage Law (KVL) to this loop; which gives:

$$V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4} \tag{3}$$

Assuming the same value for trans-conductance of the transistors, using (1) and (2) and considering that the drain-source currents of transistors $M_1$and M_2 are determined by the bias current of I_B :

$$\sqrt{I_{DS1}} + \sqrt{I_{DS2}} = \sqrt{I_{DS3}} + \sqrt{I_{DS4}} \tag{4}$$

$$\sqrt[2]{I_B} = \sqrt{I_{DS3}} + \sqrt{I_{DS4}} \tag{5}$$

By applying the Kirchhoff's current Law (KCL) for node A, I_{DS3} obtained as:

$$I_{DS3} = I_{DS4} + I_{in} \tag{6}$$

Now, inserting (6) into (5)

$$\sqrt[2]{I_B} = \sqrt{I_{DS4} + I_{in}} + \sqrt{I_{DS4}} \tag{7}$$

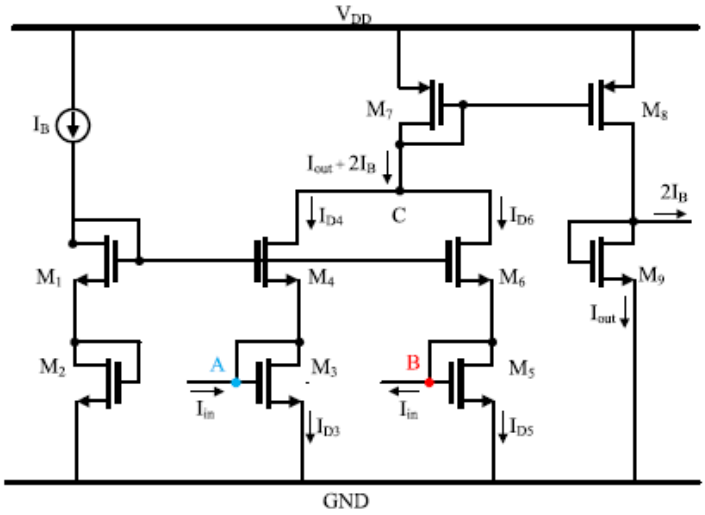

Fig2. Basic Schematic Diagram of the Proposed Squarer Circuit

Squarer both sides of (7) two times, we get,

$$16I^2{}_B + I^2{}_{in} + 8I_BI_{in} = 16\ I_BI_{DS4} \tag{8}$$

$$I_{DS4} = \frac{I^2{}_{in}}{16I_B} - \frac{I_{in}}{2} + I_B \tag{9}$$

Similarly the current I_{DS6}, for the second dual TL consisting of is including M_1, M_2, M_5 and M_6:

$$I_{DS6} = \frac{I_{in}^2}{16I_B} + \frac{I_{in}}{2} + I_B. \tag{10}$$

By applying KCL for node C (Refer Fig. 2):

$$I_{out} + 2I_B = I_{DS4} + I_{DS6}. \tag{11}$$

Thus, the output current I_{out} of proposed squarer circuit is obtained as follows:

$$I_{out} = \frac{I_{in}^2}{8I_B}. \tag{12}$$

2.2 The Multiplier Circuit

The working principle of the proposed analog Multiplier is based on the following algebraic equation, with X and Y as multiplier operands [5]:

$$(X+Y)^2 - (X-Y)^2 = 4XY \tag{13}$$

In the work of this paper X and Y are in the form of current parameters I_X and I_Y.from the above equation it is seen that the product of XY is obtained by the difference of output of two squarer circuits.one is addition of operands and another is substraction of operands I_X and I_Y.

$$I_{in1} = I_X + I_Y \qquad I_{in2} = I_X - I_Y$$

,

By considering (12)

$$I_{o1} = \frac{I^2{}_{in1}}{8I_B} \tag{14}$$

$$I_{o2} = \frac{I^2{}_{in2}}{8I_B} \tag{15}$$

The multiplication of two signals is obtained by taking the difference between two signals as mentioned above.

$$I_{out} = I_{o2} - I_{o1} \tag{16}$$

$$I_{out} = \frac{I_X I_Y}{2I_B} \tag{17}$$

In (17), output of multiplier circuit which is product of input signals divided by $2I_B$ where I_B a constant current source is. In the work of this paper I_B is taken as 10 µA.

2.3 Triangular Current Source:

As squarer circuit is based on translinear principle, input to the circuit must be a linear current source. This requirement is fulfilled using triangular current source available in Cadence analoglib library. The frequency set for this source was 1MHz while the peak amplitude was set at ±35µA. Settings for Delay time and Pulse width were equal to 0 while Rise time and Fall time was set to 500ns so as to set the total period of triangular current signal as 1 µs.

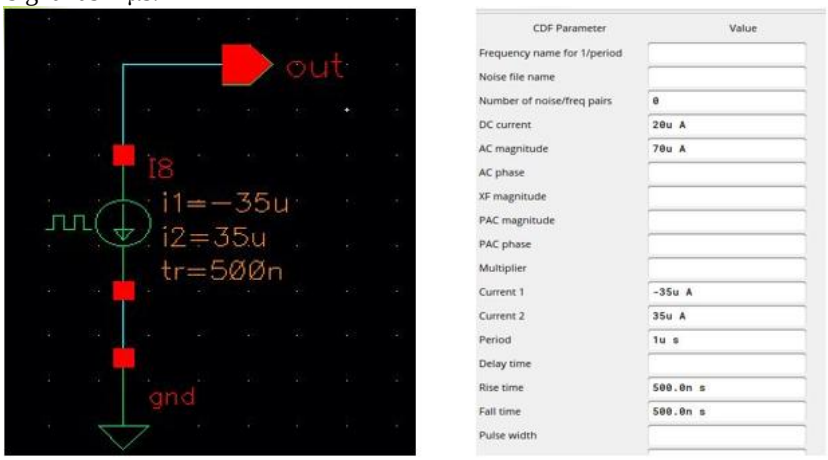

Fig.3: Input Triangular Current Source and its Specifications.

Fig.4 shows the output of a triangular current source with amplitude of ±35 µA. and 1MHZ frequency.

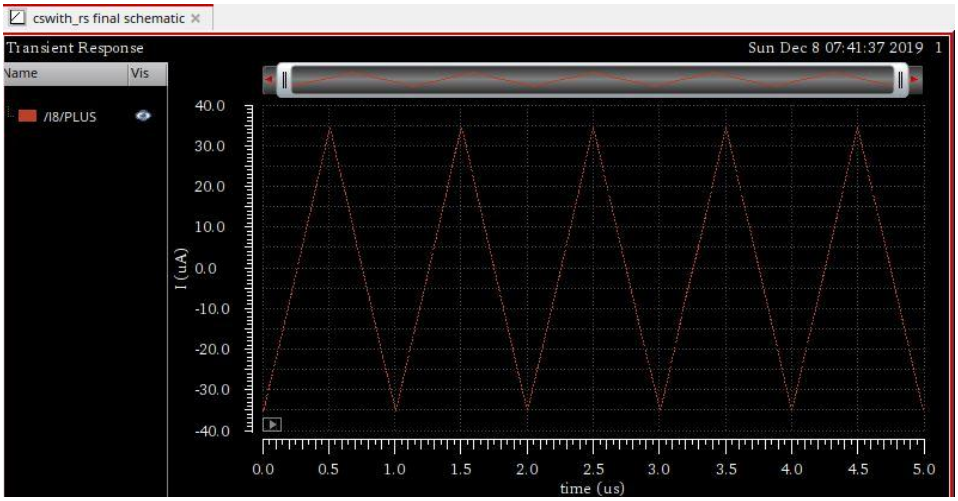

Fig.4: Output of a Triangular Current Source

III. Simulation Results

3.1 Translinear Loop

The basic circuit of translinear loop as shown in Fig. 4 was implemented using Cadence Virtuoso schematic entry tool with, 90nm technology, 1.2 V supply voltage and 30 µA constant current source for cross checking the TL function. Each of the four NMOS transistors were set with W/L ratio equal to 2.5µm/500nm. For analyzing the result of translinear loop, DC analysis was carried out. The simulation results were checked for the sum of currents flowing in clockwise and anticlockwise direction which found to be almost equal within 0.035% error establishing TL principle.

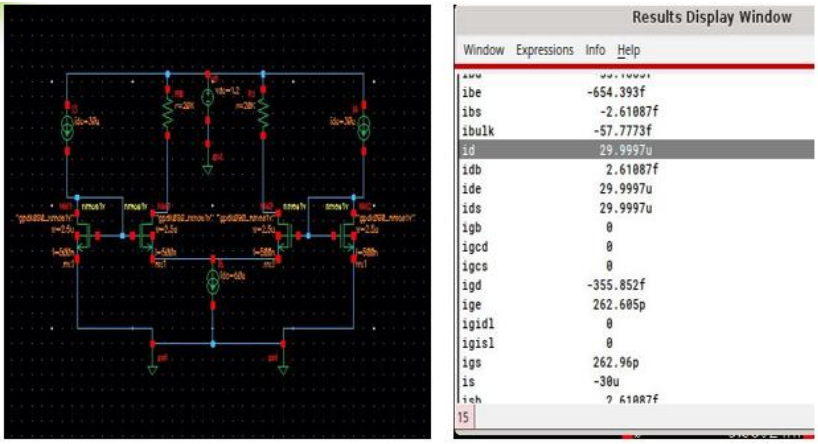

Fig.4 Implementation of Translinear Loop and its Result.

3.2 Simulation of Squarer Circuit:

Fig.5 shows the circuit diagram of squarer circuit consisting of two TL loops of Fig.4. The bias current was set to 10µA. and all the other transistor parameters are same as Fig.4 (Translinear loop).and the settings of triangular input current source is same as Fig.4.

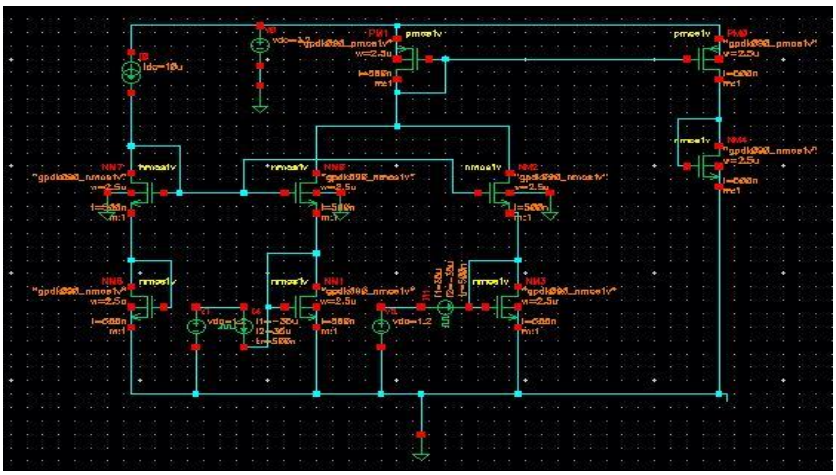

Fig.5: Implementation of Squarer Circuit.

3.3 Outpout Waveform of Squarer Circuit:

Consider the (12) for the calculation of output of the squationg circuit. Since the bias current set was at 10 µA and as per (11) viz. $I_{out}+2I_{B,}$ an offset of 20 µA is added.

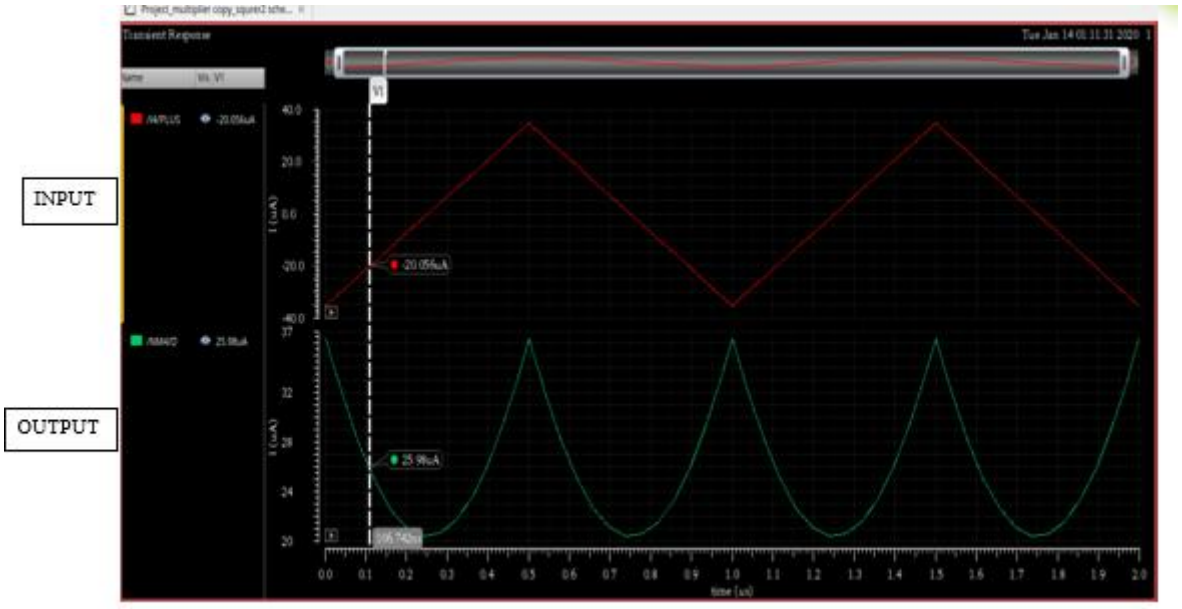

Fig.6: Output of a Squarer Circuit.

Fig. 6 above depicts the input traingular current waveform and the outut current waveform . The results at various timings corresponding to difference of 10μA in consequitive values are presented in Table 1. Here as mentioned above, 20 μA is subtracted from I_{out} to compute percentage errors between expected and simulated values.

Table 1. Results of Squarer Circuit

I_{in}(μA)	I_{out}(μA)	$\lvert I_{out}\rvert$-2I_B (μA)	$\frac{I^2_{in}}{8I_B}$(μA)	Error(μA)
- 35	35.55	15.55	15.31	0.24
-30.8	32.279	12.279	11.85	0.429
-25.037	28.245	8.245	7.83	0.415
-20.05	25.327	5.327	5.025	0.302
-15.07	23.023	3.023	2.83	0.193
-10.09	21.36	1.36	1.27	0.09
-5.1	20.35	0.35	0.325	0.025
0	19.99	-0.01	0	0.01
5.1	20.298	0.298	0.325	-0.027
10.09	21.237	1.237	1.27	-0.033
15.07	22.918	2.918	2.83	0.088
20.05	25.25	5.25	5.025	0.225
25.063	28.211	8.211	7.85	0.361
30.019	31.629	11.629	11.26	0.369
35	35.341	15.341	15.31	0.031

IV. Conclusion

Translinear principle and squarer circuit are successfully implemented in Cadence Virtuoso and output of squarer circuit matches with theoretical results with absolute result less than 0.5μA. The results obtained of squarer circuit are in tune with the results of literature [5].

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