

Optimized Design of an ALU Block Using Power Gating Technique

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Abstract: Power is the limiting factor in traditional CMOS scaling and must be dealt with aggressively. With the scaling of technology and the need for high performance and more functionality, power dissipation becomes a major bottleneck for a system design. Power gating of functional units has been proved to be an effective technique to reduce power consumption. This paper describe about to design of an ALU block with sleep mode to reduce the power consumption of the circuit. Local sleep transistors are used to achieve sleep mode. During sleep mode one functional unit is working and another functional unit is in idle state. i.e., it disconnects the idle logic blocks from the power supply. Architecture and functionality of the ALU implemented on FPGA and is tested using DSCH tool. Power analysis is carried out using MICROWIND tool.

Keywords: Low Power, Power gating technique, Sleep mode, FPGA

I. Introduction

The increasing speed and complexity of today's designs implies a significant increase in the power consumption of very-large-scale integration circuits. Voltage is increased to attain higher speed of operation with the penalty of increased power consumption. To meet this challenge, researchers have developed many different design techniques to reduce power. CMOS technology scaling has now moved to a power constrained condition. Circuit techniques to reduce chip standby leakage have become a key enabler. Scaling is a trade off between performance and leakage. One of the key features that led to the success of complementary metal-oxide semiconductor technology was its intrinsic low-power consumption [2]. This meant that circuit designers and electronic design automation (EDA) tools could afford to concentrate on maximizing circuit performance and minimizing circuit area. Another interesting feature of CMOS technology is its nice scaling properties, which has permitted a steady decrease in the feature size, allowing for more and more complex systems on a single chip, working at higher clock frequencies [1]. In fact, power consumption is regarded as the limiting factor in the continuing scaling of CMOS technology.

II. Need For Low Power

As the demand for high speed, Low power consumption and high performance continues to grow each year, there is a need to scale the devices to smaller dimensions. As the market trend moves towards a greater scale of integration, the move toward a reduction in supply voltage also have the advantage of improving the reliability of the chip. As the complexity of the chip increases design problems occurs such as layout of a chip and simulation for the circuit and these are all becomes more intense. Power consumption is regarded as the limiting factor in the present technology. High power supply affects the temperature and further influences the cooling cost of the chip. If the temperature increases it directly reflects the environmental problems. Noise and reliability [3] is the one more big issue in the field of high power consumption devices. With all this, high power consumption will defiantly degrade Battery life of the electronics devices.

III. Low-Power Design Methodologies

A significant amount of recent research has sought to reduce the power consumption. Power consumption can be reduced at many levels, from the circuit level to the application level. This paper seeks to explore the limits of power reduction available due to optimizations at the architecture level. This work identifies three broad categories of wasted power that either has been potentially be targeted for reduction. Those categories are process technology, reducing switching activity and power down modes. The focus of this research is reduction of power dissipation in Architectural level. These categories of research in architectural power reduction assuming solutions that do not fundamentally hang the system or its performance [3], [4].

A. Process Technology

The adaptation of process technology will place a major role in low level system design. It includes the technologies of reduction of capacitance and reducing leakage power, supply power and higher density of integration.

B. Reducing Switching Activity

To reduce power dissipation effectively low power methodologies can be used. Since designers have no influence on V_{dd} , and switching activity is the remaining one to influence. Methodologies for reducing the switching activity are minimization of glitches and minimization of number of operations, using low power bus. Scaling down features requires lowering the threshold voltage, which increases leakage power.

C. Power down Modes

When some modules of the program are idle and do not add any functionality to the design at the time but still consume power, that system typically is not working at maximum possible performance. The power down modes will affect the design architecture mode and it plays a major role in the power dissipation of the circuit. Mostly use the power down modes like power gating and clock gating.

IV. Low Power Techniques For Field Programmable Gate Arrays

A) Introduction

Field-programmable gate arrays are ideal for adaptive systems, since they are reconfigurable and can be programmed to implement any digital logic. Applications of such FPGA based adaptive systems include face image recognition, on-line failure recovery and analysis of fire fly synchronization. Traditionally, FPGA research focused on reducing the speed and area overhead. In recent years, much of the focus has shifted to improving the energy efficiency [9]. This shift is due to process scaling and increased demand for low power applications. Although process scaling reduces the energy needed to perform a given computation since wires and transistors are smaller, it increases power dissipation per unit area and therefore the overall power for a given die size

B) Power dissipation in CMOS

In digital circuits power dissipation is categorized into two types: peak power and time-averaged power consumption. Peak power is a reliability issue that determines both the chip lifetime and performance.[6]The voltage drop effects and Transistor sizing will affect the performance of a design due to the increased gate and interconnect delay. This large power consumption causes the device to overheat which reduces the reliability and lifetime of the circuit. The time-averaged power consumption in conventional CMOS digital circuits occurs in two forms: dynamic and static [4].

- a) **Dynamic power dissipation** Dynamic power dissipation occurs in the logic gates that are in the process of switching from one state to another. During this process, any internal and external capacitance associated with the gate's transistors has to be charged, thereby consuming power.
- b) **Static power dissipation** Static power dissipation is associated with inactive logic gates i.e. not currently switching from one state to another. Static power is caused by leakage currents while the gates are idle that is, no output transitions. Static power is important during standby especially for battery-powered devices.

C) Basic Power down Mode Techniques

a) Clock Gating

Clock power is an important component of overall dynamic power. One way to reduce clock power is to use clock gating, which dynamically disables the clock in unused parts of the circuit. This avoids the unnecessary power dissipation caused by charging and discharging the clock signal at these unused gates [3].Gating is generally achieved by ANDing the clock signal with a clock-gate signal, which rises whenever the part of the circuit that needs to be gated is active and remains low otherwise.

b) Power Gating

Power Gating has become one of the most widely used circuit design techniques for reducing leakage current in Static power dissipation. [3] This uses high threshold-voltage transistors or sleep transistors in circuit blocks that switch in frequently. Its concept is very simple, but its application to standard-cell VLSI designs involves many careful considerations. The great complexity of designing a power-gated circuit originates from the side effects of inserting current switches, which have to be resolved by a combination of extra circuitry and customized tools and methodologies.

V. Power Gating Methodology

Power-gating technique uses a high V_{th} sleep transistor in series with the pull-up and/or the pull-down of a low V_{th} logic block to reduce leakage power. The sleep transistor can be turned off when the low V_{th} logic block is inactive, thus resulting in a significant reduction of sub-threshold leakage current. Figure 1 shows a sleep transistor used for power gating. A sleep transistor can be a high V_{th} NMOS or PMOS transistor [6]. A PMOS sleep transistor served as a header switch connects the power network to virtual VDD. An NMOS sleep

transistor served as a footer switch connects the ground network to virtual GND. Normally, either a header switch or a footer switch is used to conserve area and reduce timing penalty caused by voltage drop across sleep transistors.

In this paper, consider only footer switch. The logic block in Figure 1 can be as simple as a logic gate. If it is a logic gate in a standard cell library, we call it a power gated cell. If the power gated cells in a standard cell design are used in an isolated manner, i.e., their virtual VDDs are not connected; call this power gating approach fine-grained power gating [3]. If a sleep transistor is shared by a cluster of power-gated logic cells, possibly located in close proximity, such kind of power gating is called coarse-grained or cluster-based power gating. If the virtual VDDs of power gated cells (clusters) in a design are connected together, the sleep transistors of these power gated cells (clusters) are in fact form a transistor network. We call such kind of power gating distributed sleep transistor network.

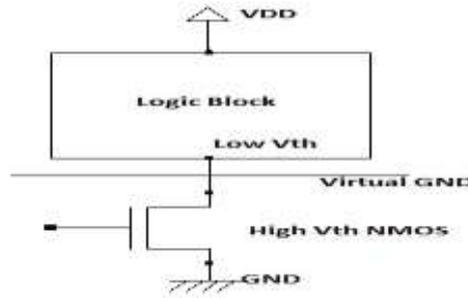


Figure 1. Power gating structure

❖ **Power Gating Considerations:**

- **Library design:** Special cells are needed like switches, isolation cells Power Gating Considerations.
- **Headers or Footers:** What type of switch have to used either small or big and what type of connection use either header or footer connection.
- Which modules, and how many, to be power gated.
- Sleep control signal must be available, or must be created.
- Switches affect source voltages which affect delays
- Power-up & power-down sequencing.
- Controller must be designed and sequencing verified.
- **Transistor Size:** The size of the transistor is measured in terms of W/L ratio. This is also called aspect ratio of transistor. While designing a Power gate, the size of the sleep transistor or switch is also one important consideration.

In the function mode, a sleep transistor is operated in the linear region and can be modeled as resistance and there will be a voltage drop across sleep transistor. Voltage drop can have performance impact and normally, the voltage needs to be confined to certain percentage of VDD such as 5 to 10% of VDD [5].

VI. Alu Design Through Power Gating Methodology

The ALU has four stages, each stage consisting of three parts: a) input b) internal modules and c) output multiplexer. The ALU performs the following four arithmetic operations, ADD, OR, FULL ADDER, INVERTER. The output sections consist of 4 to 1 and 8 to 1 and 16 to 1 multiplexers. These multiplexers were designed using the 2 to 1 multiplexer logic. A set of two select signals has been incorporated in the design to determine the operation being performed and the inputs and outputs being selected.

As from the technique of power gating the proposed ALU Design is shown in Figure 2. ALU logic block is connected to the sleep transistor network. This sleep transistor network functionality is based on the sleep signal logic.

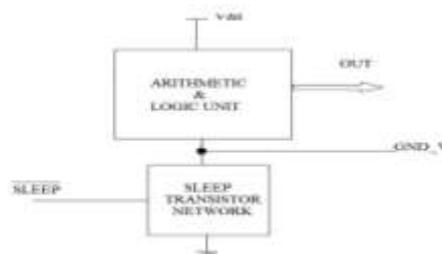


Figure 2. Modified ALU Architecture

Traditional 1 bit ALU:

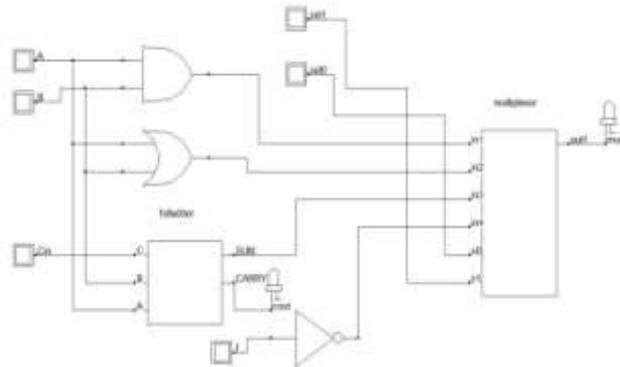


Figure 3. Traditional 1 bit ALU Architecture

As in the power analysis we first design the circuit and after that power estimation is done. Here the estimated power consumed is $2.997\mu\text{W}$.

Optimized 1 bit ALU:

Upgraded ALU architecture is shown in figure 4. As in the case of Optimized ALU, sleep transistor mode of switching technique is being used. NMOS is used as a sleep transistor and this NMOS is connected to the S1. When ever the S1 turns to ON state then the supply rail will be connected to the NMOS transistor and our C_{in} will be connected to full adder block.

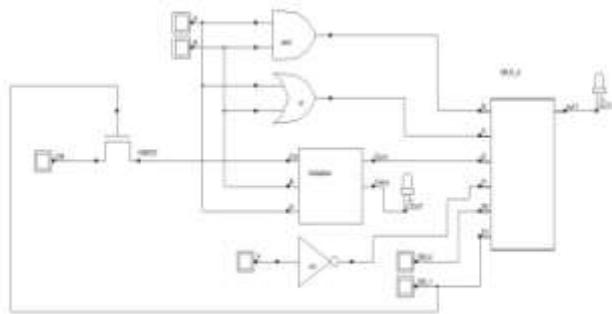


Figure 4. Optimized 1 bit ALU Architecture.

The same procedure is applied to the Optimized ALU also, i.e. design the Optimized ALU circuitry and then estimation of power is done. This estimation of power is $1.277\mu\text{W}$.

For traditional 4 bit ALU design, FOUR 1 bit ALU's are cascaded like as shown in figure 5. For this circuitry also same procedure will be apply.

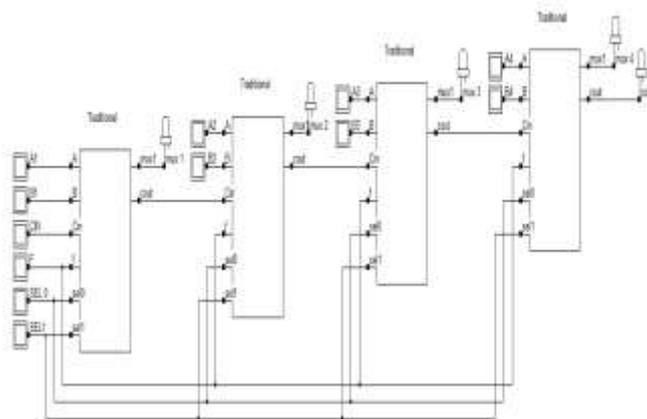


Figure 5. Traditional 4 bit ALU Architecture

The estimated power for the Traditional 4 bit ALU is $20.24\mu\text{W}$. Optimized 4 bit ALU design is shown in figure 6. There is a significant reduction in power is observed. The power estimated was $5.467\mu\text{W}$.

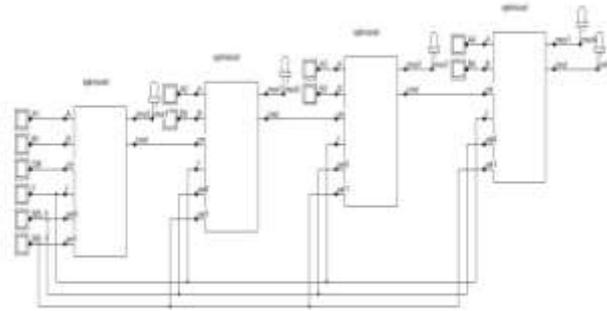


Figure 6. Optimized 4 bit ALU Architecture

Traditional 8 bit ALU architecture is shown in Figure 7. Here EIGHT 1 bit Traditional ALUs are cascaded to perform 8 bit operation. The estimated Power is 30.99 μ W.

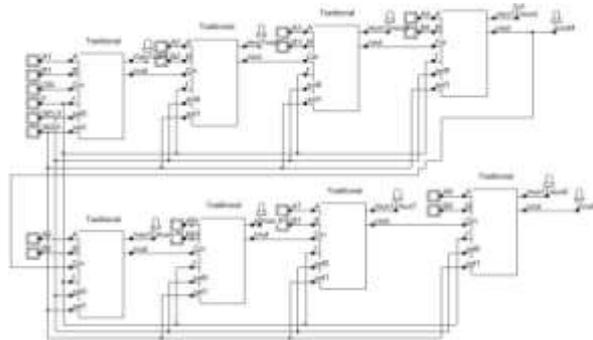


Figure 7. Traditional 8 bit ALU Architecture

For Optimized 8 bit ALU Architecture cascading of EIGHT 1 bit Optimized ALUs is done. The design of this Architecture is shown in Figure 8. The estimated power for this Optimized 8 bit ALU is 9.874 μ W.

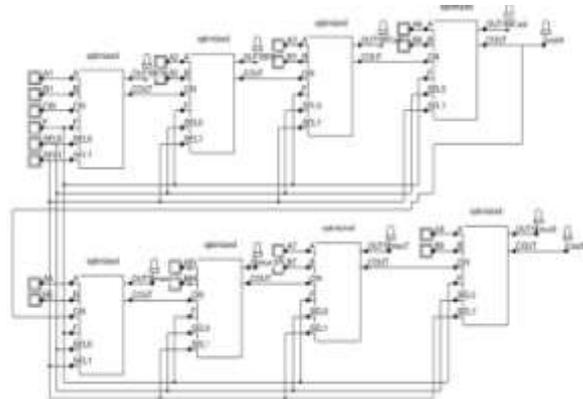


Figure 8. Optimized 8 bit ALU Architecture.

VII. Simulation Results

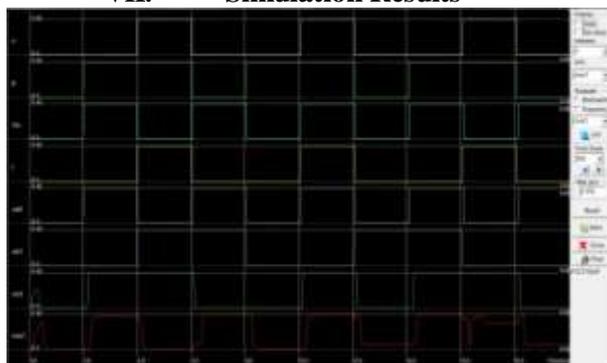


Figure 9. Waveform for Traditional 1 bit ALU

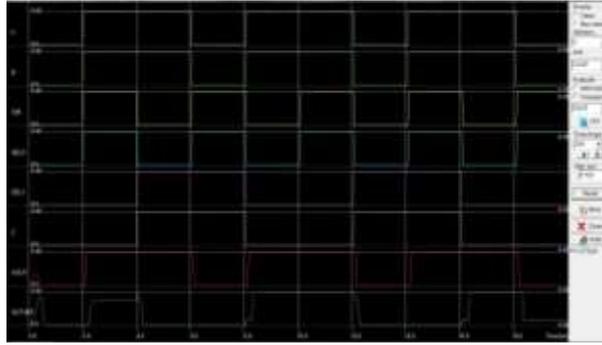


Figure 10. Waveform for Optimized 1 bit ALU

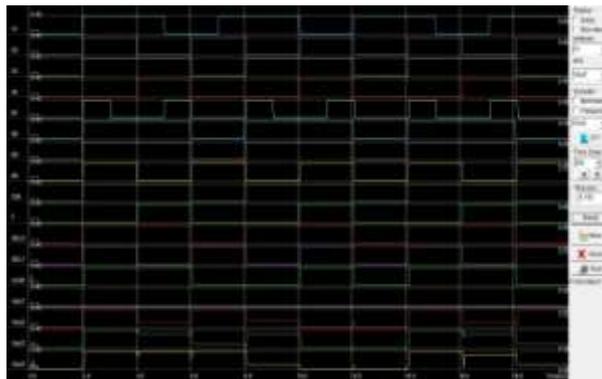


Figure 11. Waveform for Traditional 4 bit ALU

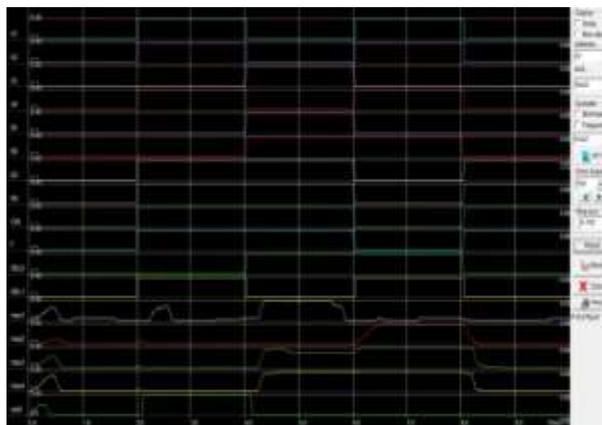


Figure 12. Waveform for Optimized 4 bit ALU

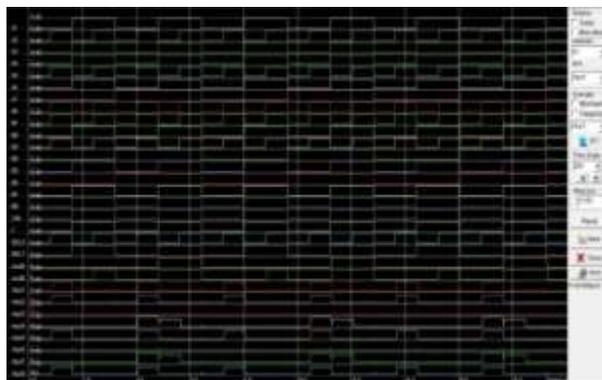


Figure 13. Waveform for Traditional 8 bit ALU

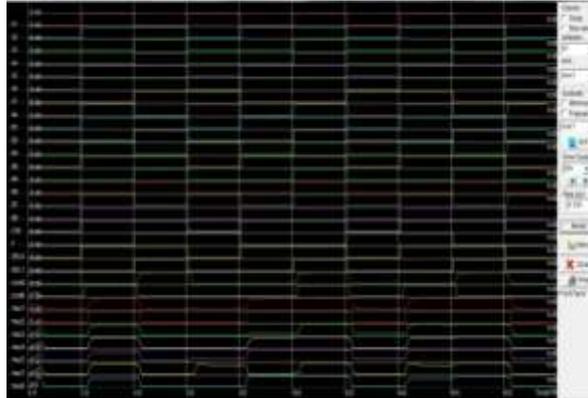


Figure 14. Waveform for Optimized 8 bit ALU

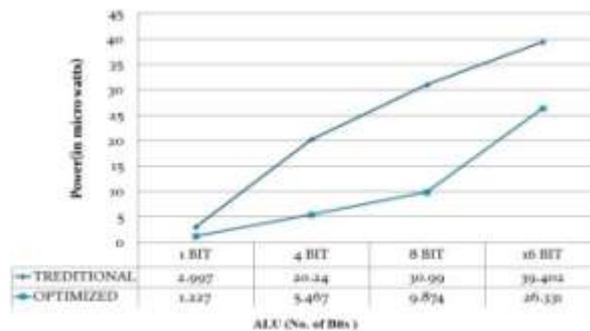


Figure 15. Power dissipation comparisons of traditional and optimized methods

VIII. Conclusion

This paper reviewed few key circuit design techniques and the corresponding implications on Power optimization. At first, designed the Traditional architecture of ALU and then optimized the Architecture using power gating technique to reduce the Power level. From this technique there is a significant reduction in power is observed. And it was a possible thing that the extension of this paper for 32 bit and 64 bit also.

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