

Systematic Analysis on Power Consumption in Conventional Cmos, Multiplexer Based and Hybrid Adder

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Abstract: *There has been a rapid increase in the popularity of portable and wireless electronic devices, like laptop computers, portable video players cellular phones, which rely on embedded digital signal processors. Since the desire is to design digital systems at best performance without power sacrifices, the need for high performance and low power multipliers is inevitable. Since multiplication is one of the most critical operations in many computational systems, Multipliers are in fact complex adder arrays. In this paper we performed a comparative analysis on power consumption in three different adders, each offering different advantages and having tradeoffs in terms of circuit complexity and power consumption. The 28 Transistor full adder is the pioneer CMOS traditional adder circuit. Which is the one which consume more power when compare to other two adder, the number of transistors required for conventional CMOS adder is 28. Recently, it has been proved that the multiplexer-based multiplier outperforms the modified Booth multiplier both in speed and power dissipation by 13% to 26%, due to small internal capacitance. After analyzing the performance characteristics of conventional multiplier types, it is observed that the one designed using multiplexer-based multiplication algorithm is more advantageous, especially when the size of the multiplied numbers is small. The number of transistors required for multiplexer based adder is 16. In order to achieve optimal power savings at smaller geometry sizes, we proposed a heuristic approach known as hybrid adder models. The hybrid adder models which consume low power among all three adder and the number of transistors required is 12. As an added advantage there will be no path from one voltage level (VDD) to the other (GND).The elimination of the direct path to the ground removes the short circuit power component for the adder module. This reduces the total energy consumed in the circuit and making it an energy efficient design. The SERF adder is not only energy efficient but also area efficient due to its low transistor count.*

Key words: Hybrid Adder, SERF Adder

I. Introduction

Conventional CMOS, allows very efficient implementation of simple gates (e.g. NAND/NOR) having only few transistors and nodes, and a small delay due to the single inversion level. The disadvantages lie in the large PMOS transistors resulting in high input capacitances and area requirements, and the weak output driving capability caused by series transistors. The conventional CMOS adder is designed in tanner s-edit and the circuit is simulated. The power consumed by the conventional CMOS adder is high when compare to multiplexer based adder and hybrid adder because the number of transistors is high which may lead to large dynamic power dissipation. Due to this the circuit will draw more power. In multiplexer based adder parallel combination of p-mos and n-mos are used. For designing a 4:1 multiplexer 16 transistors are required. In 4:1 mux four input data port, two selection lines and a single output. Similar to conventional CMOS adder the multiplexer based adder is designed in tanner s-edit and the circuit is simulated. The power consumed by multiplexer based adder is less than conventional CMOS adder but higher than hybrid adder. Finally the hybrid adder is designed in tanner s-edit and simulated for power calculation. The power consumed by each adder circuit is tabulated. The technology-independent low-power design strategy reduces power consumption through a refined design process. An obvious method to reduce power consumption is to reduce number of transistors in a circuit. Since the dynamic power dissipation in a VLSI is usually introduced by signal transitions in the circuit, many studies have also been carried out to minimize the average power dissipation by reducing switching activities of a given logic circuit. The minimization can be achieved at technology mapping phase and logic design phase. The major logic design methods for low power include. Techniques to eliminate glitches and to reduce switching activity in normal computation. In logic transformation we can either reduce the number of transistors and glitches or to transform the logic of the circuit.

II. Adder Modules

Adders are the fundamental building blocks in all the multiplier modules. Hence employing fast and efficient full adders plays a key role in the performance of the entire system. In the following section we briefly describe the adder modules used in our design. Since addition forms the basis of many binary operations, adder circuits are of great interest in digital design. In order to fulfill the various speed, power and area requirements of implementations, a wide variety of adder circuits have been proposed in literature. As the most frequently

used block in the overall design is full-adder, now we turn our attention to design an efficient full-adder, which operates with the possible power consumption.

A. Conventional CMOS Adder:

The 28 Transistor full adder is the pioneer CMOS traditional adder circuit. The schematic of this adder is shown in Figure 2.1. This adder cell is built using equal number of N-fet and P-fet transistors. The logic for the Complimentary MOS logic was realized using the Esq.(1) and (2)

$$Carry = AB + BC + AC \quad (1)$$

$$Sum = ABC + (A+B+C) \bar{C} \quad (2)$$

The first 12 transistors of the circuit produce the Carry and the remaining transistors produce the Sum outputs. Therefore the delay for computing Cout is added to the total propagation delay of the Sum output. The structure of this adder circuit is huge and thereby consumes large on-chip area.

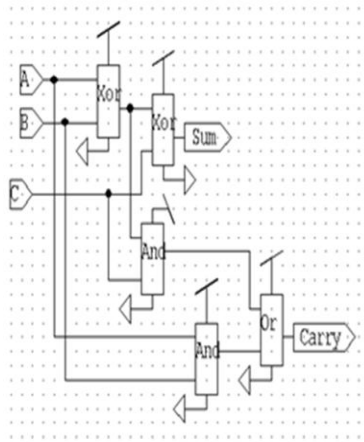


Figure 2.1 Transistor-level schematic of conventional CMOS 28-T one-bit full-adder

MY CONTRIBUTION IN THIS PAPER

B. Multiplexer Based Adder:

A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs the information to a single output line. Selection of a particular input line is controlled by a set of input variables, called selection or control bits. Generally, there are 2^n input lines and n control inputs, whose bit combinations determine which input is selected. Designing an n-to-1 MUX is possible by building a tree of 2-to-1 multiplexers. Considering that the delay of 2-to-1 MUX is smaller than that of an AND gate. Since we will use 4-to-1 MUX's in this design, creating a 2-to-1 MUX tree does not bring any drawback by means of speed or power dissipation. The schematics of the cascaded block are given in Fig. 2.2

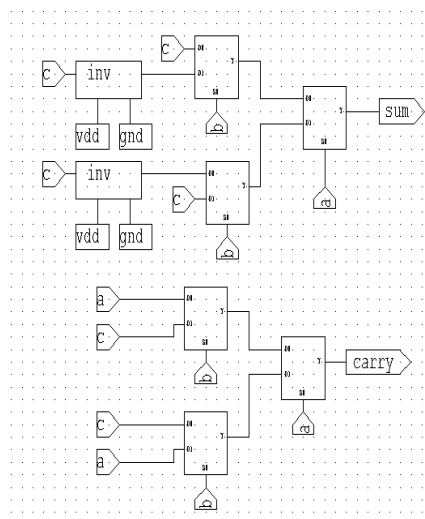


Figure 2.2 Multiplexer-based full adder

C. Hybrid Adder:

The transistor connection for a complementary switch or transmission gate consists of an n-mos and p-mos transistor connected in parallel with separate gate connection. The control signal is applied to the gate of n-mos, and its complement is applied to the gate of the p-mos device. The operation of transmission gate can be best explained by considering the characteristics of both the n-device and p-device as pass transistor individually. We will address this by treating the charging and discharging via transmission gate. n-mos pass transistor is good for transmission of '1' and poor for transmission of '0'. p-mos pass transistor is good for transmission of '0' and poor for transmission of '1'. The circuit of the 12 pass transistor adder is shown in figure 2.3 The capacitance at the outputs of the gates is also reduced as they are not loaded with inverter. If the signal degradation at the SUM and CARRY is significant for deep sub-micron circuits, drivers can be used to reduce the degradation. The driver will help in generating outputs with equal rise and fall times. This results in better performance regarding speed, low power dissipation and driving capabilities. The output voltage swing will be equal to the VDD, if a driver is used at the output.

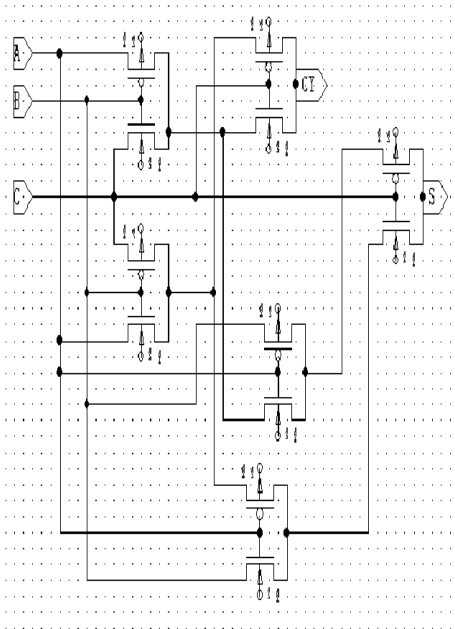


Figure 2.3 Hybrid 12 transistor adder

In this section, performance measurement of conventional CMOS 28-T one-bit full-adder, Multiplexer-based full adder and Hybrid 12 transistor adder are compared. These results were obtained from tanner s-edit simulator, the design constraints were the same for all the three adders. The results were obtained for the three circuits and the circuits were compared with respect to power consumed. For all the operand sizes, the multiplexer-based adder consumed considerably less energy compared to the conventional CMOS 28-T full-adder. The power consumed for hybrid 12 transistor adder is less as compared to multiplexer based adder and hence can be used where pass transistor logic is used.

TABLE I

ADDER	TRANSIS TORS	TOTAL AVERAGE POWER (mW)
Conventional CMOS Adder	28	0.564
Multiplexer based adder	16	0.337
Hybrid adder	12	0.20

III. Simulation Results

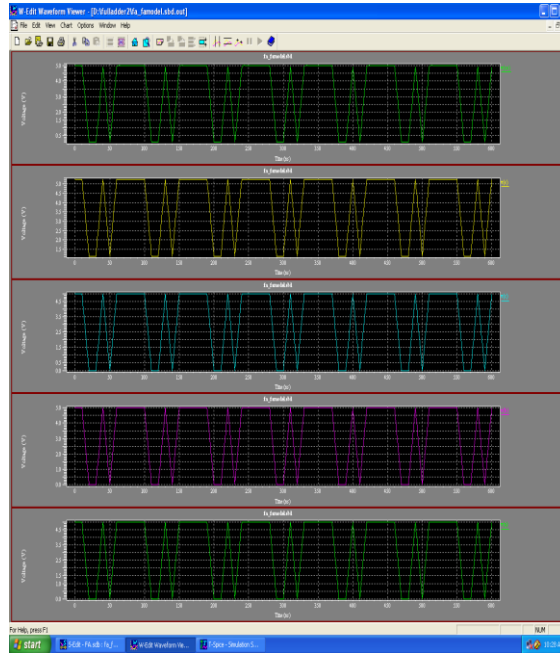


Fig 3.1 Waveform of conventional CMOS adder

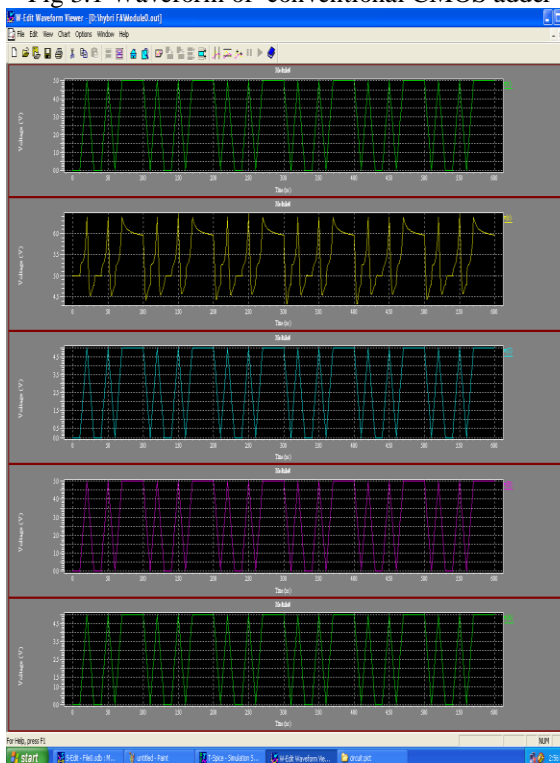


Fig 3.1 Waveform of Hybrid 12 transistor adder

IV. Conclusion

In this paper we have presented the power performance characteristics of three different adders and the transistor count is reduced. In all the adder configurations investigated, the hybrid adder exhibited better power performance compared to multiplexer based adder and conventional CMOS 28T adder based multipliers. Logic restructuring methods prove to be effective in reducing power consumption of the circuit. In the analysis conducted, only power was used in the cost function for optimization. The optimized circuit has the least power consumption of all compared circuits.

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