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A study to Design and comparison of Full Adder using Various Techniques

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Abstract: *Adders is widely used in applications such as digital signal processing (DSP) and microprocessors. In this paper Half adders are simulated and analyzed based on power dissipation, area and speed on 90nm technology using Microwind and Dsch tool. Half Adder is the basic building block in Parallel Feedback Carry Adder (PFCA).*

Keywords: *Full adder, Half adder, PFCA, VLSI.*

I. INTRODUCTION

With the extremely fast development of Very Large Scale Integrated (VLSI) technology, demand for widespread use of high performance portable integrated circuit (IC) devices such as MP3, PDA, mobile phones is increasing rapidly. Most of the VLSI applications, such as digital signal processing, image and video processing and microprocessors, extensively use arithmetic operations. Therefore, the integrated circuit performances highly depend on how the arithmetic modules are implemented. Since addition between two binaries is the most fundamental operation in arithmetic logic unit, a full adder (FA) is the core element of complex arithmetic circuits like subtraction, multiplication, division, exponentiation, etc. Consequently, enhancing performance of full adder is crucial to improve the performance of overall modules.

VLSI system with high speed, low power dissipation and Compact implementation since they are the main factors which directly affect performance of an entire system. Therefore, various full adder cell topologies were designed and developed by electronics designers in order to achieve the best performances. However, currently, VLSI designers faces two conflicting design challenges: first is to discover high performance design and implementation techniques that can meet the stringent speed constraints; second is to consider low-power design approaches to prolong the operating time of devices . Since power and speed are usually trade-off, it is necessary for the designer to consider and choose the best design which meets a specific requirement and application

Full Adder is designed using Half Adders. In this paper half adder is designed taking into consideration that Parallel feedback carry adder (PFCA) is based on the unit of half adder. So in this paper Half adder is designed using NAND Gates only and using EX-OR and AND Gates in microwind using 90nm technology . one Full Adder consists of two HAs and one OR gate, while one HA consists of one AND gate and XOR gate . Half Adder has carry-out bit but no carry-in bit, as a result HA is not a basic unit of existing adders but only a component of it.

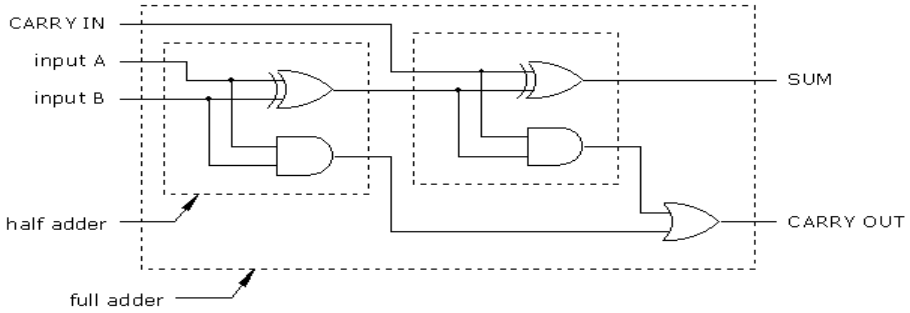

Fig.1 Full Adder using Half Adder

II. PFCA THEORY

2.1 Basic Unit of Adder: Let A and B be two *n*-bit binary numbers as follows

$$A = A_{n-1}A_{n-2}\ldots\ldots A_i\ldots\ldots A_2A_1A_0$$
$$B = B_{n-1}B_{n-2}\ldots\ldots B_i\ldots\ldots B_2B_1B_0 \quad (1)$$

Where A_i and B_i are the i-th bit of A and B. Their sum is

$$S = A+B = S_{n-1}\ldots\ldots S_i\ldots\ldots S_2S_1S_0 \quad (2)$$

and

$$S_i = A_i \oplus B_i \oplus C_i$$
$$C_i = A_iB_i+(A_i \oplus B_i)\, C_{i-1} \quad (3)$$

Where $C_{i-1}= 0$. This is called FA (Full Adder), which is the basic unit of *n*-bit adders.

All existing various adders are based on full adder and *n*-bit addition at least needs *n* FAs. A good example for this is that *n*-bit RCA needs *n* FAs with the smallest area and the most computation time. From the perspective of logic gates, one FA consists of two HAs and one OR gate, while one HA consists of one AND gate and XOR gate . HA has carry-out bit but no carry-in bit, as a result HA is not a basic unit of existing adders but only a component of it from (2) and (3).

2.2 Basic Structure of PFCA

In order to implement *n*-bit adder based on HA. Let *A* and *B* be two *n*-bit binary numbers, the superscript be the time variable, the subscript be the place in the binary number.

Then A^k,B^K is the value of A and B after k times iterative operations. That is:

$$A^K = A^k_{n-1}\ldots A^k_i\ldots\ldots A^k_2A^k_1A^k_0 \text{ , k = 0,1,2...} \quad (4)$$
$$B^K = B^k_{n-1}\ldots B^k_i\ldots\ldots B^k_2B^k_1B^k_0 \text{ , k = 0,1,2...} \quad (5)$$

Obviously, the initial value is

$$A = A^0_{n-1}\ldots A^0_i\ldots A^0_1A^0_0$$
$$B = B^0_{n-1}\ldots B^0_i\ldots B^0_1B^0_0$$

Let S_i^k and C_i^k be the intermediate variable of iteration they are as follows:

$$S_i^k = A_i^{k-1} \oplus B_i^{k-1}, \text{,i = 0,1,2....,n; k = 1,2 ...} \quad (6)$$
$$C_i^k = A_i^{k-1} \cdot B_i^{k-1}, \text{,i = 0,1,2.....,n; k = 1,2...} \quad (7)$$

Then they constitute one half adder.

A feedback mechanism is brought in, let

$$A_i^k = S_i^k, \quad \text{i = 0,1,2....n ; k = 1,2...} \quad (8)$$
$$B_i^k = C_{i-1}^k, \text{ i = 0,1,2,....n ; k = 1,2,...} \quad (9)$$

Where $C_{i-1}^k \equiv 0$,they constitute a new group of A^k and B^k, and they return back to (4) and (5), then operation repeats from(4) and (5) to (8) and (9)

Theorem 1. If $C_i^k \equiv 0$, i = 0,1,2....n-1, then the sum S of A and B satisfies:

$$S = A+B = A^k \quad (10)$$

The theorem can be easily proved. Equation (9) means that a new addend can be got through (7) which has got its previous carry-out-bit and (8) means that another new addend can be got through (6) that has got its sum-bit in each iterative round. Then the final sum will be got through many rounds of iteration until the carry-bits are all zero. Two XOR operations are required to acquire the sum in (3). Thus, (6) to (9) constitute a more basic unit of adder. As a result, an ideal *n*-bit PFCA can be drawn out by cascading *n* units of this kind and its basic structure is shown in Fig.2. The area asymptotic requirement of PFCA is *O* (*n*) and all the HAs will complete their operations at each chock, then the results are feedback to the inputs for next operations. Therefore, PFCA is a parallel adder with feedback. Compared to all existing adders, PFCA has less computation time and smaller area and its area-time efficiency can be increased 4 times because of the two advantages of PFCA:

- Parallel mode, which speeds up the circuits of adder;
- Feedback mode, which increases the times of the basic units used.

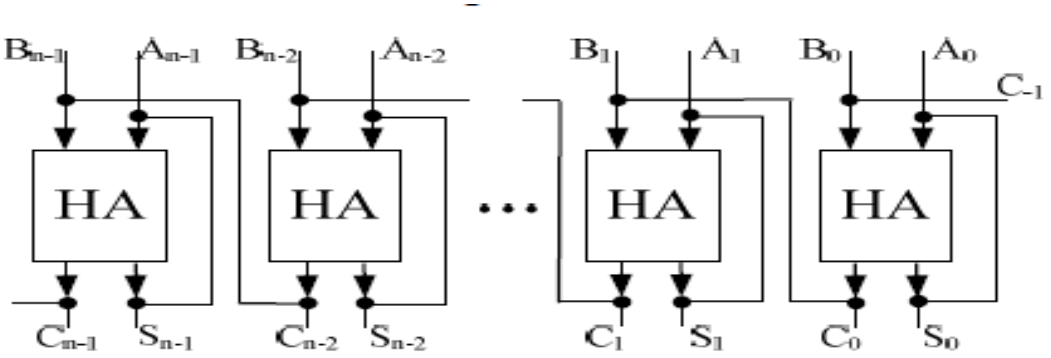

Fig.2 The basic structure of PFCA based on HA

2.3 ***Problems in the Hardware Implementation of PFCA***

PFCA has substantial potential advantages in area and speed in theory, but there are some technological problems to resolve in the implementation of hardware circuits:

- The feedback signals must be separated from the input signals.
- As an asynchronous circuit, PFCA requires a start and a finish signals.
- The difference between the delays from port *A* or *B* to port *S* and to port *C* will be enlarged afterseveral iterations and thus it lead to failure of PFCA.
- The attenuation of carry-out signal will shorten the transmitted distance.

III. THE IMPLEMENTATION OF PFCA IN CMOS GATES

To verify the possibility of hardware implementation of PFCA, a PFCA based on CMOS gates is designed. The result shows that the theory of PFCA based on HA is feasible. Compared to existing adders, PFCA has some advantages in area and speed, especially when *n* is larger. Three laws must be conformed in the design of PFCA:

1) The area and computation time of the imported circuits must be as small as possible.
2) If it requires some controlling ports, then the number of them must be small enough.
3) To ensure the delays of port *C* and port *S* to be almost equal, some changes must be taken place in the HA, at the same time, the whole delay from input to output in a HA should not increase too much.

3.1 THE IMPLEMENTATION OF PFCA IN CMOS GATES

A structure of 4-bit PFCA is given in Fig.3 . Then PFCA of any even bits can be cascaded by the unit of two 2-MUX2- 1s, two HAs, one drive circuit and some OR gates. The controlling port *Start* and two MUX2-1s can resolve the first and second problem in the previous section, which gives PFCA an enable signal to choose the input signals or the feedback signals. The next problem is resolved by designing a mechanism to test all the carry-out bits. If they are all 0, then an active low signal *Finish* is given. The method to resolve the 4th problem is that, the outputs of *S* and *C* must have almost the same computation time. A drive circuit is provided here to enhance the carry-out signal. Simulation result shows that the drive circuit is added in every two bit and then any length of PFCA can be reached.

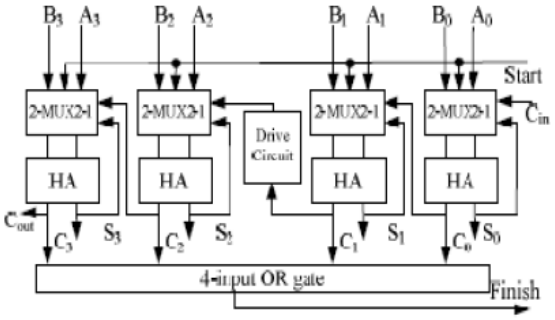

Fig.3 The structure of 4-bit PFCA

Half adder has two binary inputs and two outputs sum and carry. Half adder using NAND gates and using EX-or and AND gates is designed in microwind .

Logic Expression of Half Adder

$S = A \oplus B$

$C = AB$

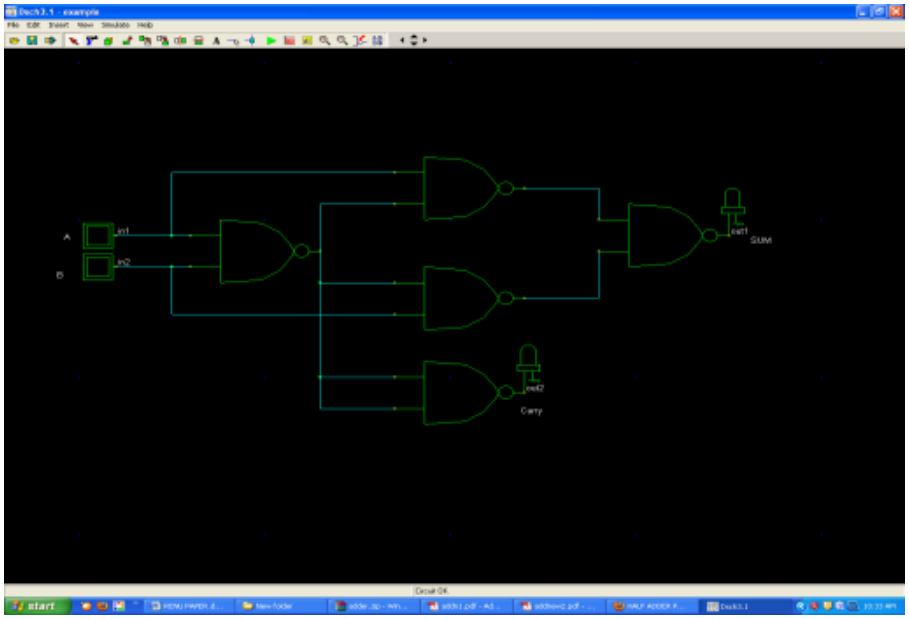

Fig. 4. Half Adder using NAND Gates

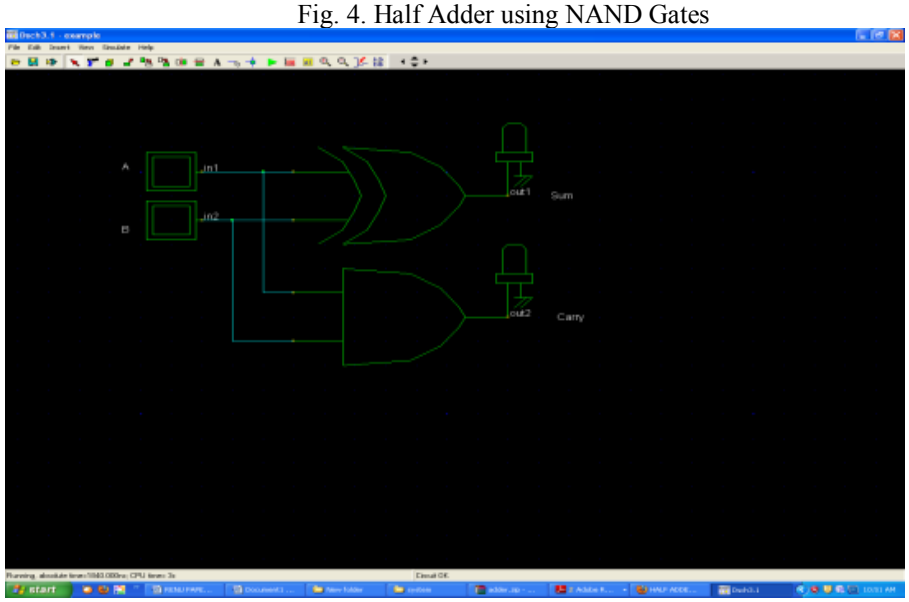

Fig. 5. Half Adder using EX-OR and AND Gate

IV. RESULT AND DISCUSSION

TABLE I: Single bit Half Adder

Parameter	NAND Gates	EX-OR & AND
No.of transistors	10 Nmos 10 Pmos	6Nmos 6Pmos
Simulation time	4 sec	3sec
size	8*9µm	6*8µm
Memory used	2.2%	1.5%

TABLE II: Using NAND Gates

Vdd(V)	P(mw)
.2	.001
.4	.016
.6	.027
.8	.039
1	.054
1.2	.072

TABLE III: Using EX-OR $ and AND Gates

Vdd(V)	P(mw)
.2	.002
.4	.004
.6	.010
.8	.020
1	.032
1.2	.059

V. CONCLUSION

This paper presents that Half adder using EX-OR AND and Gates consumes less space and power than using NAND Gates only.

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