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# Design of an Adaptive Equalizer Using Lms Algorithm

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***Abstract:*** *Equalizers are used for compensation of amplitude and phase dispersion which results in the interference of the transmitted signals with one another. In this paper design of an adaptive equalizer has bee presented using least mean square algorithm. The FPGA Implementation of the adaptive equalizer has also been presented.*

***Key Words:*** *Adaptive Equalization, Field Programmable Gate Array, Fractionally Spaced Equalizer, Least Mean square.*

## I. Introduction

Inter-symbol interference imposes the main obstacles to achieving increased digital transmission rates with the required accuracy. ISI problem is resolved by channel equalization [1] in which the aim is to construct an equalizer such that the impulse response of the channel/equalizer combination is as close to $z^{-\Delta}$ as possible, where $\Delta$ is a delay. Frequently the channel parameters are not known in advance and moreover they may vary with time, in some applications significantly. Hence, it is necessary to use the adaptive equalizers, which provide the means of tracking the channel characteristics. The following Fig.1 shows a diagram of a channel equalization system.

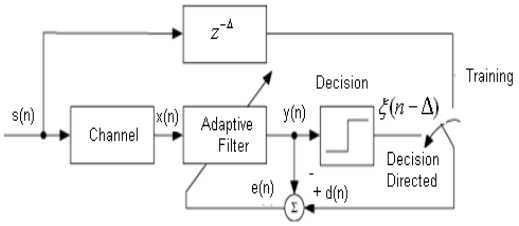


**Fig.1 Digital transmission system using channel equalization**

In the Fig. 1, s(n) is the signal that transmit through the communication channel, and x(n) is the distorted output signal. To compensate for the signal distortion, the adaptive channel equalization system completes using training and decision directed modes [11].Here, Adaptive filter plays an important role. The structure of the adaptive filter as **[2]** shown in Fig.2. To start the discussion of the block diagram takes the following assumptions:

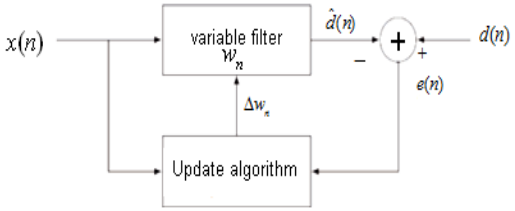


**Fig.2 Adaptive filter**

The input signal is the sum of a desired signal *d* (*n*) and interfering noise v (n)

$$x(n) = d(n) + v(n) \quad (1)$$

The variable filter has a Finite Impulse Response (FIR) structure. For such structures the impulse response is equal to the filter coefficients. The coefficients for a filter of order *p* are defined as

$$w_n = [w_n(0), \quad w_n(1), \quad ..., \quad w_n(p)]^T \quad (2)$$

the error signal or cost function is the difference between the desired and the estimated signal

$$e(n) = d(n) - \hat{d}(n) \quad (3)$$

The variable filter estimates the desired signal by convolving the input signal with the impulse response. In vector notation this is expressed $\hat{d}(n) = w_n * x(n)$ (4)

Where

$$x(n) = [x(n), \quad x(n-1), \quad ..., \quad x(n-p)]^T \qquad (.5)$$

is an input signal vector. Moreover, the variable filter updates the filter coefficients at every time instant

$$w_{n+1} = w_n + \Delta w_n \qquad (6)$$

Where $\Delta w_n$ is a correction factor for the filter coefficients .The adaptive algorithm generates this correction factor based on the input and error signals. This paper presents the comparison of some of the channel equalization techniques. The paper also presents FPGA implementation of Fractionally Spaced Equalizer.

## II. Equalization Methods

Different kinds of Equalizer are available in the text like Fractionally Spaced Equalizer**,** Blind Equalization**,** Decision-Feedback Equalization**,** Linear Phase Equalizer, T-Shaped Equalizer [4]**,** Dual Mode Equalizer [12] and Symbol Spaced Equalizer [4]. A Symbol-Spaced linear equalizer consists of a tapped delay line that stores samples from the input signal. Once per symbol period, the equalizer outputs a weighted sum of the values in the delay line and updates the weights to prepare for the next symbol period.

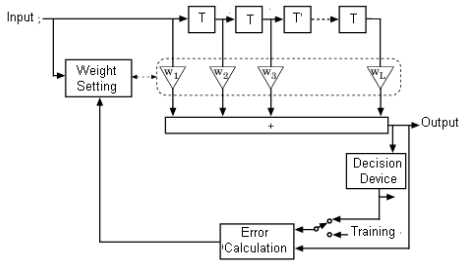


**Fig.3 Symbol Spaced Adaptive Equalizer**

This class of equalizer is called *symbol-spaced* because the sample rates of the input and output are equal. In typical applications, the equalizer begins in training mode to gather information about the channel, and later switches to decision-directed mode [1] [3]. Fig.3 shows a schematic of a symbol-spaced linear equalizer with N weights, where the symbol period is T.The basic limitation of a linear equalizer, such as transversal filter, is the poor perform on the channel having spectral nulls. A decision feedback equalizer (DFE) is a nonlinear equalizer that uses previous detector decision to eliminate the ISI on pulses that are currently being demodulated. In other words, the distortion on a current pulse that was caused by previous pulses is subtracted. Fig.4 shows a simplified block diagram of a DFE where the forward filter and the feedback filter can each be a linear filter, such as transversal filter. The nonlinearity of the DFE stems from the nonlinear characteristic of the detector that provides an input to the feedback filter.

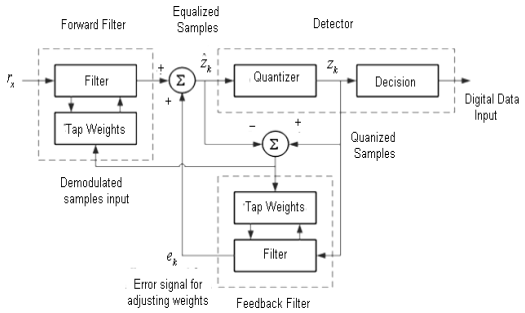


**Fig.4 Decision Feedback Equalizer**

The basic idea of a DFE (Vladimir D. Orlic and M. Lutovac ,2009) [10] is that if the values of the symbols previously appropriate weighting. The forward and feedback tap weights can be adjusted simultaneously to fulfil a criterion such as minimizing the MSE. The DFE structure is particularly useful for equalization of channels with severe amplitude distortion, and is also less sensitive to sampling phase offset. The improved performance comes about since the addition of the feedback filter allows more freedom in the selection of feed forward coefficients. The exact inverse of the channel response need not be synthesized in the feed forward filter, therefore excessive noise enhancement is avoided and sensitivity to sampler phase is decreased. The advantage of a DFE implementation is the feedback filter, which is additionally working to remove ISI, operates on noiseless quantized levels, and thus its output is free of channel noise. One drawback to the DFE structure surfaces when an incorrect decision is applied to the feedback filter. The DFE output reflects

this error during the next few symbols as the incorrect decision propagates through the feedback filter. Under this condition, there is a greater likelihood for more incorrect decisions following the first one, producing a condition known as error propagation. On most channels of interest the error rate is low enough that the overall performance degradation is slight.Blind equalization of the transmission channel has drawn achieving equalization without the need of transmitting a training signal. Blind equalization algorithms that have been proposed are the constant modulus algorithm (CMA) and multimodal's algorithm (MMA). This reduces the mean-squared error (MSE) to acceptable levels. Without the aid of training sequences, a blind equalization is used as an adaptive equalization in communication systems. In the blind equalization algorithm, the output of the equalizer is quantized and the quantized output is used to update the coefficients of the equalizer. Then, for the complex signal case, an advanced algorithm was presented in. However, the convergence property of this algorithm is relatively poor [12]. In an effort to overcome the limitations of decision directed equalization, the desired signal is estimated at the receiver using a statistical measure based on a priori symbol properties, this technique is referred to as blind equalization [5]. Blind equalization is shown in Fig. 5

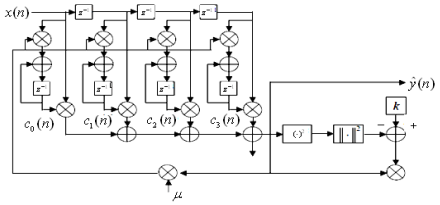


**Fig.5 Blind Equalization**

In the Blind Error is selected as the basis for the filter coefficient update. In general, blind equalization directs the coefficient adaptation process towards the optimal filter parameters even when the initial error rate is large. For best results the error calculation is switched to decision directed method after an initial period of equalization, call this the shift blind method. Referring to, the Reference Selector selects the Decision Device Output as the input to the error calculation and the Error Selector selects the Standard Error as the basis for the filter coefficient update. A Fractionally Spaced Adaptive Equalizer ([6]is a linear equalizer that is similar to a symbol-spaced linear equalizer. By contrast, however, a Fractionally Spaced Equalizer receives say K input samples before it produces one output sample and updates the weights, where K is an integer. In many applications, K is 2. The output sample rate is 1/T, while the input sample rate is K/T. The weight-updating occurs at the output rate, which is the slower rate. Fig.6 shows the Fractionally Spaced Adaptive Equalizer.

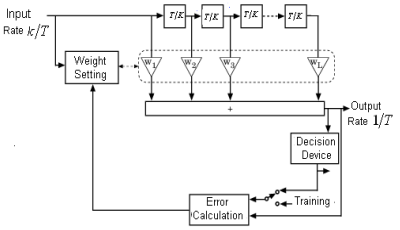


**Fig.6 Fractionally Spaced Adaptive Equalizer**

Sometimes the input to the equalizer is oversampled such that the sample interval is shorter than the symbol interval and the resulting equalizer is said to be Fractionally Spaced Adaptive Equalizer. Equalizer Taps are spaced closer than the reciprocal of symbol rate. Advantages of FSE are it has ability to be not affected by aliasing problem, shows fast convergence and sample rate is less the symbol rate [7].

More recently, Fractionally Spaced Adaptive Equalizers (FSE's) have assumed an increasing presence, especially in the area of voice band data transmission. This technological shift is based upon at least two factors: first, the performance superiority of FSE's relative to that of Conventional equalizer and second, the availability of variants on the conventional stochastic gradient algorithm that mitigate coefficient drift during decision-directed operation. With regard to the former, many studies have clarified the performance attributes of FSE's. It is known, for example, that Conventional equalizer operates on an aliased spectrum of the received signal, thus rendering performance acutely sensitive to the receiver timing phase. In contrast, FSE's are far less sensitive to timing phase provided the delay line tap spacing $T'$ is less than or equal to the reciprocal of twice the highest frequency component in the transmitted signal. As a result fractional equalizers compensate for timing phase offset or channel delay within the limits of their finite tapped delay lines (TDL).

As an additional attribute, FSE's theoretically approach the properties of an optimal receiver. Operating in the presence of Gaussian noise, the mean-square distortion between the estimated binary data and actual sampler output is minimized, as is the average error probability**.** The theoretical performance of infinite fractional equalizers can also be shown to be independent of channel phase or timing phase. To the extent that FSE's can operate on the unaliased input spectrum and thus permit operation with Nyquist channel spectra up

to the baud frequency, they can also be used to minimize the effects of timing jitter relative to that of Synchronous equalizer, thereby offering more robust operation**.**

FSE performance for voice band channels has been extensively studied. In simulations reported by (Gitlin and Weinstein, 1981) [8], 48 tap, "$T/2$" $(T')$ fractional equalizers were compared to 24 tap Conventional equalizer in a 9.6 kb/s 4-level QAM (2.4 kbaud) system and were found to offer superior performance. In the earlier work of (Qureshi and Fomey, 1985) [9], simulations for somewhat different channels and system characteristics showed FSE's almost as good as or better than Conventional equalizer counterparts, although the numbers of taps in each equalizer were the same.In spite of their advantages, only lately have FSE's been seriously considered for high-speed digital radio where they can improve the effects of dispersion caused by not normal propagation. The tardy application is probably due to the satisfactory operation of Synchronous equalizer for low-level QAM systems and the complexity of implementing the least mean-square (LMS) algorithm. It should be mentioned that in spite of the widely cited advantages of the linear LMS algorithm relative to zero-forcing (ZF), the latter is almost universally used in digital radio systems.

## III. Fpga Implementation Of The Equalizer

This section presents the Virtex-II Field Programmable Gate Array (FPGA) implementations for proposed Fractionally Spaced Adaptive Equalizer (FSE) using Xilinx Integrated System Environment (ISE 9.2i) software for resource calculation.Fig.7 shows a RTL schematic diagram of FSE. In this design, register transfer level (RTL) is a level of abstraction used in describing the operation of a synchronous digital circuit.


**Fig.7 Top level RTL Schematic diagram**

In RTL design, a circuit's behaviour is defined in terms of the flow of signals (or transfer of data) between hardware registers, and the logical operations performed on those signals. Register transfer level abstraction is used in hardware description languages (HDLs) like Verilog and VHDL to create high-level representations of a circuit, from which lower-level representations and ultimately actual wiring can be derived.

Using an EDA tool for synthesis, VHDL code of the circuit can usually be directly translated to an equivalent hardware implementation file for an FPGA. The synthesis tool also performs logic optimization. Here, Fig.8 shows an internal structure of RTL Schematic diagram.

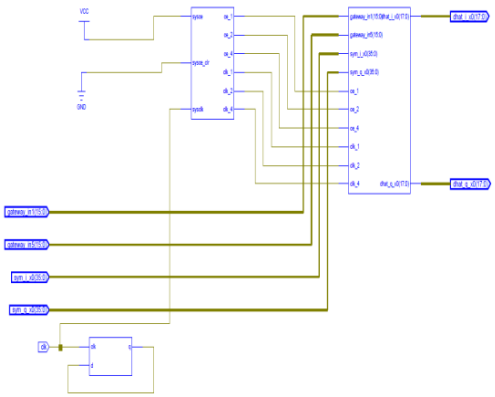

**Fig.8 Internal Structure of RTL Schematic diagram**

After testing model on simulation, the simulation design is compiled to ISE file before generating the programming file, bit file. Table 1 show the resources used in this model which just takes a small part in Xilinx Virtex-II Kit.

**Table 1: Device Utilization Summary of Xilinx FPGA**

| **Logic Utilization** | **Used** | **Available** | **Utilization** |
|---|---|---|---|
| Number of Slice Flip Flops | 2,232 | 67,584 | 3% |
| Number of 4 input LUTs | 1,070 | 67,584 | 1% |
| **Logic Distribution** | | | |
| Number of occupied Slices | 1,746 | 33,792 | 5% |
| **Total Number of 4 input LUTs** | 1,981 | 67,584 | **2%** |

Table 1 shows that how much logic resource of FPGA is used to implement the whole system, and as shown in the table utilization of every item to implement the system is almost below 40%. It means that one can select a smaller and cheaper FPGA to further reduce the cost, or one can also build up an Intellectual Properties (IP) into FPGA to implement more sophisticated control algorithm.

## IV. Conclusion

Fractional Spaced Adaptive Equalizer has better performance in terms of bit error rate and fast convergence. The fractionally spaced equalizer has been implemented on a Xilinx FPGA device and FPGA resources used by the design have been presented.

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