IOSR Journal of Electronics and Communication Engineering (IOSRJECE)
ISSN : 2278-2834 Volume 2, Issue 5 (Sep-Oct 2012), PP 12-17
www.iosrjournals.org

High Speed Data Acquisition System with Ethernet Interface

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Abstract: *This paper introduces a high speed data acquisition system based on a field programmable gate array (FPGA) . The aim is to develop a "distributed" data acquisition interface. The development of instruments such as personal computers and engineering workstations based on "standard" platforms is the motivation behind this effort. Using standard platforms as the controlling unit allows independence in hardware from a particular vendor and hardware platform. The distributed approach also has advantages from a functional point of view: acquisition resources become available to multiple instruments; the acquisition front-end can be physically remote from the rest of the instrument. High speed data acquisition system transmits data faster to a remote computer system through Ethernet interface. The data is acquired through 16 analog input channels. The input data commands are multiplexed and digitized and then the data is stored in 1K buffer for each input channel. Then the input data is filtered using FIR filters implemented using processor. The filtering is used to reduce the band width of the input data The main control unit in this design is the 16 bit processor implemented in the FPGA. This 16 bit processor is used to set up and initialize the data source and the Ethernet controller, as well as control the flow of data from the memory element to the NIC Using this processor we can initialize and control the different configuration registers in the Ethernet controller in a easy manner. Then these data packets are send to the remote PC through the Ethernet interface. The main advantages of the using FPGA as standard platform are its flexibility, low power consumption, short design duration, fast time to market, programmability and high density. The main advantages of using Ethernet controller AX88796 over others are its non PCI interface, the presence of embedded SRAM where transmit and reception buffers are located and high-performance SRAM-like interface. The paper introduces the implementation of the distributed data acquisition using FPGA by VHDL. The main advantages of this system are high accuracy, high speed, real time monitoring.*

Key words: *Field Programmable Gate Array(FPGA), Data Acquisition System (DAS), Ethernet.*

I. Introduction

Data Acquisition system is an embedded system which has wide application in real time monitoring, communication, data transmission ,image data acquisition ,radar, telemetry, remote sensing etc[1]. The main process involved in data acquisition system is to convert analog signal to digital signal that can be processed by various systems and then sent to the computer for real time monitoring. Its accuracy, reliability and versatility make it prominent to play a leading role in modern electronic instruments.

Data acquisition involves collection of data for the purpose of analysis or documentation of some process. Data acquisition using electronic equipments increases the accuracy and reliability. Analog to digital converter is the main part of the data acquisition system as it determines the resolution which in turn fixes the speed of the data acquisition system. The different types of data acquisition system that we are using nowadays are serial communication data acquisition system, Universal Serial Bus (USB) data acquisition system .data acquisition system plug in board, parallel port data acquisition system. RS232 and RS485 are used for serial communication system. Transmission distance is the main limitation in all this communication .RS485 can support only up to a distance of 5000 feet. Personnel Computer can be connected to the data acquisition using parallel port. However the distance between the computer and the data acquisition device is limited to a few feet. USB is the new technology in the field of data acquisition system that supports higher bandwidth than any other competent in this field[2]. The main advantage of using computer plug in board is its higher speed as it is directly connected to the computer. The fourth type of data acquisition system parallel port technology has the advantage of higher sampling rate.

Earlier we used data acquisition system based on microcontroller unit[3]. The data that may be in analog or digital form are read, filtered, processed and send to different displaying devices using proper interfaces. In microcontroller based systems the processing is done using the microcontroller unit. The main advantages of this system are its low cost, low power consumption and smaller size. This system has got several drawbacks such as low processing speed and poor usage of memory resources. The embedded field now uses Advanced RISC Machines (ARM) , DSP chips and FPGA as the three main controlling unit in the data acquisition system. The three processors have their own advantage in their application field. ARM has a formidable transaction management function; it is mainly used in embedded control, multimedia, mobile

applications and other areas[4]. The main advantages of DSP are its strong data processing capability and high operating speed. DSP are mainly used to greatly reduce the control system computation and band width requirement[5].

Flexibility is the most favorable feature of FPGA's. The development and verification of a system can be done using FPGA. The most important uses of FPGA as a processor are its ability to implement glue logic, signal processing and for developing a system using System On Chip (SoC)[6]. Small internal delay and high clock frequency helps it to realize the complex circuits using simple control logic and accurate timing. Parallel processing structure of FPGA is highly advantageous for implementing complex algorithms. The FPGA is more and more popular and widely used in various applications for its low power consumption, short design cycle, fast time-to-market, programmability and high density. Now a day FPGA is fully equipped with hard and soft core processors. This helps in the development of low cost embedded systems design and development. Gigabit Ethernet interface is used to exchange the data between acquisition board and PC in real time remote transmissions.

The advantage of FPGA based Ethernet connections is, that one hardware platform is capable of supporting all industrial Real-Time Ethernet protocols. Only the required FPGA configuration and software has to be uploaded for the selected protocol. This can be made during the production phase or even later by using the device CPU. As a result, future Ethernet-based protocol standards can be supported anytime without changing the hardware. As another advantage, the device manufacturers are not bound to one, possibly smaller vendor. Of course, there is almost no second source available when choosing a special chip from a specific vendor, but with a reasonable effort the manufacturer can switch to another FPGA vendor, since VHDL and Verilog are standard FPGA programming languages.

II. Data Acquisition System

The real world Physical parameters which are in analog form are converted into artificial world digital control and computation parameters using data acquisition system. Digital systems are accurate, implemented using simple logic and low development cost. The analog to digital converters and digital to analog converters together known as the data converters. Data converters are used include data telemetry systems, pulse code modulated communications, automatic test systems, computer display systems, video signal processing systems, data logging systems, and sampled data control systems.

The main components involved in the data acquisition system are transducers, amplifiers, filters, nonlinear analog functions, analog multiplexers, sample-holds.

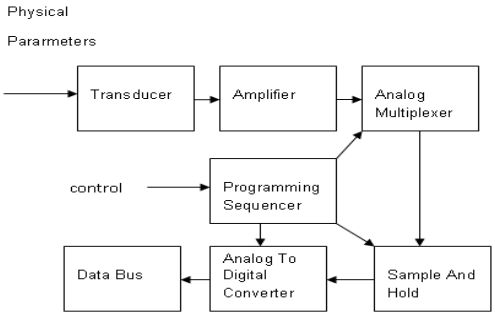

Figure 1: Data Acquisition System

The analog quantities such as temperature, pressure, flow, acceleration, and position are the input to the system .Transducer converts the physical parameter into electrical signal; electronic circuits performs further processing . Next, an amplifier boosts the amplitude of the transducer output signal to a useful level for further processing. Transducer outputs may be microvolt or millivolt level signals, which are then amplified to 1 to 10V levels. Furthermore, the transducer output may be a high impedance signal, a differential signal with common-mode noise, a current output, a signal superimposed on a high voltage, or a combination of these. The amplifier, in order to convert such signals into a high-level voltage, may be one of several specialized types. The amplifier is frequently followed by a low-pass active filter that reduces high-frequency signal components, unwanted electrical interference noise, or electronic noise from the signal. The amplifier is sometimes also followed by a special nonlinear analog function circuit that performs a nonlinear operation on the high-level signal. Such operations include squaring, multiplication, division, rms conversion, log conversion, or linearization. The processed analog signal next goes to an analog multiplexer, which switches sequentially between a number of different analog input channels. Each input is in turn connected to the output of the multiplexer for a specified period of time by the multiplexer switch. During this connection time, a sample-hold circuit acquires the signal voltage and then holds its value while an A/D converter converts the value into digital form. The resultant digital word goes to a computer data bus or to the input of a digital circuit. Thus the analog

multiplexer, together with the sample hold, time shares the A/D converter with a number of analog input channels. The timing and control of the complete DAS is done by a digital circuit called a *programmer sequencer*, which in turn is under the control of the computer. In some cases, the computer itself may control the entire DAS. While this is perhaps the most commonly used DAS configuration, there are alternative ones. Instead of multiplexing high-level signals, low-level multiplexing is sometimes used with the amplifier following the multiplexer. In such cases, just one amplifier is required, but its gain may have to be changed from one channel to the next during multiplexing. Another method is to amplify and convert the signal into digital form at the transducer location and send the digital information in serial form to the computer. Here, the digital data must be converted to parallel form and then multiplexed onto the computer data bus.

III. Embedded Processor in FPGA

The most flexible components in the embedded system design are processors and the flexibility is achieved through the standardization of hardware and software technology. The most commonly implemented processors are the Reduced Instruction Set Computer type. Every conceivable type of embedded system uses RISC architecture and high level programming language. The flexibility of SRAM base FPGA can be increased by embedding processors within the FPGA. The different types of processors implemented in FPGA are soft, hard and firm core. Potential benefits associated with implementing a processor within an FPGA include reduced obsolescence, increased design content ownership, and fewer board-level components. Some of the factors influencing an embedded processor implementation include clear and concrete system requirements, good design methodology, efficient co-design , and proper design partitioning. There are multiple hardware and software trade-offs that must be completed to implement a processor within an FPGA. Some design considerations include selection of the processor core, selection of the peripherals blocks and IP, processor memory architecture and design element interconnection. Some software design considerations include informed coding, selection and use of a real-time operating system (RTOS), and device driver development. Both software and hardware tools are critical factors, and every effort should be taken to select the best tools available.

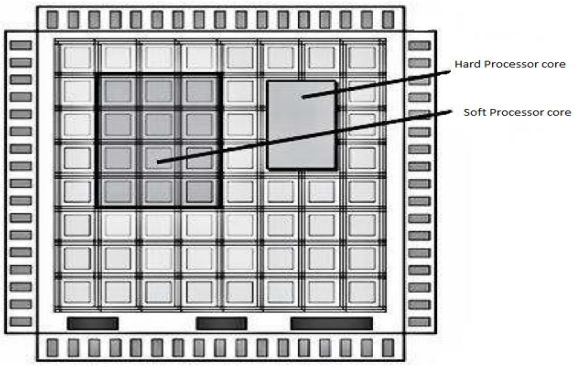

Figure 2: An example of FPGA hard and soft processor.

Soft cores are processor implementations in an HDL language without extensive optimization for the target architecture. Soft cores typically have lower performance and are less efficient in terms of resource utilization. Firm cores are also HDL implementations but have been optimized for a target FPGA architecture. Figure 2 above shows a hard and soft processor example.

IV. Design

The design of the FPGA is detailed in this section. The Figure3 is the block representation of the proposed design. The components in the FPGA board, besides the designed chip include instrumentation amplifier, analog multiplexer, buffer, Analog to digital converter, DPRAM and Ethernet controller. These additional components are used for interfacing both the inputs to the chip and output to the PC. The input voltage commands are multiplexed, digitized and stored in DPRAM. The data from the ADC is stored in DPRAM in successive locations. 16 Kbytes of memory locations are reserved for the entire 16 channel ie, 1K bytes of memory locations are allocated for each channel. FPGA's main task is to generate the control signals and driving timing signals for the various parts of the system, complete the logic control of the whole system and the driven of the A/D. The FPGA is used to reduce the bandwidth of the incoming data by implementing suitable filter using the soft processor implemented in the FPGA. It also provides the software flexibility to present data from various I/O modules in a consistent manner. Then the data is the taken by the FPGA and it is framed as per the Ethernet protocol. The data is then transmitted to the SRAM in the Ethernet Controller via the data bus according to the address output of the address bus.

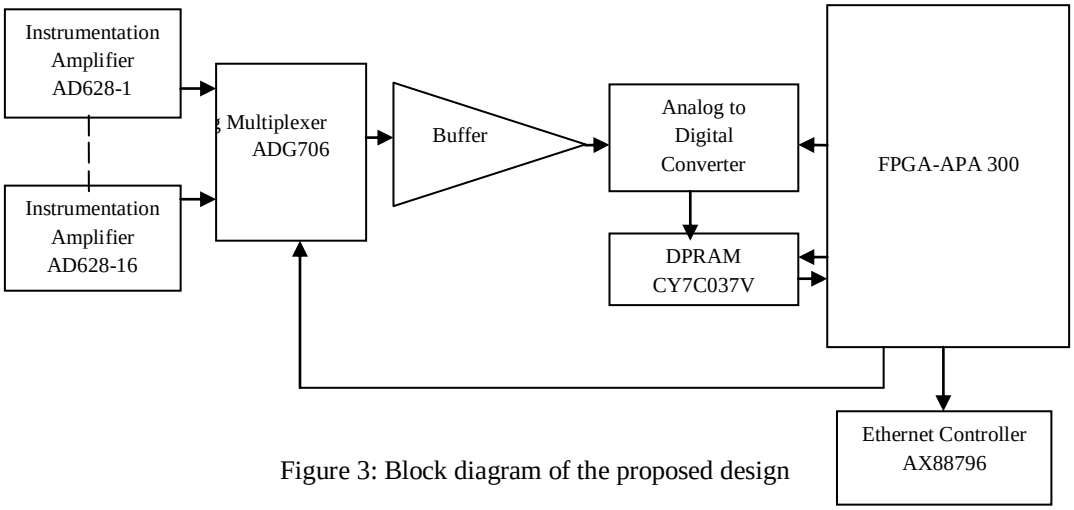

Figure 3: Block diagram of the proposed design

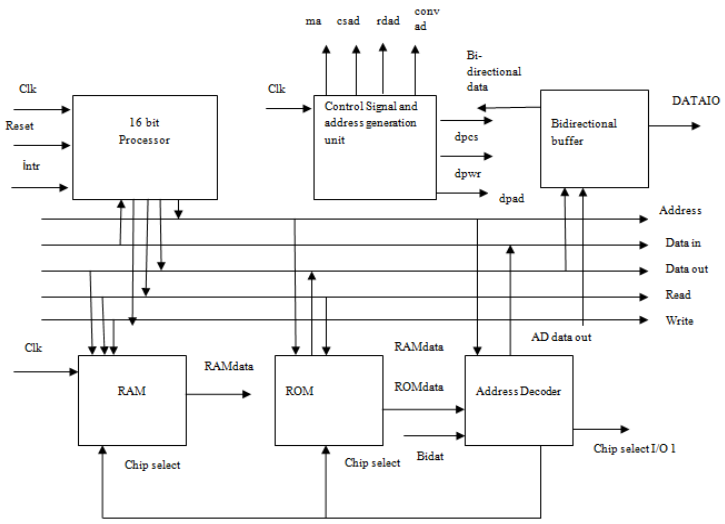

Figure 4: Block diagram of the developed FPGA

Each of the modules is explained in detailed as below.

A. 16 bit processor

CPU-16 is a 16 bit CPU with 64K address space. It has 16 bit address bus and a separate 16 bit data bus. The CPU is a synchronous design therefore it is provided with external clock input and reset signal. To ease communication between CPU and memory or I/O peripherals there are some control signals like write enable (WE_O) to indicate a write operation and read enable (RE_O) to indicate a read operation .

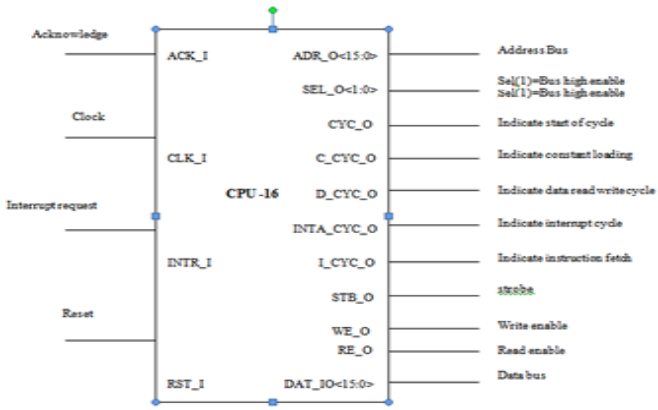

Figure 5: Top view of the 16 bit processor

The two main parts of the 16 bit CPU are the datapath and control unit. The datapath consists of functional units like ALU, Shifter etc and registers: PC, SP, FLAGS, General purpose registers, along with

several other units, registers and muxes. The datapath inputs are control signals like registers' load control signals, muxes' data select signals, operation select signals of ALU and Shifter, Clock input. The data bus is used for both input and output operations. The control of current implementation of CPU-16 is implemented as big synchronous Mealy Machine with 10 states. All the state transitions are performed on next rising edge. The control unit generates various control signals like, data select lines of muxes, clock enable of registers, operation select signals of ALU and Shifter and Bus control signals. The processor is mainly implemented to realize some FIR filter to reduce the bandwidth of the incoming data , configure the registers of the Ethernet controller in a easy way and to store and transmit the data using some special instructions such as movestring

B. Random Access Memory (RAM)

Memory is required to hold programs, perform operations, and execute programming instructions. CPU-16 has 2Kbytes of internal RAM. This memory block is mainly configured as data memory and hence primarily used to store data. Data memory is used for program calculations, look-up tables, and any other memory used by an algorithm. Data memory is normally written to during the execution of a program, where the program might use the data memory as temporary storage for calculation variables and results.

There is a set of data lines and a set of address lines. The data lines serve for both input and output of the data to the location that is specified by the address lines. In addition to the data and address lines, there are usually two control lines: chip enable read enable and write enable. In order for a microprocessor to access memory, either with the read operation or the write operation the chip enable must be active low. The write operation can be done by asserting the write enable signal low and read operation can be done by asserting the read signal active low.

C. Read Only Memory (ROM)

ROM contains the circuit of pre stored words, being the one selected by the address inputs presented at the output. Since it is a read only memory no clock or write enable is required. 2K bytes of memory location is reserved for internal ROM. The pre stored words are the encoded instructions that are to be executed in a particular algorithm.

D. Address Decoder

Address decoder is mainly used to generate the chip select signal for the internal RAM, ROM and the external interfaces. It makes use of the upper address lines to generate the chip select signal. It also determines driver of the data out bus at a particular instance making use of the upper address lines.

E. Control Signal and Address generation unit.

This unit generates the address required by the analog multiplexer for selecting one of the sixteen input channels. It also provides the start of conversion signal for the analog to digital converter and the address for the dual port RAM. It generates the control signals and address by making use of the timing information of the various devices.

F. Bidirectional buffer

A bi-directional buffer can be an input or output buffer with high impedance capability. Here output data from the CPU-16 is given as the input and write enable signal as the control signal to the bi- directional buffer and at the output we get the bidirectional data bus. This data bus provides data to be transmitted to the Ethernet controller and receive the data from the Ethernet controller.

V. Simulation Results

The simulation of VHDL code is done using the Libero IDE 9.1 software. Initially the programmable reset is set for a period of five clock cycle and the inputs, including the clock are applied to the system through the test bench. Then simulation is run and at the end of the run time, we get the output waveforms. Simulation of behavioral models described using VHDL is done for output to conform to requirements.

The simulation results are shown below in figure 6. The shown results are the configuration of internal registers of Ethernet controller and the transmission of data across the Ethernet controller. The data from the DPRAM is taken by the FPGA and moved it to the data port of the Ethernet controller using the move string instruction of the CPU-16. The address bus outputs the address of the instruction to be fetched from the ROM . The steps corresponding to each instruction took place and the data is outputted in the data bus whenever the write becomes low. The chip select corresponding to Ethernet controller is enabled during the configuration of the registers and the transmission of data. FPGA implementation of the proposed design is shown in figure 7.The design is verified in the FPGA by checking the write signal with respect to address and the clock signal.

VI. Conclusions

This paper mainly presents the implementation of a high speed data acquisition system with Ethernet interface. It is designed with the FPGA as the main controller. Because of high integration level, low power consumption, design flexibility, high efficiency and user-programmability, the FPGA-based systems can greatly shorten the system's design cycle, reduce design cost and risk investment. FPGA's main task is to generate the control signals and driving timing signals of the various parts of the system, complete the logic control of the whole system. A 16 bit processor is designed to implement in the FPGA to increase the flexibility, design content ownership, and fewer board-level components. Ethernet comes handy for remote data acquisitions. It also increases the transmission and reception speed of the data. Ethernet is asynchronous in nature and medium access control can be achieved by client-server model. Using a standard network as the interconnection scheme allows independence (in hardware, at least) from a particular vendor and hardware platform. Acquisition resources become available to multiple instruments is the main advantage of the distributed network approach..

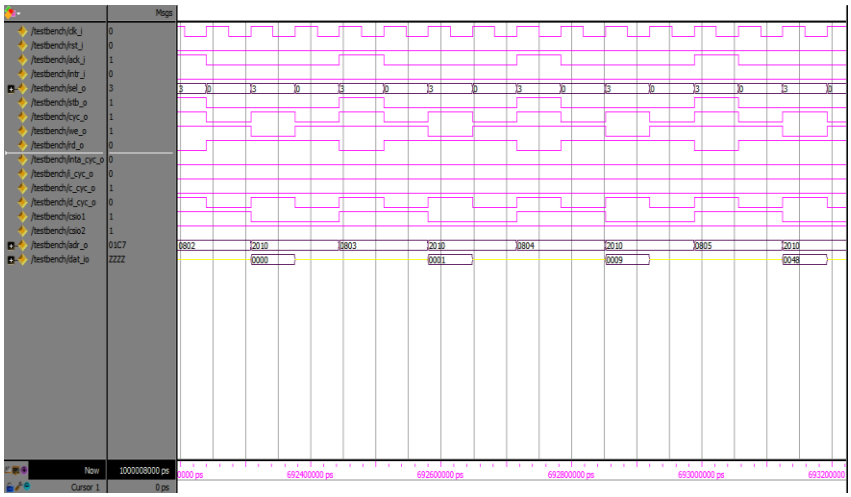

Figure 6: Simulated waveform

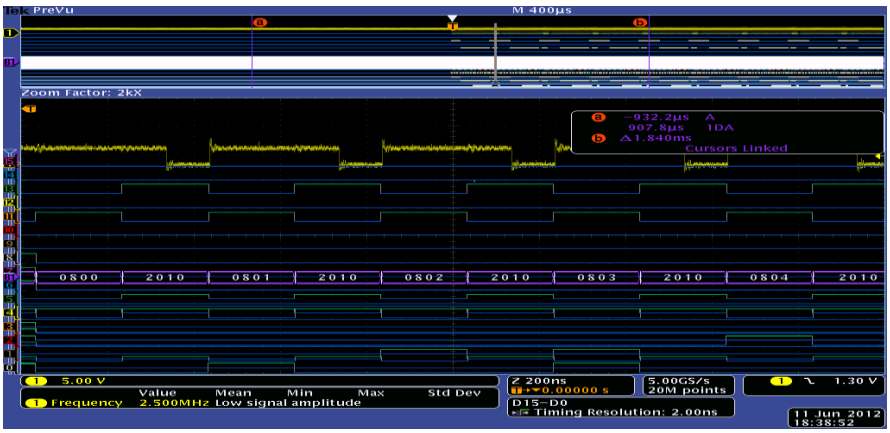

Figure 7: FPGA implementation of the proposed design.

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