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Design of Half Bridge LLC Resonant Converter for Low Voltage Dc Applications

A.Gowri
Department of Electrical and Electronics Engineering Anna University Regional Campus Coimbatore, India.

Abstract: *An advanced hybrid LLC series resonant converter with united flying-capacitor cell is proposed in this paper to permit the high step-down conversion in the high input voltage applications. The in-built flying-capacitor branch in the primary side can efficiently share out the primary switch voltage stress related with the half-bridge LLC converters. And the input voltage can be shared correspondingly and automatically between the two series half-bridge components lacking additional balance circuit or control strategies owing to the built-in flying- capacitor cell. Likewise, the inherent soft switching performance in extensive load range that exists in the LLC converters is still kept to decrease the switching losses, which ensures the high efficiency. In addition, the proposed converter can be comprehensive to reduce the switch voltage stress byemploying stacked connection. Finally, a 500~640 Vinput 48 Voutput 1 kW prototype is built and tested to verify the efficiency of the proposed converter. The results prove that the proposed converter is an excellent candidate for the high input voltage and high step-down dc/dc conversion systems.*

Keywords: *Flying capacitor, Hybrid LLC converter, VoltageAuto-balance.*

I. Introduction

Now a days, The ac/dc converters have been extensively used for numerous offline appliances, such as telecommunications power supply, LED driver, uninterruptible power supply, etc.[1],[2]. Due to the aggregate extent urges the researchers to improve the more advanced ac/dc converters, such as they should be highly efficient, compact in size, and at rational cost. To encounter the standards of harmonic regulation such as, a power factor corrector is generally needed.

Because of the benefits of simple circuit topology and ease control, the boost or buck converters are widely used for power factor correction [3]-[6]. To achieve unity power factor, the output voltage of both converter should be higher than the amplitude of the acline voltage. The suggested integrated ac/dc converter comprises of two stages.

The first one is the acto dc conversion and the second one is dc to dc stage. Theboost converter accomplishes the functionof power factor correction and buck converter controls the dc link voltage. Although it's good performance, the two step operation has two energy conversion manners, which could produce various losses including switching loss, conduction loss, and magnetic core loss. Except the buck and boost converter methodologies, the CUK and SEPIC converter are also used as the power factorcorrectors and regulate the dc voltage. The collective form of buck and the boost converter is CUK converter and the SEPIC converter is the mixture of boost and buck-boost converter. Advantage of both converter is they have a simple circuit topology since they use only one active switch and one diode. An unity power factor can be achieved by operating the boost converter both at discontinuous conduction mode (DCM) or continuous conduction mode (CCM). And the buck or buck- boost converter regulate the output voltage of the boost converter to attain the smooth dc voltage. Before turning ON the active switch, the output voltage is across its parasitic capacitor. The deposited energy in the parasitic capacitor is discharged by turning on the active switch, it sources high switching losses and a high spike current. They also function at the critical conduction mode to active high power factor. The widelyused methodis synchronous rectification (SR) while operating these converters. Replacing the freewheel diode, by using MOSFET hence the conduction loss is effectively reduced. Although, the SR technique requires additional control circuitry to adjust the timing of the switches. Commonly DC to DC converters are used in portable electronic devices such as cell phones and laptop computers, by the power supply from the batteries. Such electronic devices often contain (sometimes higher or lower than the supply voltage).The switched DC to DC converters had an method to increase voltage from the partially lowered battery so the space should be saved instead of using multiple batteries to accomplish the same thing. Mostly DC to DC converter regulate the output voltagealso except high efficiency LED power sources. The DC/DC converters is usually used to maximize the energy harvest for photovoltaic systems and for wind turbines those are called power optimizers. Transformers are used for voltage conversion at foremost frequencies of 50-60 HZ must be large and heavy for power exceeding a few watts. This makes them expensive, and they are subject to energy losses

in their windings and due to eddy currents in their cores. DC/DC techniques that use transformers or inductors work at much higher frequencies, requiring only much smaller, lighter, and cheaper wound components. Consequently these techniques are use where a mains transformer could be used; for example, for domestic electronic appliances it is needed to rectify mains voltage to DC, by using switch-mode techniques to convert it to high frequency AC at the desired voltage, then rectify to DC. The entire complex circuit is cheaper and more efficient than asimple mains transformer circuit of the same output. Because of high efficiency and high power factor the researchers have presented many single stage ac/dc converters based on the integration of PFC stage and a dc to dc stage. Comparing with two stage approaches, the single stage method has advantage of less component count and the circuit topology is simple and the circuit efficiency is improved with single power conversion process.

II. Circuit configuration and operation modes

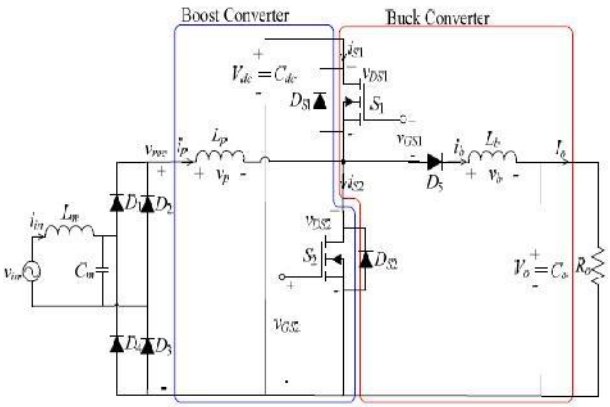


Fig 1. Circuit topology of integrated ac/dc converter

In two stage converter they obtain high power factor with wide load range. If both active switches of the two stage converter operate at the hard switching condition, resulting in a high switching loss and voltage stress.

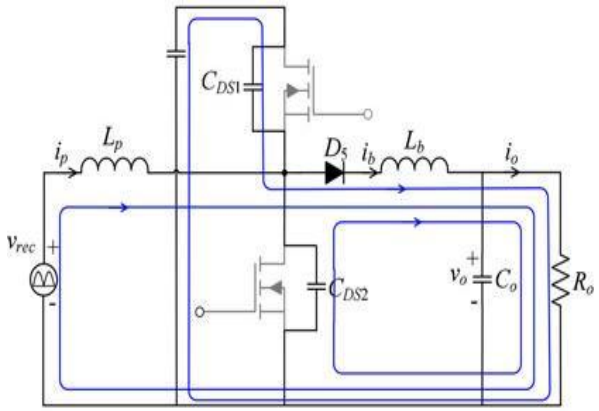
In order to reduce the power issues created by two stage converter, an integrated ac/dc converter is proposed which is shown in Fig.1. The circuit topology of an integrated ac/dc converter is constructed by relocating the position of semiconductor devices. The proposed converter is simply operated by using two switches without zero switchingnetwork andcomplex control. The integrated converter consists of a power switch, diodes and capacitors. Since the switch has a low voltage rating and low conducting resistance, therefore the integrated converter has high efficiency. The output voltage was then taken as feedback and compared with the desired value of the output voltage and the difference is then fedto the PI control which then produces the PWM signal to the switch of the converter. Here the MOSFETs S1 and S2 are used as active switches and the antiparallel diode Ds1 and Ds2 are their intrinsic body diodes. The proposed integrated circuit mainly consists of a low pass filter (Lm and Cm), a diode bridge rectifier (D1 to D4), then the boost and a buck converter. The boost converter is composed of Lp, Ds1, S2 and Cdc and similarly the buck converter is composed of Lb, D5, Ds2, S1 and Co. The buck and the boost converter are operated at the high frequency, fs. The power factor correction is obtained by the boost converter. When the boost converter operates at the discontinuous conduction mode (DCM), the average value of the inductor current at every high switching cycle is approximately a sinusoidal function. The low passfilter is used to reduce the high frequency current. Hence the boost converter can wave shape the input line current to be sinusoidal and in phase with the input voltage. Otherwise called high power factor and low total harmonic distortion (THDi) is achieved. And similarly the buck converter regulates the output voltage of the boost converter to supply stable dc voltage to the load.

Although, the VGS1 and VGS2 are the two gate voltages obtained from a half bridge gate driver integrated circuit are used to alternately turn ON and OFF the switches S1 and S2. The two gate voltages are the complementary rectangular wave voltages. To prevent the active switches from cross conducting, there is a short non overlap time is called “dead time”. In this period, the VGS1 and VGS2 are at the low level. Neglecting the short dead time, the duty cycle of VGS1 and VGS2 is 0.5.

In steady state the circuit operation can be divided in to eight modes that’s shows in Fig.2. It shows the equivalent circuit of each operating modes. The rectified voltage Vrec represents the low pass filter and the diode rectifier. The Fig.3 illustrates the theoretical waveforms in operating modes of the buck converter at DCM. The circuit operation is described as follows.

Fig. 2 Operation modes (a) Mode I (b) Mode II (c) Mode III (d) Mode IV (e) Mode V (f) Mode VI (g) Mode VII(h) Mode VIII.

A. Mode I (t0 < t < t1)



(a)

In Mode 1, S1 is at ON state, the boost inductor current *ip is* zero and the buck inductor current *ib is* supplied by the dc link capacitor which flows through the S1,*D*5,*Lb*, and *Co*.

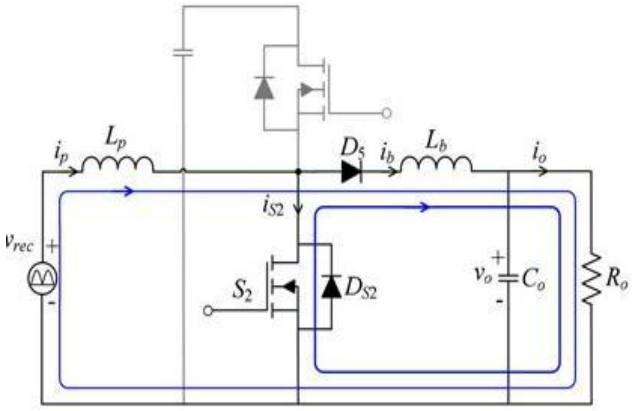
When *S*1 is turned OFF by the gate voltage, *vGS1* the mode 1 get started. The time interval of this mode 1 is the turn-off transition. At the beginning of this mode 1, *ib* is diverted from *S*1 and get flow through the output capacitors *CDS*1 and *CDS*2. Then *CDS*1 and *CDS*2 are charged and discharged, respectively. The voltage across *CDS*2 (*vDS*2) are decreases and to be lower than the rectified input voltage *V*rec, the boost-inductor current *ip get* starts to increase. When *vDS*2 reaches−0.7 V, *DS*2 turns ON and Mode I ends.

B. Mode II (t1 < t <t2)

In Mode II, voltage *vDS*2 is maintainedat −0.7 V by the antiparallel diode *DS*2. After the short dead time, the gate voltage, *vGS*2 turned ON the switch *S*2. If the on resistance of *S*2 is small, most of *ib* current will flow through *S*2 in the direction from its source to drain. By neglecting this small value of *vDS*2, the voltages across *Lb* and *Lp* are equal to

$vb\ (t) = -Vo$

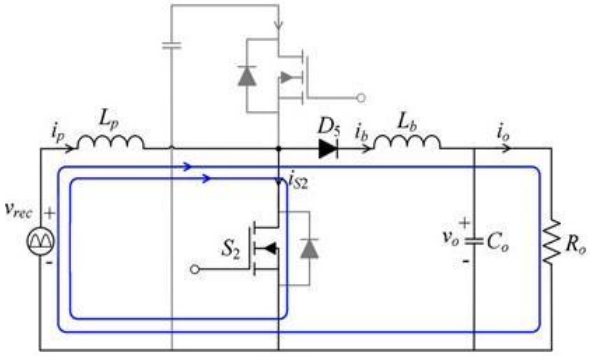
$vp\ (t) = V\text{rec}\ (t) = Vm\ |\sin(2\pi fL\ t)|$



(b)

Where *fL is* the frequency and *Vm is* the amplitude of theInput line voltage, respectively. Since the time interval of ModeI is very short. The boost converter is operate at DCM; therefore, *ip* increases linearly from zero with a rising slope that is proportional to *V*rec. In Mode II, *ib* is higher than the *ip* . And the current *ib has* two loops. Parts of *ib flow* through S2 and the others are equal to *ip and* flow through the line-voltage source, diode rectifier, and *Lp*. This mode 2 ends when *ip rises* to become higher than *ib* .

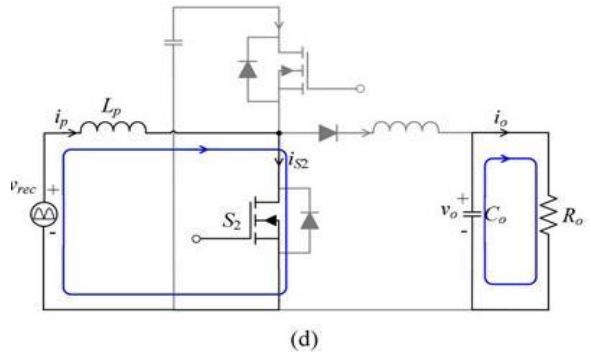
C. Mode III (t2 < t <t3)



(c)

In Mode III operation, *ip* is higher than that of *ib* .Here also the Current *ip* has two loops. Parts of *ip* are equal to *ib* and flow into the buck converter, while the rest flow through *S*2. The current direction in *S*2 is changed naturally, i.e., from drain to source. The voltage and current equations for *vb*,*vp*,*ib*, and *ip*are the same as (1) – (4). Current *ib* continuously decreases. On this period, *ip keeps* increasing. Since the buck converter is designed to operate at DCM, *ib* will decrease to zero at the end of this mode.

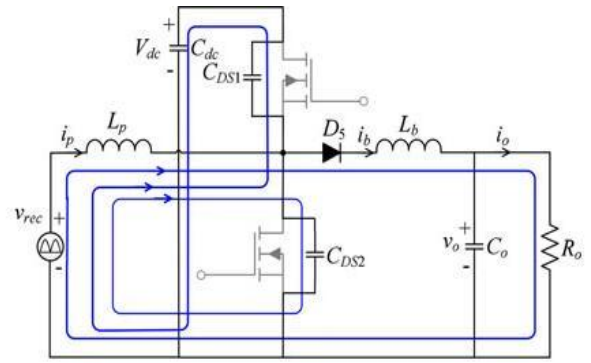
D. Mode IV (t3 < t <t4)



(d)

In this mode 4 operation, S2 remains ON to carry boost inductor current *ip*. Because buck inductor current *ib* is zero, the buck converter is at "OFF" state and the output capacitor *Co* supplies the current to load. When *S*2 is turned OFF by the gate voltage *vGS*2 , Mode IV ends.

E. Mode V (t4 < t <t5)



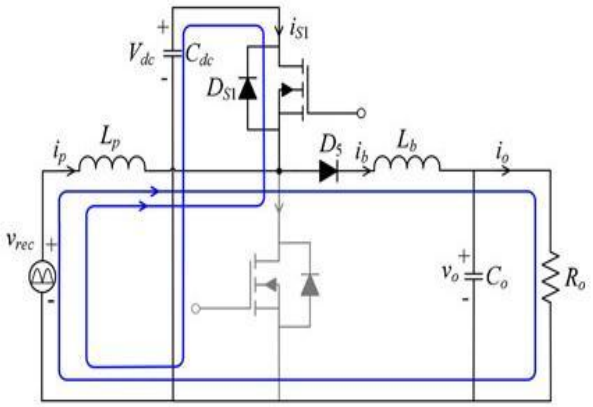
(e)

The boost inductorcurrent ip *reaches* a peak value at the time instant of turning OFF *S*2. For maintaining flux balance in *Lp*,*ip* will be diverted from the *S*2 to flow through *CDS*1 and *CDS*2 when the switch

S2is turned OFF. *CDS*1 and CDS2 are discharged and charged, respectively. Buck inductor current *ib* is zero at the beginning of this mode and it will start to increase, when the voltage across *CDS*1(*vDS*1) decreases tobe lower than the *V*dc − *Vo* , that is the voltage across *Lb* becomes positive. When *vDS*1 reaches −0.7 V, *D*S1 turns ON and Mode V ends.

F. Mode VI (t5 < t <t6)

At the beginning of Mode VI operation, *vDS*1 is maintained at about −0.7 V by the antiparallel diode *DS*1. After the short dead time, the gate voltage *vGS*1 turned ON the switch *S*1. If the on-resistance of switch *S*1 is small enough, most of boostinductor current *ip* will flow through *S*1 in the direction from its source to drain.

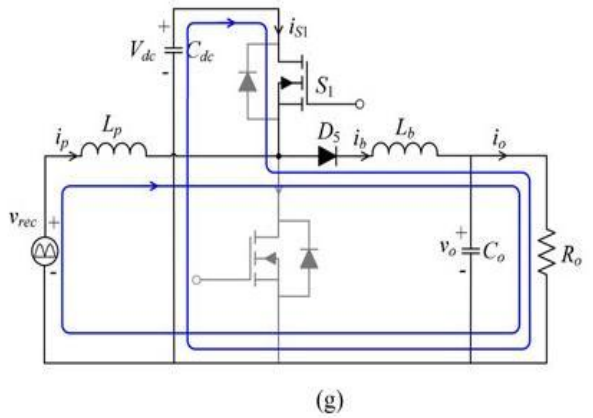


(f)

By neglecting this small value of *vDS*1, the voltage imposed on *Lp* and *Lb* can be, respectively, expressed as
vp (*t*) = *V*rec (*t*) − *V*dc = *Vm* |sin (2*πfL t*)| − *V*dc
vb (*t*) = *V*dc − *Vo* .

In Mode VI, boost inductor current *ip* is higher than buck inductor current *I b.* There are two loops for buck inductor current *ip* .Parts of *ip* flow through *S*1 to charge the dc-link capacitor *C*dc and the rest are equal to *ib* and flow into the buck converter. This mode ends when boost inductor current *ib rises* to become higher than the buck inductor current *ip.*

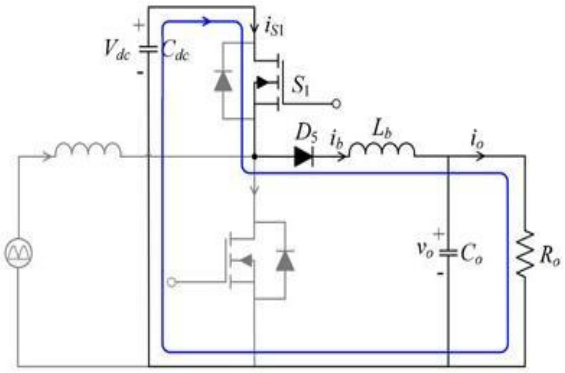
G. Mode VII (t6 < t <t7)



(g)

In operation Mode VII, *ib is* higher than that of *ip.* Here there are two loops for *ib* . Parts of *ib* are equal to *ip* and flow into the boost converter, while the rest flow through switch *S*1 . The current direction in switch *S*1 is changed naturally, i.e., from drain to source. The voltage and the current equations for *vp,vb,ip,* and *ib are* the same as (5)–(8).Buck inductor current *ib* increases continuously, while boost inductor current *ip keeps*decreasing. The circuit operation enters next mode as soon as*ip decreases* to zero.

H. Mode VIII (t7 < t <t8)



(h)

The switch *S*1 remains ON and the buck inductor current *ib* keeps increasing. When the gate voltage *vGS*1 is at low level to turn OFF *S*1, this mode get ended and the circuit operation again returns to Mode I of the next high-frequency cycle. Based on the circuit operation, prior to turning on one active switch, the output capacitance is discharged to about 0.7 V by the inductor current. Then, the intrinsic body diode of the active switch is turns ON to clamp the active voltage at nearly zero voltage. In this way, each active switch achieves ZVS operation. The reason for operating the buck converter at DCM is, In operation Mode II, *ip* rises and *ib* decreases. It should be noted that the *ip* rises in proportional to the input voltage and has a small peak value of zero-cross point of the input voltage. If the buck converter is operated at CCM, *ib* could be keep higher than *ip*. On this condition, the circuit operation would not enter in to the Modes III and IV, and gate voltage *vDS*1 is maintained at about *V*dc. When *S*1 is turned ON, *ib is* diverter from *S*2 to*S*1 .*CDS*1 is discharged at the high voltage of *V*dc, resulting a spike current and high switching losses.

III. CIRCUIT ANALYSIS

According to the operating modes in the previous section,
it can be clearly seen that the antiparallel diode of the active switch of one converter serves as the freewheeling diode of the other converter. Therefore, the two converters can be analyzed separately.

A. Boost-Converter-Type Power-Factor Corrector

The boost-inductor current *ip increases* from zero and reaches then a peak value at the end of the Mode IV. Practically, the frequency of the input line voltage, *fL,* is much lower than that of the converters. It is reasonable to consider that the rectified input voltage *V*rec as a constant over a high-frequency cycle. The peak values of boost inductor current *ip can* be expressed as.

$$i_{p,\,peak}(t) = \frac{V_m\,|\sin(2\pi f_L t)|}{L_p}(t_4 - t_0)$$

$$= \frac{V_m\,|\sin(2\pi f_L t)|\,T_s}{2L_p}$$

$$k = \frac{V_{dc}}{V_m}$$

where the index *k* is defined as
Where *T* is the high-frequency switching period. At the beginning of Mode V, boost inductor current *ip* start to decrease. Therefore the above equation can be rewritten from

$$i_p(t) = \frac{V_m\,|\sin(2\pi f_L t)|\,T_s}{2L_p}$$

From the above equation, the duration of the interval during which the boost inductor current *ip* decreases

from the peak value to zero is described by

$$t_{p,\,\mathrm{off}}(t) = \frac{0.5 T_s V_m |\sin(2\pi f_L t)|}{V_{dc} - V_m |\sin(2\pi f_L t)|}$$

In order to operate the boost converter at discontinuous mode (DCM), $tp,\mathrm{off}\ (t)$ must always be less than the half of the switching period

$$tp,\mathrm{off}\ (t) \le 0.5Ts\ .$$

Combining above two equations, the gate voltage $V\mathrm{dc}$ should be high enough to ensure the discontinuous conduction mode (DCM)operation over an entire input line-frequency cycle, as follows:

$V\mathrm{dc} \ge 2Vm.$

It is noted that the peak values of boost inductor current *ip* follow a sinusoidal envelope. The average value of *ip* over a high-frequency cycle is given by

$$Ip(t) = \frac{(0.5T_s + t_{p,\,\mathrm{off}}(t)).\ i_{p,\,\mathrm{peak}}(t)}{2T_s}$$

After substituting the equations

$$i_p(t) = \frac{V_m |\sin(2\pi f_L t)|}{8.\ L_p.\ f_s^2} \cdot \frac{1}{1 - \frac{1}{k}.|\sin(2\pi f_L t)|}$$

It can be seen that the *i*in will be close to a sinusoidal waveform at a large value of index *k*. In other words, gate voltage *V*dc should be high enough to have a sinusoidal input current. Using above equations, the input power can be obtained by the taking average of the instantaneous product of the input voltage and current over one line-frequency cycle.

Assuming ac efficiency of η, the output power can be expressed

$$P_o = \frac{\eta V m^2}{8.\ L_p.\ f_s} \cdot y$$

Since the input voltage is purely sinusoidal, then the power factor is defined as the ratio of input power to the product of the root-mean-squared values of input voltage and current can be obtained by using above equations.

$$\mathrm{PF} = \frac{P_{in}}{\frac{V_m}{2} I_{in,rms}}$$

The power factor as a function of index *k* is calculated, by using above equations. As shown, high power factor can be achieved at a high-valued *k*. The index *k* should be higher than
2. In this situation, power factor is better than 0.99.

B. Buck Converter

For discontinuous conduction mode (DCM) operation, buck inductor current *ib* rises from zero. Neglecting the short transition of turning OFF switch *S*2 , the rising time of buck inductor current *ib* is equal to 0.5*Ts*. Then, the *ib* has a peak value that is equal to

$$i_{b,\,\mathrm{peak}} = \frac{(V_{dc} - V_o)\ T_S}{2L_b}$$

The buck inductor current *ib* starts to decrease, when the switch *S*1 is turned OFF. The time duration for buck inductor current *ib* decreasing from the peak value to zero is given by
For the DCM operation, *tb*,off should be less than 0.5*Ts.* This leads to

$$V\mathrm{dc} \le 2Vo$$

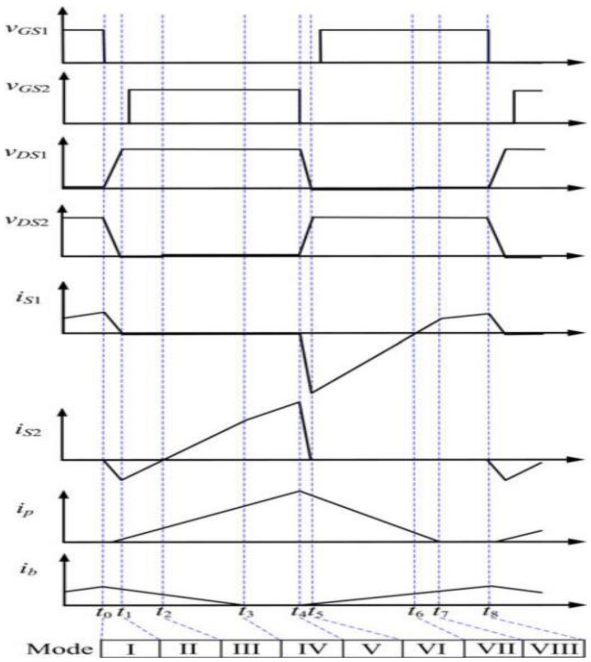


Fig. 3. Theoretical waveforms of the proposed converter.

As shown in Fig. 3, buck inductor current *ib* is with a triangular waveform and its average value can be derived by

$$\overline{ib} = \frac{(0.5T_s + t_{b,\text{off}})i_{b,\text{peak}}}{2T_s} = \frac{(V_{dc} - V_o)V_{dc}T_s}{8L_bV_o}$$

At the steady-state operation, the average value of buck inductor *ib* will be equal to the output current

$$\overline{ib} = I_o = \frac{V_o}{R_o}$$

By combining above all equations, the formula of *Lb* for discontinuous conduction mode (DCM) operation is derived as follows:

$$L_b = \frac{(V_{dc} - V_o)V_{dc}T_s}{8V_oI_o}$$

$$= \frac{(V_{dc} - V_o)V_{dc}}{8P_of_s}$$

IV. Design example and experimental results

An illustrative example for driving the 60 1-W high-brightness LEDs is provided. These light emitting diode (LEDs) are connected in series. The rated voltage and current of each LED are 3.6 V and 0.28 A, respectively. Table I lists the circuit parameter specifications. In this design example, both buck and boost Converters are designed to operate at discontinuous conduction mode (DCM). The circuit parameters are designed as follows

Table ICircuit Specifications

Input Line Voltage, *v*in	110 *V*rm s ± 10%, 60 Hz
High Switching Frequency, *fS* 1, *fS* 2	50 kHz
Output Power, *Po*	60 W
Output Voltage, *Vo*	216 V (= 3.6 V × 60) Output Current, *I*o 0.28 A

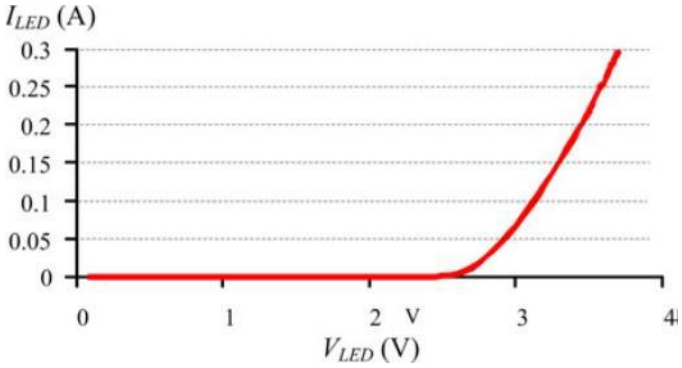


Fig. 4. *V–I* curve of tested LED.

A. Parameters Design

*V*dc should be limited between 2*Vm* to 2*Vo* . Taking the chosen to be *V*dc = 360V. In this case, index *k* is calculated to be 2.3. From Fig. 6, the power factor higher than 0.99 can be expected. Assuming 95% circuit efficiency, *Lp* and *Lb* can be calculated

Filter inductor*Lm* and Filter capacitor *Cm* are designed to perform as a low-pass filter to filter out the high-frequency components of the boost inductor *ip* . By rule of thumb, the natural frequency of a low-pass filter is about 1 decade below the switching frequency. Here, the natural frequency of low pass filter is designed to be 5 kHz, and *Lm* and *Cm* are determined to be *Lm* = 2.16 mH ,*Cm* = 0.47 μF.

B.DimmingOperation

The prototype circuit is built and tested. Table II lists the circuit parameters. Since the *I-V* characteristic of an LED is similar to that of a diode characteristics, a small variation in the LED voltage will result in the significant change in its current. Generally, the constant current control with the low- frequency pulse-width modulation is usually used to realize the LED dimming. However, it requires complicated circuit to detect the peak value of the pulsed LED current.

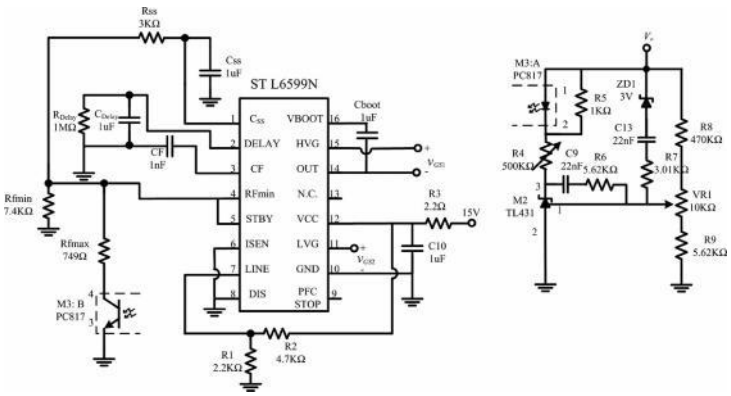


Fig. 5. Control circuit.

In this prototype circuit, 60 LEDs are connected in series, and then, more voltage change is needed to dim the light emitting diode (LED). It makes the series-connected LEDs can be easily dimmed by the voltage control. The closed-loop control circuit that mainly consists of a double-ended controller (L6599) for half-bridge topology and a photo coupler (PC817). The L6599 provides a pair of gate voltages with fixed dead time (0.3 μs) to drive both the active switches. Output voltage regulation is achieved by modulating the switching frequency. The feedback signal of the output voltage is transferred to the pin 4 of L6599 through the phototransistor of the optocoupler to modulate the switching frequency. The output voltage is varied by adjusting the variable resistor VR1 for dimming LED.

Figs. 6–19 shows the voltage and current waveforms that are measured the rated output power. Fig. 6 shows the waveforms of the input voltage, the input current, and the boost-converter current. It has been seen that the boost converter operates at discontinuous conduction mode over an entire cycle of the line voltage. The input current is nearly close to a sinusoidal waveform. Although, the input current and the input voltage are

in phase with each other. High power factor and the low total harmonic distortion (THDi) can be achieved. The measured power factor and (THDi) are 0.994 and 9.27%, respectively. It complies with the standards of IEC 61000-3-2 class D. It reaches nearly unity power factor.

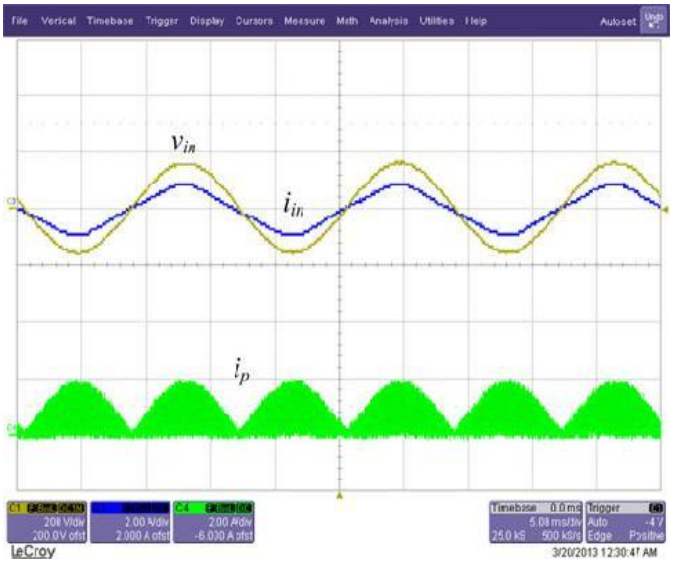


Fig. 6. Waveforms of *v*in , *i*in , and *ip* (*v*in : 200 V/div, *i*in , *ip* : 2 A/div, time: 5 ms/div)

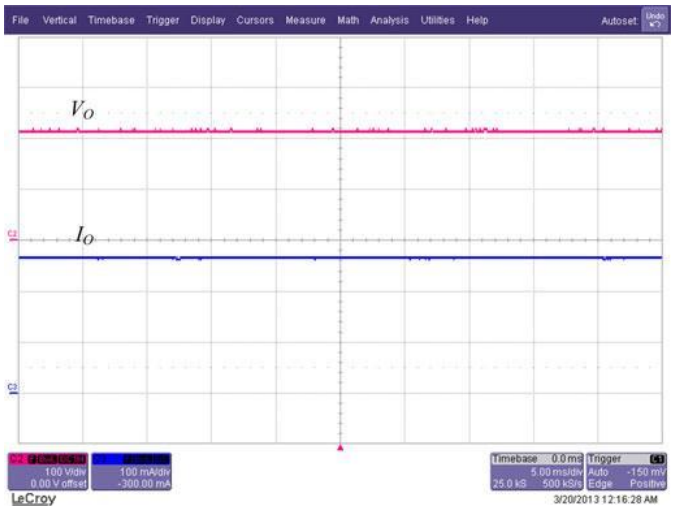


Fig. 7. Waveforms of *Vo* and *Io* (*Vo* : 100 V/div, *Io* : 0.1 A/div, time:

Fig. 7 shows the waveforms of the output voltage and output current. The measured values well satisfy the theoretical prediction. The inductor-current waveforms of both converters are shown in Fig. 8. Both converters operate at DCM. Fig. 9 shows the voltage and current waveforms of the active switches, which are measured at the peak point and thezero-crossing point of the input-line voltage, respectively.As shown, both the active switches are switched ON at nearly zero voltage.

With ZVS operation at both active switches, the circuit efficiency is as high as 94.8%. It is noted that boost inductor current *ip* is almost zero at the zero-crossing point of the ac voltage and cannot fully discharge the output capacitance of switch *S*1 within the dead time. When switch *S*1 is turned ON at the end of dead time,the remaining charges in the output capacitance rapidly flow through the switch *S*1 , resulting in the spike current, as shown in Fig. 9(b). In order to know how much the efficiency can be improved with proposed integrated circuit, a two-stage boost and buck prototyped circuit is built and tested with the same circuit specification as the proposed circuit. At 50-kHz switching frequency, the measure efficiency of the two-stage circuit is 90.7%.

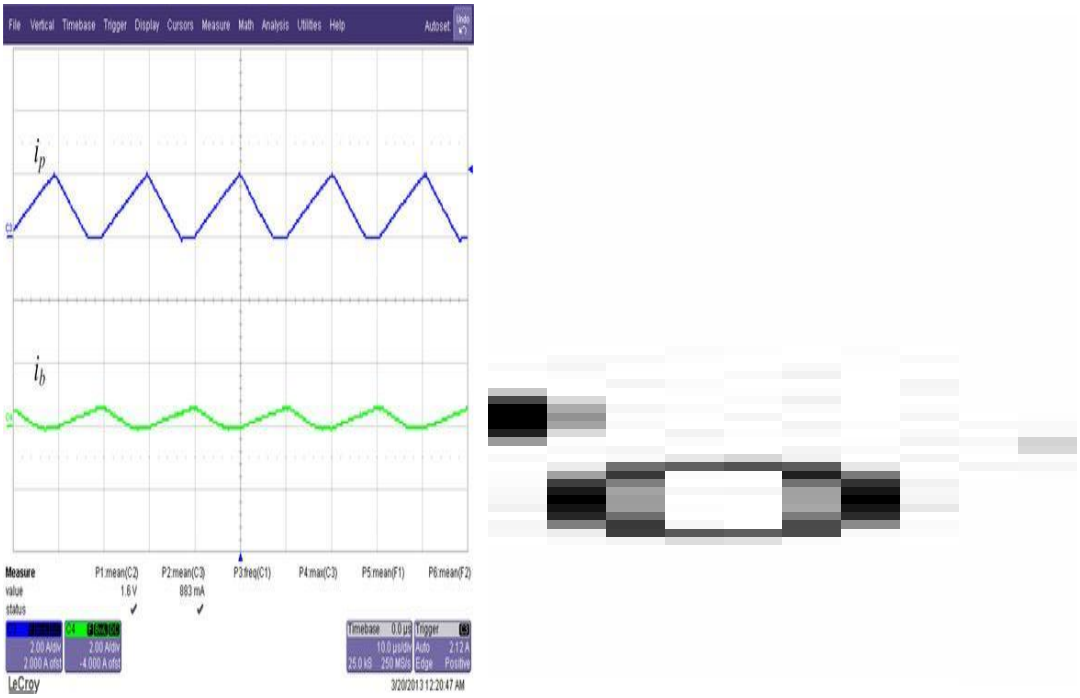


Fig. 8. Waveforms of *ip* , and *ib* (*ip* , *ib* : 2 A/div, time: 10 us/div).

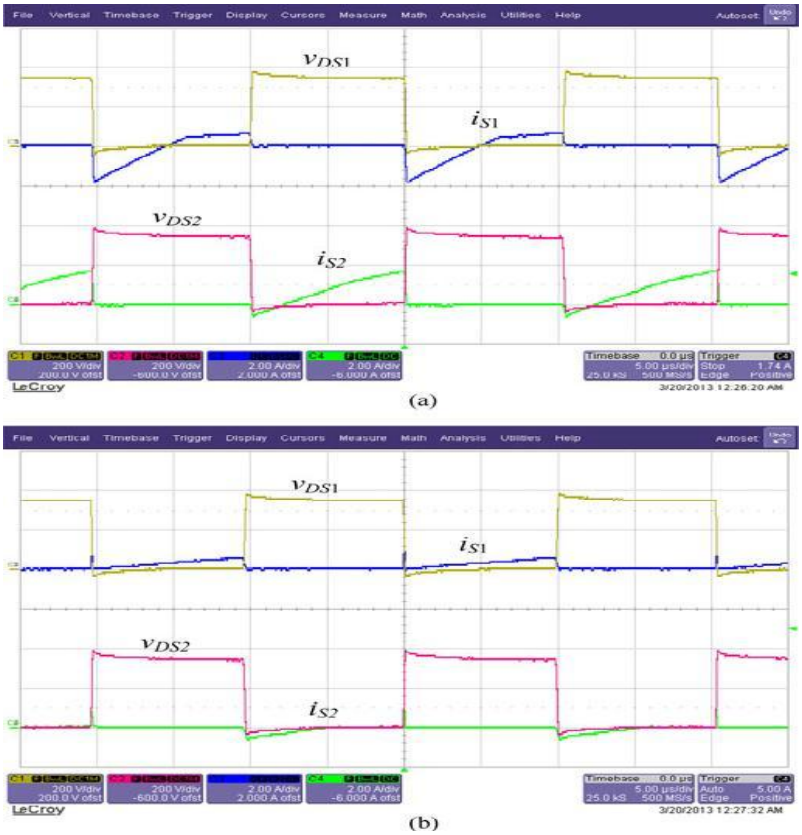


Fig. 9. Waveforms of *vDS*1 , *iS* 1 , *vDS*2, and *iS* 2 at (a) the peak point and (b) the zero-crossing point of the input-line voltage (*vDS*1 , *vDS*2 : 200V/div, *iS* 1 , *iS* 2 : 2 A/div, time: 5 us/div).

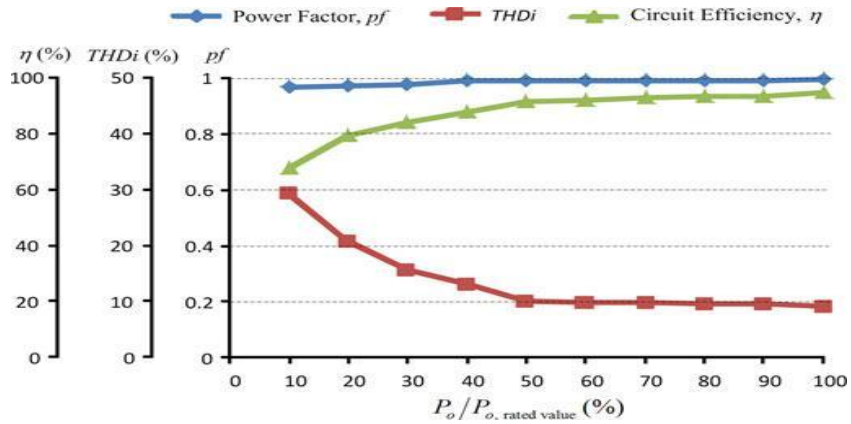


Fig. 10. Measured power factor, THD*i*, and circuit efficiency for different output power.

The measured curves of the power factor, THDi, and circuitefficiency over a load ranges from 30% to 100% rated power are shown in the Fig. 10. Power factor is close to unity over the wide load range, while THDi increases dramatically when the output power is less than 50% of rated power. Since the output power is inversely proportional to the switching frequency, more circuit losses would happen at light load. The circuit efficiency drops to 0.84 at 30% rated power.

V. Conclusion

The high-efficiency integrated ac/dc converter that combines the boost converter and a buck converter is proposed. Byfreewheeling the inductor currents of the converters to flow through each of the intrinsic diodes of the MOSFETs, both the active switches are turned ON at zero voltage switching ZVS. It assures high circuit efficiency. The boost converter is designed to operate at discontinuous conduction mode(DCM)to perform the function of power factor correction PFC. Itrequires that dc link voltage should be two times higher than that of the amplitude of input voltage. The buck converter further regulates the dc-link voltage to obtain the stable dc voltage with low ripple contents. Experimental results based on the 60-W prototype circuit show that high circuit efficiency, high power factor, and low harmonics THDi can be achieved over a wide load range. A circuit efficiency of94.8%, power factor of 0.993 and a THDi of 9.27% are measured at rated output power.

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