IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)
e-ISSN: 2278-1676,p-ISSN: 2320-3331, Volume 12, Issue 2 Ver. I (Mar. – Apr. 2017), PP 66-79
www.iosrjournals.org

High Efficiency Dc-Dc Converter for Renewable Energy Applications and High Voltage Gain with Less Losses

S.Prema
[1]*(PG Scholar, Electrical and Electronics Engineering, Anna University Regional Campus, Coimbatore, India)*

Abstract: *Renewable sources like solar PV cell is prefer to be operated at low voltages. This paper proposes a novel high voltage gain, high efficiency dc-dc converter based on coupled inductor, intermediate capacitor. The input energy acquired from the source is first stored in the coupled inductor and intermediate capacitor in a lossless manner. Improve the voltage gain and efficiency of the system. Exorbitant duty cycle values are not required for high voltage gain, when prevent the problems such as diode reverse recovery. Presence of a passive clamp network causes reduced voltage stress on the switch. Overall performance of the renewable energy with a step-up DC/DC converter using closed loop control action is used in the proposed system, improving the overall efficiency of the system.*

Keywords: *Dc-Dc Power Converter, Power Conditioning, Coupled Inductor, Switched Capacitor, Active Clamp, Passive Clamp, High Voltage Gain, Solar Photovoltaic).*

I. Introduction

Renewable energy sources (RES) hase experienced a fast development in recent years. Those systems employ with micro sources like PV, fuel cells etc. Though PV cells can be made into array and connected in series to produce high voltage they exist serious problems like shadowing effects, short circuit which drastically reduces its efficiency. In order to overcome such effects this micro source energy is utilized by the high step up converter to produced high voltage and satisfy the demands. Conventional boost converters can't provide such a high DC voltage gain for extreme duty cycle.In the last few decades, there has been a drastic increase in the demand for electricity. This has rapid use and depletion of fossil fuels. These factors have led the researchers to renewable energy sources such as wind, solar PV and fuel cell stack. Solar Photovoltaic (PV) and fuel cell energy sources play a prominent role among the existing renewable sources poses major challenges such as: (a) Optimal utilization of the source due to their non-linear characteristics (e.g. Maximum Power Point Tracking (MPPT) is required to track maximum available power from a PV source); (b) They are usually operated at low output voltage levels (typ. 25-50V) because of safety issues. This makes their application to the grid connected systems and some stand-alone loads difficult because of large voltage boosting is required.
Use of conventional dc-dc converters has the following disadvantages:
1. It causes large peak current to flow on the input side, which adversely affects the magnetic components and results in high losses. 2. It causes large voltage to appear across the switch. As the on state resistance of a switch depends on its voltage rating [*RDS(on)□VDS 2*], the conduction losses increase. Due to large duty cycle, the losses in parasitic resistances of inductance and capacitance also increase. 3.Diode reverse recovery becomes a major concern. In view of the above, there is clearly a need to develop and use special high gain, high efficiency dc-dc converters to implement MPPT and to step up voltage level. Several circuit topologies have been proposed in the past [3-6] for this application. They follow one or more of the following philosophies to achieve high voltage at the converter output.

II. Circuit Configuration And Operation Modes

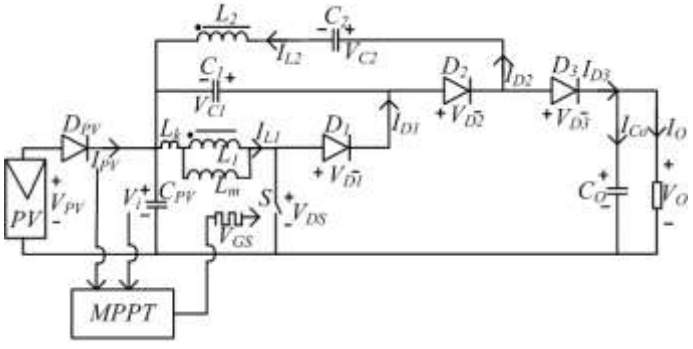


Fig 1. Circuit topology of dc/dc converter

Energy conversion efficiency of solar PV is quite low (about 12–25%) [24]. Therefore, it is essential to use a highly efficient power conversion system to utilize the PV generated power to the maximum. The proposed high gain dc-dc converter configuration is shown in Fig. 3. It consists of one passive clamp network, a coupled inductor (*L1*,*L2*) and an intermediate capacitor apart from other components The symbol *VPV* represents the PV voltage applied to the circuit. *S* is the main switch of the proposed converter. The coupled inductor's primary and secondary inductors are denoted by *L1* and *L2*. *C1* and *D1* represent the passive clamp network across *L1*. The capacitor *CO* is the output capacitor while *D3* is the output diode. The voltage *VO* is the average (dc) output across the load. The intermediate energy storage capacitor, *C2* and the feedback diode *D2* are connected on the secondary side.

CL FILTER

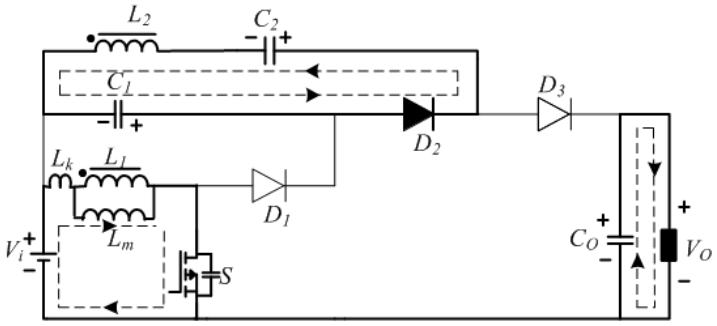
A device (usually a membrane or layer) that is designed to block certain objects or substances while letting others through.Due to the global energy challenge, grid-tied inverters for the renewable energy sources are becoming widely used today. They can be divided into voltage-source inverters (VSI) and current-source inverters (CSI), where the VSI is the dominant converter.

One of the reasons is the Voltage Source Inverter (VSI) does not need to large inductor as the energy storage element, while the current Source Inverter (CSI) should adopt a larger inductor in order to keep the dc current constant for a proper modulation technique. The research related to Current Source Inverter (CSI) mainly focus on the control. So far, the total dc-link inductance for Current Source Inverter (CSI) is a challenge, especially in the low voltage and the three-phase applications area. Since the VSI is a step-down inverter and the Current Source Inverter (CSI) is a kind of step-up inverter, the *Z*-source inverters (ZSI) was proposed in order to fully utilize the basic character of Voltage Source Inverter (VSI) and Current Source Inverter(CSI) and the minimum semiconductors is used with the combined characters of the step-down and the step-up converters. However, compared to the Current Source Inverter(CSI) or theVoltage Source Inverter(VSI), the Z-Source Inverter Z(SI) has two extra inductors in the power loop, which may sacrifice the efficiency the control difficulty is also a demerit in the *Z* source impedance.

Full-bridge single-phase grid-tied inverters with the different power sources are introduced. And a new type of "buck in buck Converter, boost in boost Converter" grid-tied inverter is proposed and the operating principle is illustrated through a half-bridge inverter is equivalent circuits in the different working stages. Then, the modeling is carried out with a small signal model method. Based on this, the indirect current control method is introduced, when the inverter is working in the "boost" stage.

Fig. 2 Operation modes (a) Mode I (b) Mode II (c) Mode III (d) Mode IV (e) Mode V .

A. Mode I (t0 < t < t1)



The gain ratio, *n* is given by:

$$n = \frac{V_{L2}}{V_{L1}} \quad (1)$$

where, *VL1* and *VL2* represent the voltages across inductors *L1* and *L2*. The operating modes for continuous conduction mode (CCM) are shown in Fig. 4. Various operating modes are described below:

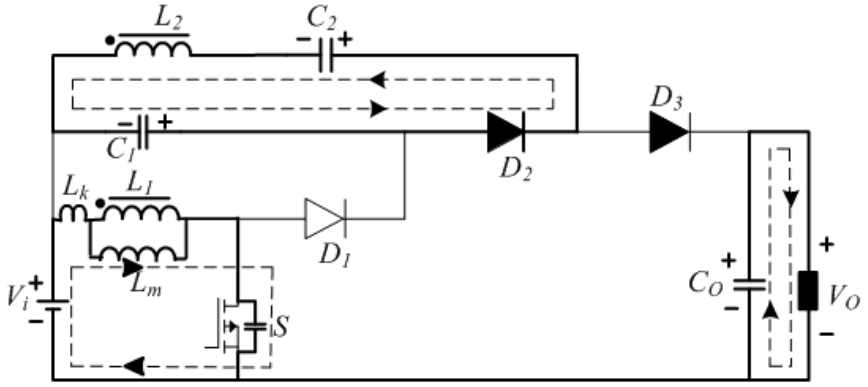
Mode 1[*t0-t1*]:

The switch (*S*) is turned on at the start of the converter operation. The current flows through the switch and the primary side of the coupled inductor (*L1*), energizing the magnetizing inductance (*Lm*) of the coupled inductor. The current path is as shown in Fig. 4(I). The two diodes, *D1* and *D3* are reverse biased, while *D2* is forward biased during this mode. The intermediate capacitor, *C2* is charged through *D2* by *L2* and capacitor, *C1*.If voltage across intermediate capacitor (*C2*) becomes equal to the summation of voltages across *L2* and *C1*, diode *D2* turns off. The current flowing through *Lm* (*iLm*) in this mode may be obtained by using the following relation:

$$i_{Lm}(t) = \frac{v_i}{L_m + L_k}(t - t_0) + i_{Lm}(t_0) \qquad (2)$$

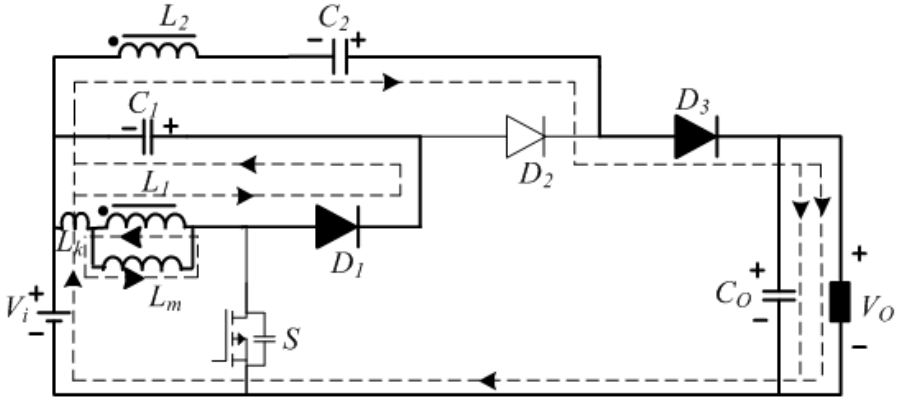
B. Mode II (t2-t3):

The parasitic capacitance of the switch *S* is charged by the magnetizing current flowing through the inductor *L1*. The diode *D2* remains forward biased and current continues to flow through this. Current path in this mode is shown in Fig. 4(II).The magnetizing inductance current for this mode is given by the following equation:

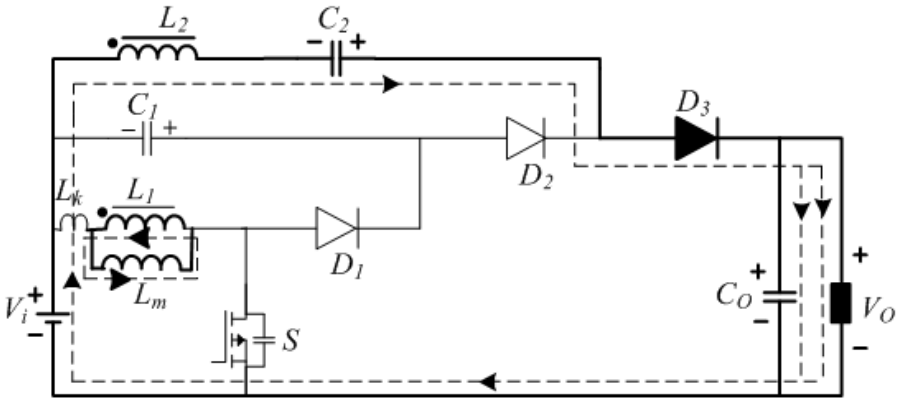


$$i_{Lk}(t) = \frac{v_{C1}}{L_m + L_k}(t - t_2) + i_{Lm}(t_2) \qquad (3)$$

C. Mode III[*t2-t3*]:



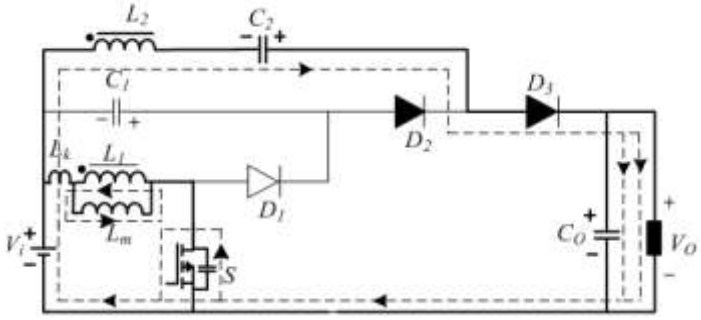
In Mode III operation, *ip* is higher than that of *ib* .Here also the Current *ip* has two loops. Parts of *ip* are equal to *ib* and flow into the buck converter, while the rest flow through *S*2 . The current direction in *S*2 is changed naturally, i.e., from drain to source. The voltage and current equations for *vb* , *vp* , *ib* , and *ip* are the same as (1) – (4). Current *ib* continuously decreases. On this period, *ip* keeps increasing. Since the buck converter is designed to operate at DCM, *ib* will decrease to zero at the end of this mode.



Mode 4[*t3-t4*]:
This mode begins after the completion of recovery of the leakage energy from inductor *L1*. The diode *D1* now becomes reverse biased while diode *D3* remains forward biased in this mode. The current flows from the input side to the output side to supply the load as shown in Fig. 4(IV). The current *iLm* flowing through secondary inductor (*L2*) is given by the following equation:

$$i_{Lm}(t) = \frac{(V_0 - V_{C2} - V_i)}{nL_m}(t - t_3) + i_{Lm}(t_3) \qquad (8)$$

E. Mode V (t4 < t < t5)



Mode 5[*t4-t0*]:
This mode begins by turning on switch *S*. The leakage inductor energizes quickly using the full magnetizing current while the parasitic capacitance across the switch discharges in this mode. The two diodes *D1* and *D2* are in reverse biased condition. The current flow path in this mode is shown in Fig. 4(V). This mode ends when diode *D3* becomes reverse biased and current flow through inductor, *L2* changes direction. The secondary inductor current (*iLm*) continues to flow in this mode and current is given by:
Since the current through an inductor.

$$i_{Lm}(t) = \frac{(V_0 - V_{C2} - V_i)}{nL_m}(t - t_4) + i_{Lm}(t_4) \qquad (4)$$

cannot change instantaneously, current rises slowly. The voltage (*VDS*) across the switch 'S' cannot change instantaneously and decreases slowly. Thus, there is little overlap of falling voltage and rising current and negligible switching loss at turn-on. Typical waveforms of the circuit are shown in Fig. 5.

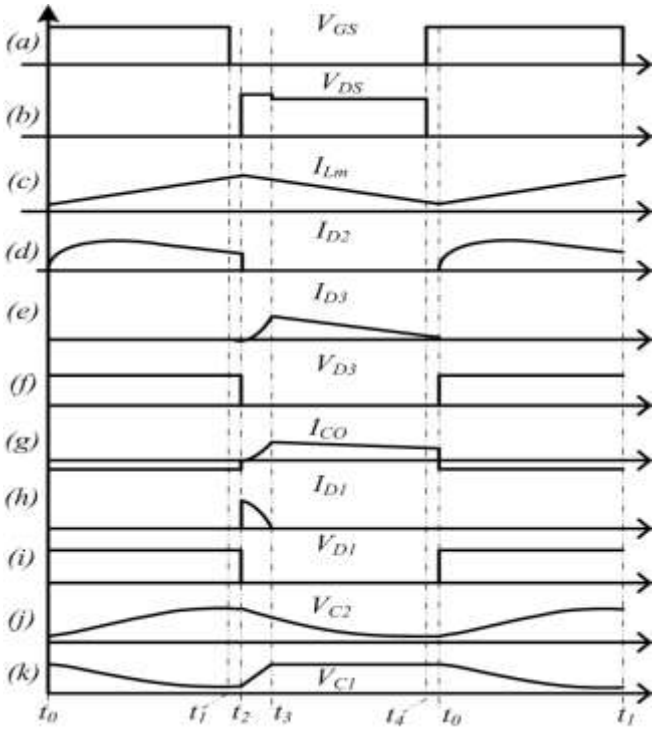


Fig. 5 Typical waveforms during CCM operation.

III. Circuit Analysis

This section presents the analysis of the proposed converter which can be used for its design. All the elements used in the converter are assumed to be ideal. When Switch S is ON: The voltage across L1 is given by:

$$V_{L1(ON)} = V_i \quad (5)$$

The voltage across L2 is given by:

$$V_{L2} = V_{C2} - V_{C1}$$

$$V_{L2} = nV_i \quad (6)$$

When Switch S is OFF: The voltage across L1 is given by:

$$V_{L1(OFF)} = -V_{C1} \quad (7)$$

Applying Kirchoff's voltage law in Mode 3 yields:

$$V_{L2} = V_i + V_{C2} - V_o \quad (8)$$

By substituting VC2 from (11) and (12) into (13), it becomes:

$$V_{L2} = V_i - V_{L1(OFF)} + nV_i - V_o$$

$$\text{Also, } V_{L1} = \frac{V_{L2}}{n} \quad (10)$$

By substituting (7) into (8), voltage expression during switch off condition becomes:

$$V_{L1(OFF)} = \frac{(V_i - V_{L1(OFF)} + nV_i - V_o)}{n}$$

$$\text{or, } V_{L1(OFF)} = \frac{(V_i + nV_i - V_o)}{(n+1)} \quad (11)$$

Voltage Gain: By applying voltage-sec balance across L1:

$$V_{L1(ON)}d + V_{L1(OFF)}(1-d) = 0 \quad (12)$$

Substituting values of *VL1(ON)* and *VL1(OFF)* from (6) and (11) respectively into (12) yields:

$$V_i d + \frac{(V_i + nV_i - V_o)}{(n+1)}(1-d) = 0$$

$$\frac{V_o}{V_i} = \frac{(n+1)}{(1-d)}$$

Substituting (18) into (16) results in:

$$V_{L1(OFF)} = -\frac{d}{(1-d)}V_i \quad (12)$$

Switch voltage: Voltage across the switch during OFF time is given by:

$$V_{DS} = -V_{L1(OFF)} + V_i \quad (13)$$

Substituting (19) into (20) results in:

$$V_{DS} = \frac{d}{(1-d)}V_i + V_i$$

$$V_{DS} = \frac{V_i}{(1-d)} \quad (14)$$

Again, the voltage across the clamp capacitor, C1 is nearly constant for the entire switching period. Using (12) and

$$V_{C1} = \frac{d}{(1-d)}V_i \quad (15)$$

Intermediate Capacitor Voltage (*VC2*): The voltage across intermediate energy storage capacitor would be nearly
constant (negligible ripple) and can be determined from (11) as follows:

$$V_{C2} = V_{C1} + V_{L2}$$

By substituting (13) and (23) in (24):

$$V_{C2} = \frac{d}{(1-d)} V_i + nV_i$$

$$V_{C2} = \frac{d(1-n)+n}{(1-d)} V_i \quad (16)$$

Reverse bias voltage across diodes (*VD1, VD2, VD3*):
Voltage across diode (*D1*):

$$V_{D1} = V_{L1(ON)} + V_{C1} \quad (17)$$

By substituting (10) and (23) into (27), the voltage across diode, *D1* becomes:

$$V_{D1} = \frac{V_i}{(1-d)} \quad (18)$$

Voltage across diode (D2) is:

$$V_{D2} = V_{L2} + V_{C2} - V_{C1} \quad (19)$$

By substituting (13), (23) and (26) in (29), it becomes:

$$V_{D2} = 2nV_i \quad (20)$$

Voltage across diode D3:

$$V_{D3} = V_{L2} - V_{C2} - V_i + V_o \quad (21)$$

By substituting the value of *VL2* from (13), Vo from (18) and *VC2* from (26) in (31) yields:

$$V_{D3} = \frac{n}{(1-d)} V_i \quad (22)$$

Magnetizing Inductance (*Lm*):

$$L_m = \frac{1}{2} \times \frac{V_i \times d}{d \times I_{Lm} \times f_s} \quad (23)$$

Forward Bias Diode Currents (*ID1, ID2, ID3*):
Current flow through diode *D1* can be derived as follows:

$$L_1 \frac{dI_{D1}}{dt} = V_{C1}$$

$$I_{D1} = \frac{V_{C1} \times d_{lk}}{L_1 \times f_s} \quad (24)$$

where *dlkTS* is the period during which the leakage energy is transferred. Current flowing through diode *D2* can be calculated as below (S ON):

$$L_2 \frac{dI_m}{dt} = V_{C2} - V_{C1}$$

$$I_m = nI_{L2};\ I_{L2} = I_{D2}$$

$$\therefore \quad I_{D2} = \frac{(V_{C2} - V_{C1}) \times d}{n \times L_2 \times f_s} \quad (25)$$

Similarly, the current flowing through diode *D3* can be calculated as below (S OFF):

$$L_2 \frac{dI_m}{dt} = V_o - V_{C2} - V_i \quad (26)$$

Presence of leakage inductance in the circuit manifests itself in the following manner:

$$V_i = L_m \frac{di}{dt} + L_k \frac{di}{dt} \quad (27)$$

$$i = \int \frac{V_i}{(L_m + L_k)} dt \quad (28)$$

From (38), it is clear that the current flowing through the circuit is reduced if leakage inductance is present.

$$V_{L1} = kV_i \quad (29)$$

$$V_{L1} = knV_i \quad (30)$$

$$\frac{V_o}{V_i} = \frac{(nk+1)+d(k-1)}{(1-d)} \quad (31)$$

IV. Design Example And Experimental Results

An illustrative example for driving the 60 1-W high-brightness LEDs is provided. These light emitting diode (LEDs) are connected in series. The rated voltage and current of each LED are 3.6 V and 0.28 A, respectively. Table I lists the circuit parameter specifications. The input voltage is 110Vrms ±10%. The switching frequency is about 50 kHz at rated power operation. In this design example, both buck and boost converters are designed to operate at discontinuous conduction mode (DCM). The circuit parameters are designed as follows.

Table I: Circuit Specifications

S	FDH055N15A (150V /167 A, $R_{DS(ON)}$ = 4.8mΩ)[2]
D_1 D_2 D_3	BYC20X-600(t_{rr}=35nS) DPG20C300PB (t_{rr}=35nS) CSD01060
C_O	400V/180µF Ceramic caps
C_2	250V/47µF
C_1	63V/1µF
Coupled Inductor	Cosmo ferrite core with L_m=50uH DC resistance Primary=70mΩ DC resistance Secondary=300mΩ

The system specifications of the proposed converter developed in the lab are given in Table-II.

Table II: Specifications of the Laboratory Prototype Converter

Rated Power	400W
Input DC Voltage	25-50V
Output Voltage	(400-500)V
Turns ratio of the coupled Inductor (n)	4
Switching Frequency (f_s)	50kHz

Design Procedure:

For the given input, output specifications, a suitable turns ratio is selected [Table II] and the nominal duty cycle can then be calculated using (18). The value of the magnetizing inductance (*Lm*) can be derived from (10) .

$$L_m = \frac{V_i d}{2\Delta I_m f_s} \quad (32)$$

As the boost converter switch has to bear much higher voltage, a higher voltage switch (MOSFET FCH47N60N, RON=0.068□) is used.

The minimum value of the clamp capacitor *C1* can be derived as follows:

$$C_1 = \frac{I_m d_{1k}}{\Delta V_{C1} f_s} \quad (33)$$

The minimum value of the intermediate capacitor *C2* can be derived as follows:

$$C_2 = \frac{I_m d}{n\Delta V_{C2} f_s} \quad (34)$$

The minimum value of the output capacitor *Co* can be derived as:

$$C_o = \frac{I_o d}{\Delta V_o f_s} \quad (35)$$

The output voltage ripple in (45) includes ripple due to the presence of parasitic resistance of the output capacitor and duration of the holding time during transients of the switch as per the following equation.

$$\Delta V_o = \Delta V_{Co} + r_{co} \quad (36)$$

where, *rco* is the parasitic resistance of the capacitor *Co*. Initially, we don't know the value of *Co*. Hence, it is not possible to determine the value of *rco*. For initial calculation it is assumed that voltage ripple is 1% of *Vo*. The value of output capacitor is derived as below:

$$C_o = \frac{I_o d T_s}{0.01 V_o} \quad (37)$$

$$0.01 V_o = \Delta V_{Co} + r_{co} I_{co}$$

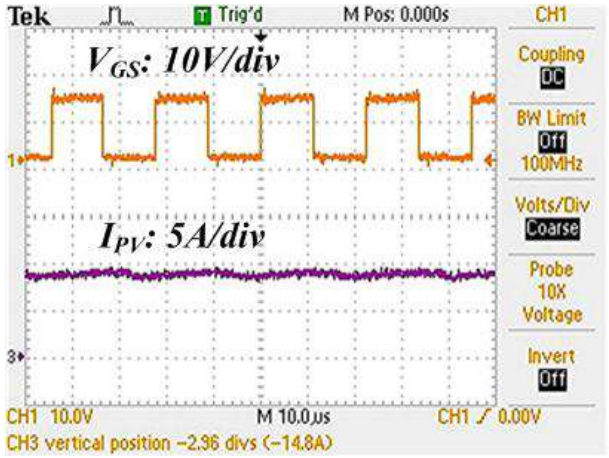
The minimum required value of output capacitance is derived as below:

$$C_{o(min)} = \frac{\Delta I_o x T_s}{0.01 V_o} \quad (38)$$

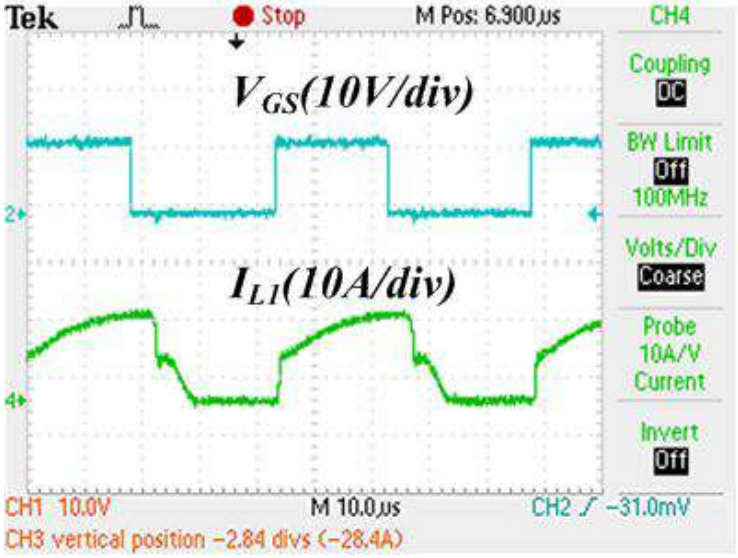
where is the hold-up time for the load transient oft he value of *x* can vary from 10% to 50%.

TABLE III
KEY CIRCUIT VARIABLES AND COMPARISON BETWEEN ANALYTICAL AND HARDWARE RESULTS

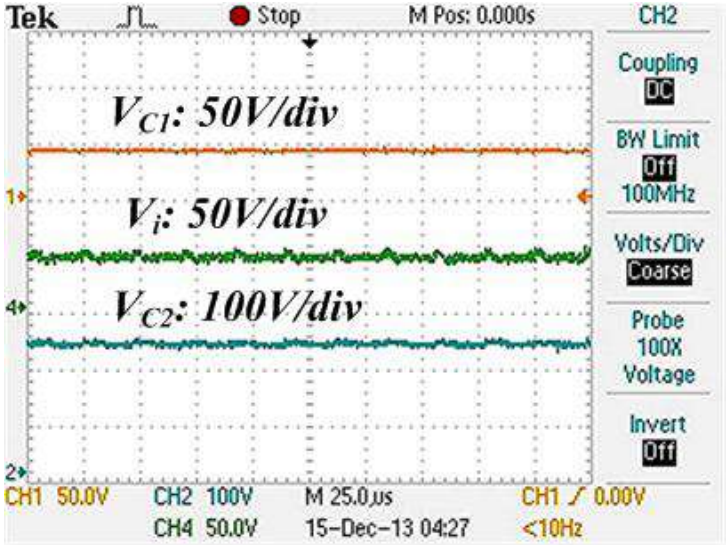
Parameters	Formula	Analytical Results	Hardware Results
Voltage across C_1	$V_{C1} = \frac{d}{(1-d)} V_i$	45V	45V
Voltage across C_2	$V_{C2} = \frac{d(1-n)+n}{(1-d)} V_i$	225V	224V
Reverse voltage across D_1	$V_{D1} = \frac{V_i}{(1-d)}$	90V	87V
Peak current through D_1	$I_{D1} = \frac{V_{C1} \times d_{lk}}{L_1 \times f_s}$	7.2A	7A
Reverse voltage across D_2	$V_{D2} = 2nV_i$	360V	350V
Peak current through D_2	$I_{D2} = \frac{(V_{C2} - V_{C1}) \times d}{n \times L_2 \times f_s}$	2.25	2.5A
Reverse voltage across D_3	$V_{D3} = \frac{n}{(1-d)} V_i$	360V	350V
Peak current through D_3	$I_{D3} = \frac{(V_o - V_{C2} - V_i)(1-d-d_{lk})}{n \times L_2 \times f_s}$	1.75A	1.85A
Reverse voltage across switch S	$V_{DS} = \frac{V_i}{(1-d)}$	90V	87V
Peak Current through L_m	$I_{Lm} = \frac{V_i}{L_m} d T_s$	9A	9.25A
Peak current through L_1	$I_{L1} = \frac{n}{2} I_{Lm}$	18A	18.5A
Value of the magnetizing inductance	$L_m \geq \frac{1}{2} \times \frac{V_i d}{d \times I_L \times f_s}$	$L_m \geq 48\mu H$	$50\mu H$



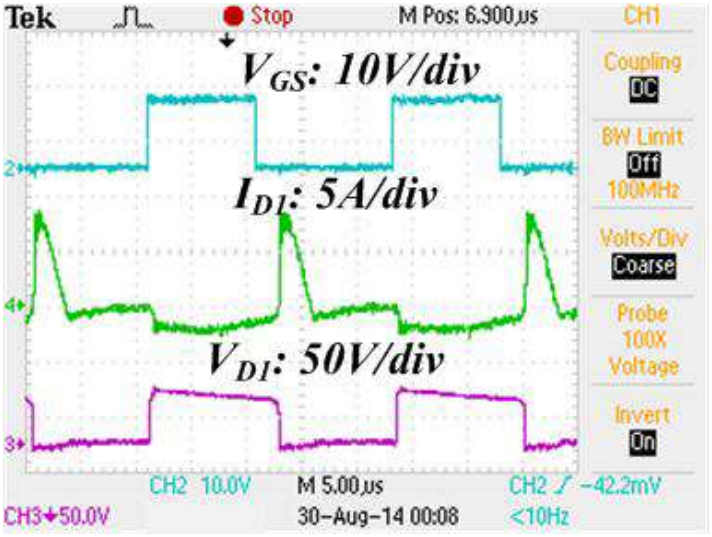
(a)


Tek
Stop
M Pos: 6.900µs
CH4
V_{GS}(10V/div)
I_{L1}(10A/div)
Coupling
DC
BW Limit
Off
100MHz
Volts/Div
Coarse
Probe
10A/V
Current
Invert
Off
CH1 10.0V
M 10.0µs
CH2 ⁄ -31.0mV
CH3 vertical position -2.84 divs (-28.4A)

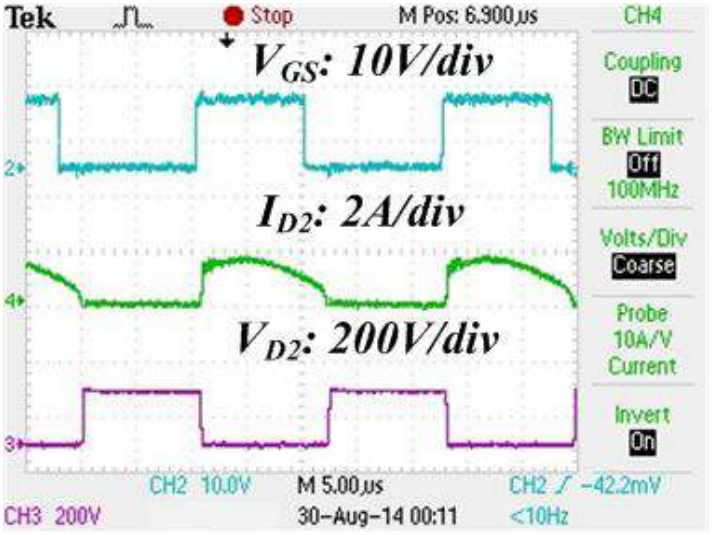
(b)


Tek
Stop
M Pos: 0.000s
CH2
V_{C1}: 50V/div
V_i: 50V/div
V_{C2}: 100V/div
Coupling
DC
BW Limit
Off
100MHz
Volts/Div
Coarse
Probe
100X
Voltage
Invert
Off
CH1 50.0V
CH2 100V
CH4 50.0V
M 25.0µs
15-Dec-13 04:27
CH1 ⁄ 0.00V
<10Hz

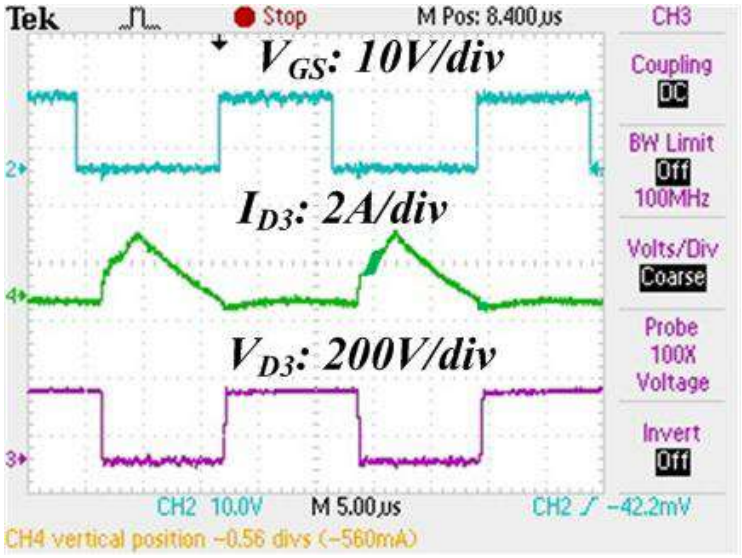
(c)


Tek
Stop
M Pos: 6.900µs
CH1
V_{GS}: 10V/div
I_{D1}: 5A/div
V_{D1}: 50V/div
Coupling
DC
BW Limit
Off
100MHz
Volts/Div
Coarse
Probe
100X
Voltage
Invert
On
CH2 10.0V
CH3 50.0V
M 5.00µs
30-Aug-14 00:08
CH2 ⁄ -42.2mV
<10Hz

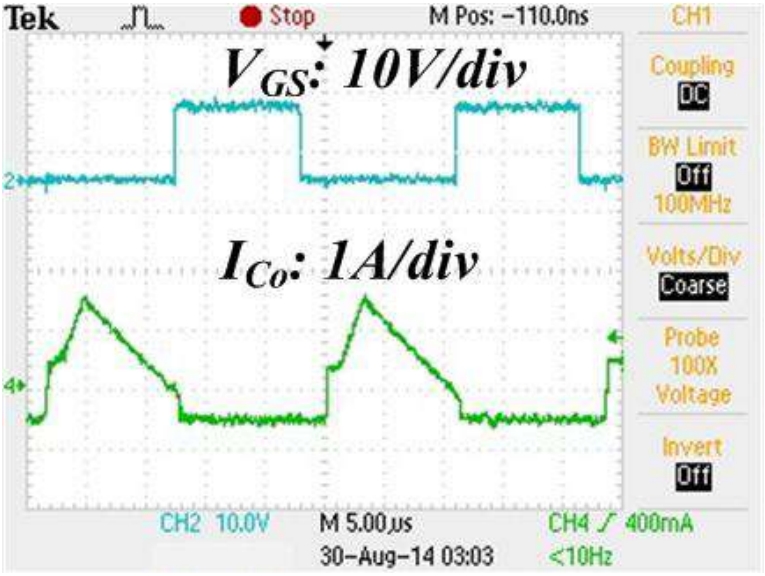
(d)


Tek
Stop
M Pos: 6.300µs
CH4
V_{GS}: 10V/div
I_{D2}: 2A/div
V_{D2}: 200V/div
Coupling
DC
BW Limit
Off
100MHz
Volts/Div
Coarse
Probe
10A/V
Current
Invert
On
CH2 10.0V
M 5.00µs
CH2 ∕ -42.2mV
CH3 200V
30-Aug-14 00:11
<10Hz

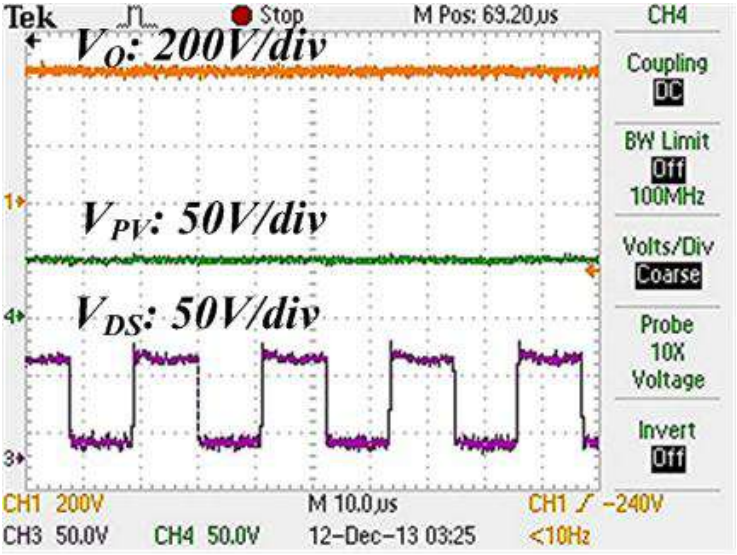
(e)


Tek
Stop
M Pos: 8.400µs
CH3
V_{GS}: 10V/div
I_{D3}: 2A/div
V_{D3}: 200V/div
Coupling
DC
BW Limit
Off
100MHz
Volts/Div
Coarse
Probe
100X
Voltage
Invert
Off
CH2 10.0V
M 5.00µs
CH2 ∕ -42.2mV
CH4 vertical position -0.56 divs (-560mA)

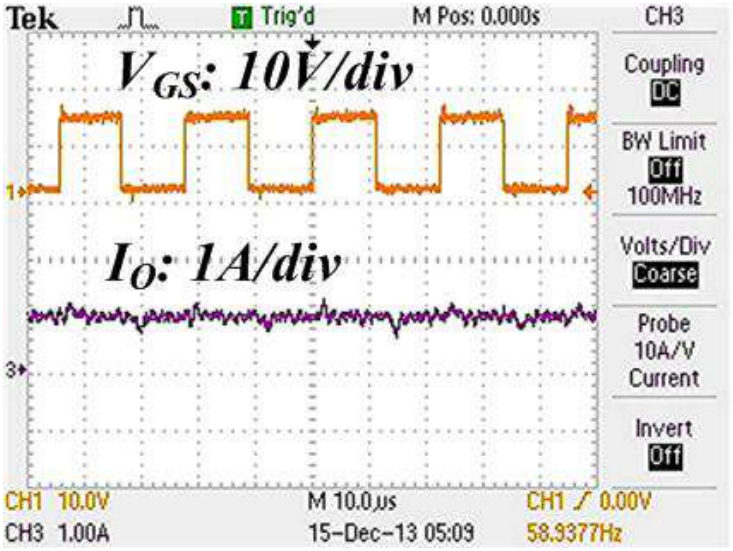
(f)


Tek
Stop
M Pos: -110.0ns
CH1
V_{GS}: 10V/div
I_{Co}: 1A/div
Coupling
DC
BW Limit
Off
100MHz
Volts/Div
Coarse
Probe
100X
Voltage
Invert
Off
CH2 10.0V
M 5.00µs
CH4 ∕ 400mA
30-Aug-14 03:03
<10Hz

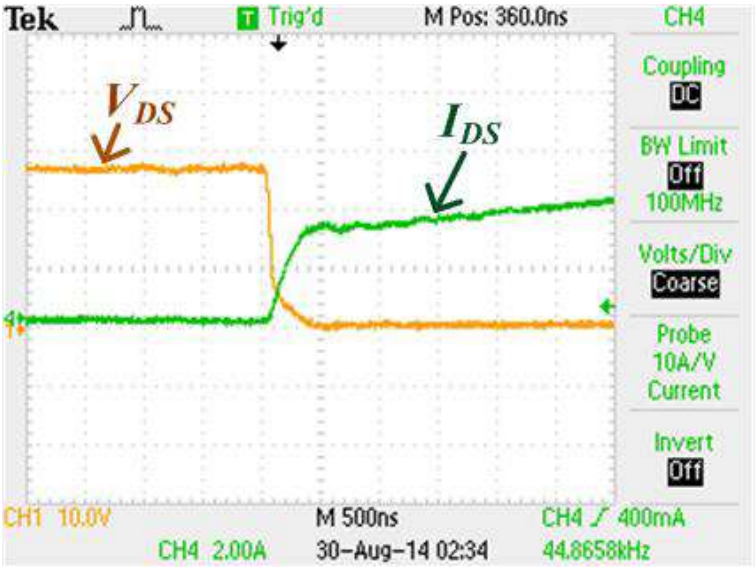
(g)


Tek
Stop
M Pos: 69.20µs
CH4
V_O: 200V/div
V_{PV}: 50V/div
V_{DS}: 50V/div
Coupling
DC
BW Limit
Off
100MHz
Volts/Div
Coarse
Probe
10X
Voltage
Invert
Off
CH1 200V
M 10.0µs
CH1 ∫ -240V
CH3 50.0V
CH4 50.0V
12-Dec-13 03:25
<10Hz

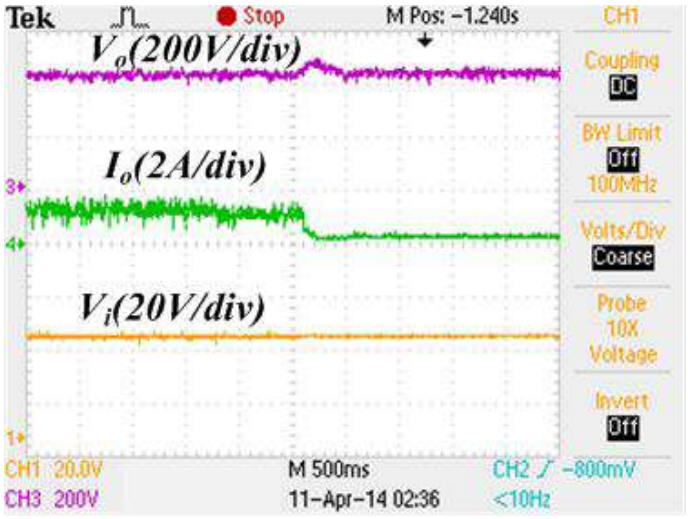
(h)


Tek
Trig'd
M Pos: 0.000s
CH3
V_{GS}: 10V/div
I_O: 1A/div
Coupling
DC
BW Limit
Off
100MHz
Volts/Div
Coarse
Probe
10A/V
Current
Invert
Off
CH1 10.0V
M 10.0µs
CH1 ∫ 0.00V
CH3 1.00A
15-Dec-13 05:09
58.9377Hz

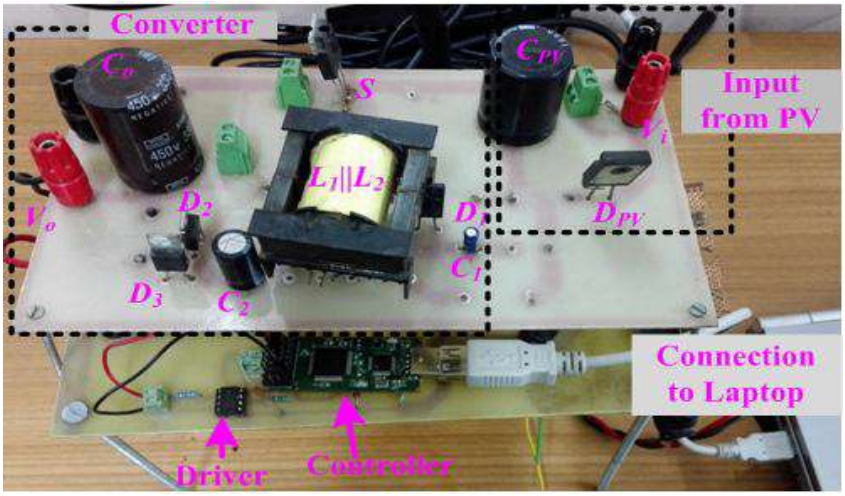
(i)


Tek
Trig'd
M Pos: 360.0ns
CH4
V_{DS}
I_{DS}
Coupling
DC
BW Limit
Off
100MHz
Volts/Div
Coarse
Probe
10A/V
Current
Invert
Off
CH1 10.0V
M 500ns
CH4 ∫ 400mA
CH4 2.00A
30-Aug-14 02:34
44.8658kHz

(a)



(b)



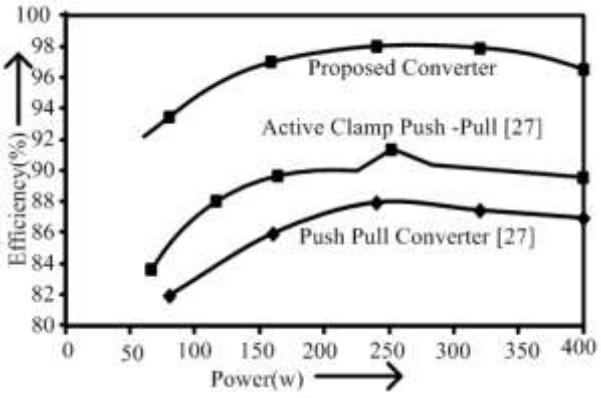
(c)

All the voltage and current values are derived and calculated in Table III. Those values can be used for the selection of suitable MOSFET and diodes. The key circuit variables of the proposed converter prototype along with their expressions are given in Table III. For analytical calculations given in column 3 of Table III, *d=0.5*, *Vi=45V*, *n=4* and *fs=50kHz* have been used. The hardware results shown in column 4 are for CCM operation and compare well with the steady state analytical calculations [column The experimental waveforms are shown in Fig. 6. These are the measured waveforms under full load (400W) conditions with MPPT. A 'TerraSAS' PV simulator is used as the PV source. For a given radiation level, the current drawn from the input PV source is nearly constant as shown in Fig. 6(a). The current flowing through primary of coupled inductor (*L1*) is shown in Fig. 6(b). The voltage across clamp capacitor (*C1*) and intermediate capacitor (*C2*) with input buffer capacitor across PV are also nearly constant as shown in Fig. 6(c).The current and voltage waveforms of the clamp diode *D1* are shown in Fig. 6(d), which match with typical waveform *ID1* shown in Fig. 5(h). The current and voltage of intermediate diode *D2* are shown in Fig. 6(e), which compare reasonably well with Fig. 5(d). The current and voltage waveforms of the output diode (*D3*) are shown in Fig. 6(f). The nature of current through the output filter capacitor is shown in Fig. 6(g), which compares well with the typical simulation waveform shown in Fig. 5(g). According to the calculation *VDS* is □80V for a 450V output voltage, which matches closely with Fig. 6(h). The output current of the converter is shown in Fig. 6(i). An interesting benefit of the proposed converter is that it incurs "low loss switching" during turn ON, without any extra circuit arrangement. The leakage energy is recycled by the passive clamp circuit. So, the current flowing through the switch starts from zero during turn ON. Experimental verification of low loss switching feature of the proposed converter is depicted in Fig. 7(a), which makes turn-ON losses almost zero. The result shown in Fig. 7(b) is for a load step down from 400W to 40W, to show transient stability of the converter. The output voltage of the converter is stable even with the change of load from 100% to 10%. A picture of the experimental prototype is

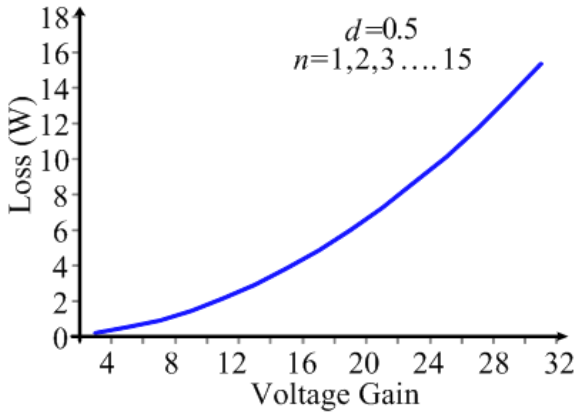
shown in Fig. 7(c). Efficiency plot with respect to load variation of the proposed converter is shown in Fig. 8(i). The efficiency plot of the proposed converter is compared with conventional push-pull converter having identical inputoutput voltage ratings (Vi=40V; Vo=400V) and operating frequency (50kHz). Full load (400W) efficiency of the converter, obtained from experimentation, is 96% (maximum ☐97% at lighter load). A comparison is also shown with conventional, hard switched push pull converter (of identical rating, operating frequency and input/output voltage specifications) with and without active clamp across the main switch. The proposed system shows a higher efficiency under all load conditions. Fig. 8(ii) shows a plot of gain versus losses by varying the turns ratio of the coupled inductor while duty cycle of the dc-dc converter is held constant at 0.5. Fig. 8(iii) shows the gain versus loss curve as the duty cycle of the dc-dc converter is varied (with turns ratio of the coupled inductor held constant at 4).

V. Conclusions

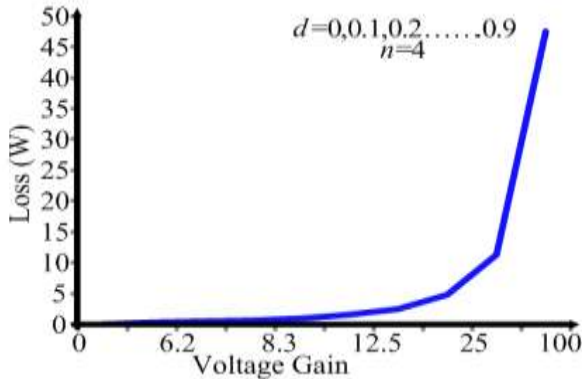
The high gain, high efficiency converter proposed in this paper is highly suitable for low output voltage sources (e.g. solar PV, Fuel Cell Stack, Battery).



(i)



(ii)



(iii)

Fig. 8 (i) Efficiency versus load curve for the proposed dc-dc converter and comparison with existing versions; (ii) Loss versus gain plot by varying
voltage gain with the variation of turns ratio (*n*), keeping duty cycle (*d*) constant; (iii) Loss versus gain plot by varying voltage gain with the variation
of *d*, keeping *n* constant.

A circuit efficiency of 96% is achieved under full load conditions. Table III provides a comparison of the key circuit variables values obtained analytically with hardware measurements. The error in the results between analytical derivation and experimental results [Fig. 6] is found to be between 0 to 5%. This could be attributed to measurement errors, presence of parasitics and use of imprecise values of circuit components for experimentation. The trend shown in the plots of Figs. 8(ii) and 8(iii) suggests that a good way to design and use the proposed converter would be to use turns ratio of the inductor around 4 or 5 (fixed during the design) and vary the duty ratio from 0 to 0.7 while operating. Beyond this range of duty cycle and turns ratio, the losses become significantly higher. High voltage gain is achieved without using extreme duty cycle values, which is
a big advantage over conventional step-up converters. One of the reasons for high efficiency in the proposed converter is reduction in the switching loss during turn-on due to low loss switching. Table IV provides a comparison of the key circuit parameters of a conventional boost converter with proposed high gain converter for identical applications and
specifications. Looking at these numbers, the superior performance of the proposed converter is quite evident. The Euro efficiency and CEC efficiency [28] for the proposed converter are obtained as follows: Euro Efficiency = (0.03×90% + 0.06×93% + 0.13×95% + 0.1×96% + 0.48×97%+ 0.2×96%) = 96%
CEC Efficiency = (0.04×90% + 0.05×93%+ 0.12×95% + 0.21× 96% + 0.53× 97% + 0.05× 96%) = 96.02%.

TABLE IV
COMPARISON WITH CONVENTIONAL BOOST CONVERTER

	Boost Converter ($d=0.9, V_i=45V, f_s=50kHz$, MOSFET FCH47N60N, $R_{ON}=0.068\Omega$, $L=50uH$, $C=4.7uF$)	Proposed Converter ($d=0.5, f_s=50kHz$, $V_i=45V$, $n=4$, MOSFET FDB86135, $R_{ON}=0.0035\Omega$, $L=50uH$, $C=4.7uF$)
Voltage gain	$\frac{V_o}{V_i}=\frac{1}{(1-d)} \Rightarrow 450V$	$\frac{V_o}{V_i}=\frac{(n+1)}{(1-d)} \Rightarrow 450V$
Switch loss	$R_{ON_{sw}} \times d \times \left(\frac{I_{out}}{(1-d)}\right)^2 \Rightarrow 6.12W$	$R_{ON_{sw}} \times d \times \left(\frac{(n+1)}{(1-d)} I_{out}\right)^2 \Rightarrow 0.18W$
Inductor loss	$r_L \times \left(\frac{I_{out}}{(1-d)}\right)^2 \Rightarrow 100r_L$	$r_L \times \left(\frac{(n+1)}{(1-d)} I_{out}\right)^2 \Rightarrow 100r_L$
Switch voltage drop(V_{DS})	$\frac{V_i}{(1-d)} \Rightarrow 450V$	$\frac{V_i}{(1-d)} \Rightarrow 90V$
Current through Inductor	$\frac{V_i}{L} dT_s \Rightarrow 18A$	$\frac{V_i}{L} dT_s \Rightarrow 9A$
Leakage energy $C = C_{snubber}$	$\frac{1}{2} C \left(\frac{V_i}{(1-d)} d\right)^2 \Rightarrow 0.38W$	$\frac{1}{2} C \left(\frac{V_i}{(1-d)} d\right)^2 \Rightarrow 0.004W$
Switch current	$I_{sw} = I_L = I_{in} \Rightarrow 18A$	$I_{sw} = I_L = (I_{in} - \frac{I_{L2}}{n}) \Rightarrow 9A$

References

[1]. E. Mamarelis, G. Petrone, G. Spagnuolo, "Design of a Sliding-Mode- Controlled SEPIC for PV MPPT Applications," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3387-3398, July 2014.

[2]. K. W. Ma and Y. S. Lee, "An integrated fly-back converter for dc uninterruptible power supply," *IEEE Trans. Power Electron.*, vol. 11, pp. 318–327, March 1996

[3]. C. T. Pan, C. F. Chuang and C. C. Chu "A Novel Transformer-less Adaptable Voltage Quadrupler DC Converter with Low Switch Voltage Stress", *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4787-4796, Sept. 2014.

[4]. J. H. Lee, T. J. Liang and J. F. Chen, "Isolated Coupled-Inductor- Integrated DC–DC Converter With Nondissipative Snubber for Solar Energy Applications," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3337 3348, July 2014.

[5]. J. Xu, "Modeling and analysis of switching DC-DC converter with coupled-inductor," in *Proc. IEEE CICC*, pp. 717-720, 12-15 May 1991.

[6]. C. M. Young, M. H. Chen, T. A. Chang, C. C. Ko and K. K. Jen, "Cascade Cockcroft–Walton Voltage Multiplier Applied to Transformerless High Step-Up DC–DC Converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 2, pp. 523-537, Feb. 2013.

[7]. A. Ioinovici, Power Electronics and Energy Conversion Systems, Vol. 1, Wiley 2013.

[8]. J. C. Hung, T. F. Wu, J. Z. Tsai, C. T. Tsai and Y. M. Chen, "An active-clamp push-pull converter for battery sourcing applications," in *Proc. IEEE APEC*, vol. 2, pp.1186-1192, Mar. 2005.

[9]. B. Brooks and C. Whitaker, *Guideline for the Use of the Performance Test Protocol for Evaluating Inverters Used in Grid-Connected Photovoltaic Systems*, Tech. Rep., KEMA-Xenergy and BEW Engineering, Feb. 25, 2005.

[10]. Marian K. Kazimierczuk, Pulse-width Modulated DC-DC Power Converters, 1st-ed, John Wiley & Sons, 2008.