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Design of Event Driven 8- bit Processor using VHDL

[1]Prajakta A. Satpute, [2]Dr. AmolMorankar, [3]Dr. Vibha Bora
[1]PG Scholar, Department of Electronics Engineering, G. H. Raisoni College of Engineering, Nagpur, Maharashtra, India.
[2]Managing Director , Riva Labs Pvt. Ltd, Nagpur, Maharashtra, India.
[3]Head, Department of Electronics Engineering, G. H. Raisoni College of Engineering, Nagpur,Maharashtra, India.
Corresponding Author: Prajakta A. Satpute

Abstract:*During this modern era, Each and every customer desires a style that suits their need. Hence, choosing acceptable processor and supporting peripherals is becoming really vital. In Reduced Instruction set Computing (RISC) most instructions are present in internal memory. This helps us to improves performance of processor. This paper presents associate degree implementation of Event Driven 8-bit Reduce Instruction Set Computer Processor with single interrupt capability that works on 375.038 MHz with delay of 2.66 ns.*

Keywords:*Very High Speed Integrated Circuit Hardware Description Language (VHDL),Reduced Instruction set Computing (RISC), Arithmetic and Logical Unit(ALU), Register Transfer Logic(RTL).*

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I. Introduction

Innovations in electronics is updating at a really fast rate in this modern era. Market is turning towards more and more client based only. Clients desire different styles of system to suit their requirement; this can be a golf stroke a lot of stress on embedded system designer. Selecting appropriate processor and its peripherals is turning into terribly troublesome. Considering this growth in VLSI style, therefore the day is no any longer when people will start designing their own processor.

A trend is towards development in design of RISC processor that's economical for specific application. Performance is the main criteria for bobbing up with such processor. Reduced Instruction set Computer Processor uses simplified instructions for higher performance with quicker execution of instruction. It reduces the delay in execution. It conjointlyuses general instructions rather than specialized instructions. They are less expensive to vogue and are most cost-effective to vogue, test and manufacture. This has created a major advantage in implementation of reduced instruction set computer in technological field. Reduce Instruction set Computer processor operates on mainly on data interpretations and on the direct parallel forwardedoperations. It supports only several addressing modes and is sometimes register based. Most of the operations are executed in the given data present in internal registers conjointly instruction length is fastened and hence decoding is easier.

The selected project is aiming towards the planning of an 8-bit data Reduce Instruction Set Computer (RISC) processor. It comprises several blocks of execution like a 256 instruction set, program and data memories, program counter, flag register; interrupt structure and a simple Arithmetic Logical Unit (ALU) for basic operations. Throughout this design all the instructions are of uniform length and similar architecture. The processor relies on single interrupt and single clock at the side of 10-bit address bus and 8-bit information bus. Control Unit generates signals for the chosen direction to support Arithmetic, Logical, Branching, Interrupt control. The contents of this paper are as follows. Section II explains the design details of 8-bit RISC processor. Section III presents the planning of module of ALU, Data Memory, Program Memory, Control Unit and Program Counter. Section IV presents the simulation result and at last the ultimatesection presents the conclusion.

II. Architecture of 8-Bit RISC Processor

The design of 8-bit processor is shown in figure (1). The projected style consists of arithmetic and logical unit, Control Unit, Comparator, Internal Interrupt structure, Program Counter, Flag register. The processor consist load/store (Von Neumann) design. There are two memory programand data memory along with one address bus and data bus between processor and memory. No pipelining is usedin whole processor and every instruction is executed on single clock that increase the speed of operation of the processor.The control unit reads the op-code and instruction bits and then creates control signals as outputs that track the information path to perform the specific task.

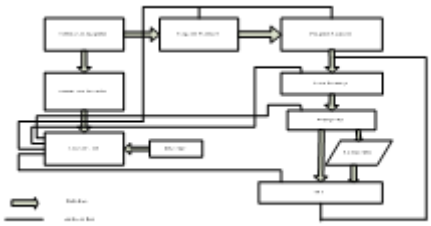

Figure 1: Architecture of 8-bit RISC Processor

The operands are received from source and destination and result keeps in destination. All the operations are register based mostly data transfer from register to register. Looking on the management signal from the control unit the ALU performs either arithmetic or logical operations. Input is taken form register A and register B and conjointly the operation is done based on the control lines activated by control unit.Once, the execution of the instruction is completed, the result's is stored in the source register

III. Module Design of 8-Bit RISC Processor

This section presents the design of different modules likes Arithmetic Logical Unit, Data Memory, Program Memory Control Unit and Program Counter.

A. Arithmetic Logical Unit:

ALU is vogue to perform a pair of operations. One unit is meant for logical operation containing AND, OR, NOT and XOR and therefore the other unit is meant for arithmetic operations like ADD, ADD by 1, SUB, SUB by 1. The Arithmetic and logical unit is of 8-bit with 8 operations to perform. The RTL View is shown in Figure (3.1) and therefore the simulation result is shown in Figure (3.1.1).

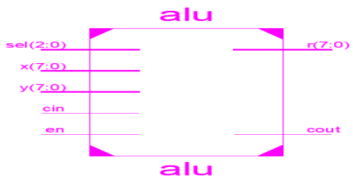

Figure 3.1: RTL View of Arithmetic and logical unit

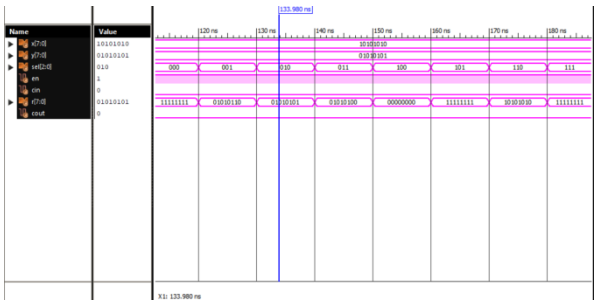

Figure 3.1.1 Timing Diagram of Arithmetic and logical unit

B. Data Memory:

It is used for temporarily storing and keeping intermediate result includes 32 8-bit registers. It consists of 32 D- flip flops and 32 AND gates. Initially RESET is about to high to clear the register. Taking RESET as low and CLOCK as High to low and READ as high the information is hold on within the register. Taking RESET as low and CLOCK as High to low and WRITE as high the information is written within the memory. The RTL View is pictured in Figure (3.2) and therefore the timing waveform is shown in Figure (3.2.1).

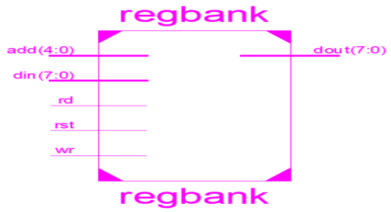

Figure 3.2: RTL View of Data Memory

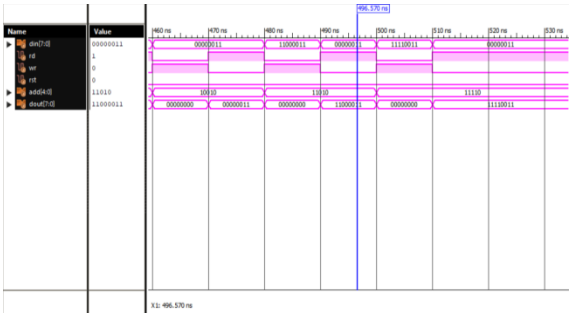

Figure 3.2.1 Timing Diagram of Data Memory

C. Program Memory:

The memory size is of 1024 kb. Associate instruction memory is employed for storing the data to be executed. Initially RESET is set to high to clear the register. Taking RESET as low and clock as high to low and READ as high the information is hold on within the register. The Figure (3.3) shows the top block of program memory and simulation result using Xilinx tool is shown in Figure (3.3.1).

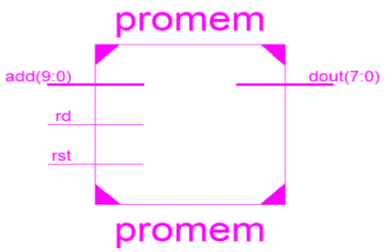

Figure 3.3: RTL View of Program Memory

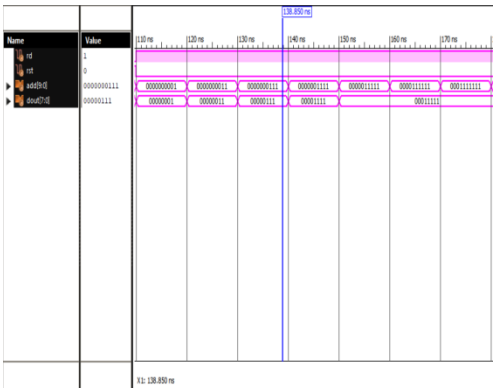

Figure 3.3.1: Timing Diagram of Program Memory

D. Control Unit:

The control unit of the Reduced Instruction Set Computer processor reads the instruction op-code and decodes the instruction to produce 14-control signals to use within the remaining module. The signal dmr ,pmr, dmw accustomed read and write the data from data memory and program memory. The operation jump, call,

returns control signal used to selects the jump, call, and return address into PC. ALU result and ALU select signal employed to work out with the ALU performance. The RTL View and simulation result is diagrammatic in Figure (3.4) and Figure (3.4.1).

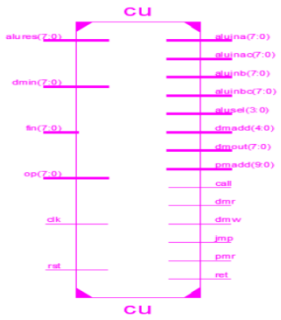

Figure 3.4: RTL View of Control Unit

E. Program Counter:

Program Counter contains address of the instruction being executed. It's accustomed increment the address once each execution. The program counter vogue consists of MUX and D flip flop. The value of the program counter is initializing to 0000011111. Prime block of program counter is shown in Figure (3.5) and simulated timing waveform in Figure (3.5.1).

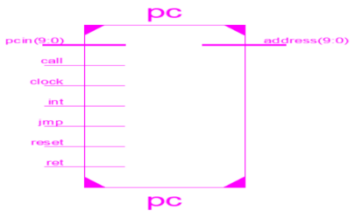

Figure 3.5: RTL View of Program Counter

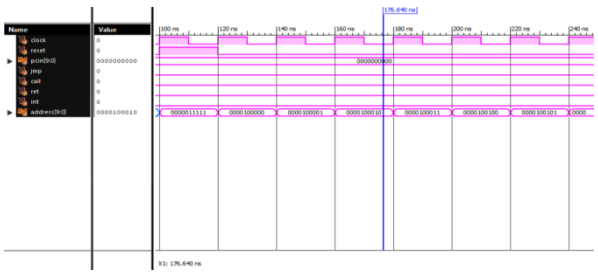

Figure 3.5.1: Timing Diagram of Program Counter

IV. Simulation Result

The projected processor is simulated using VHDL and synthesized using Xilinx ISE 14.7. For simulation place a piece of code on to the program memory and perform the simulation and verify the operations. Figure 4.1 shows the movement of the instruction MOV R0, R2 and figure 4.2 shows the movement of instruction LDA 01H.

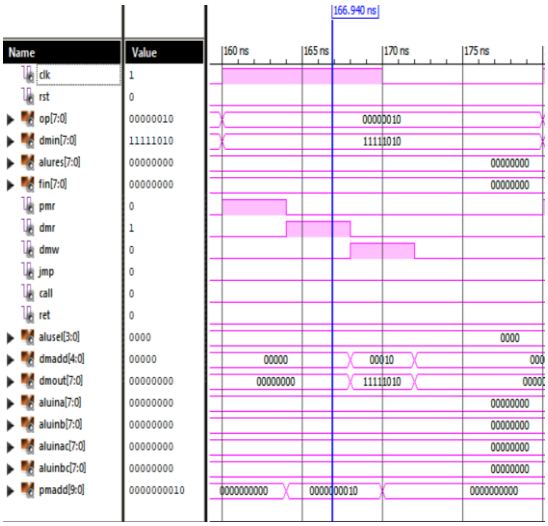

Figure 4.1: Instruction MOV R0, R2

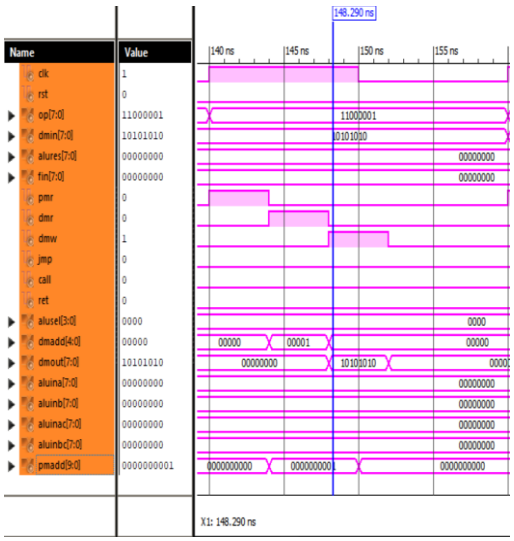

Figure 4.2: Instruction LDA 01H

The projected processor is synthesized mistreatment Xilinx ISE 14.7 software. Figure 5 shows the Register Transfer Level (RTL) read of projected processor. Table 1 shows the device utilization of the planned processor.

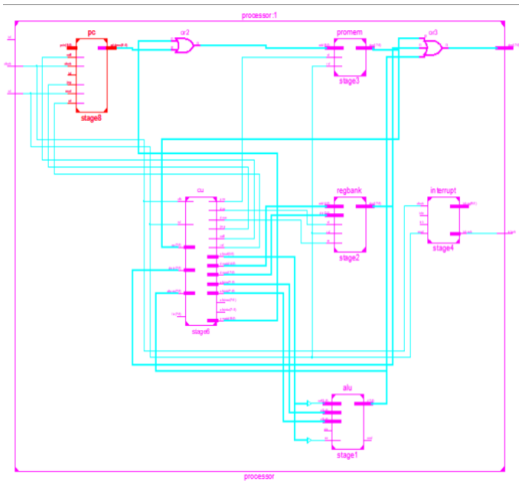

Figure 5: RTL View of proposed processor

Table 1: Device Utilization

Parameter	Utilization
No. of Slice Register	17/82000(0%)
No. of Slice LUT's	14/41000(0%)
4 Input LUT's	12/19(63%)
No. of Bonded TOB's	11/285(3%)

V. Conclusion

RISC processor has design an implemented on Xilinx ISE 14.7. An 8-bit Reduced Instruction Set Computer processor with 256 instruction set has been designed. Each instruction is executed in one clock cycle. The processor achieves higher. The processor support 9-bit address line, 8-bit data line with the frequency of 375.038 MHz, with delay of 2.66 ns. The application of planned processor is that it is employed in car and Automation Systems.

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