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Computation and Confirmation of Conduction Band Offset and Oxide Breakdown Fields from a Combination of Electrical and Physical Measurements on a N-Type C-Face 4H-SiC MOS Device

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Abstract: *This article combines electrical and physical measurements to obtain and confirm the conduction band offset and the oxide breakdown field in a MOS device fabricated on the n-type C-face of 4H-SiC having (000-1) orientation. The device has the oxide grown by wet oxidation and wet re-oxidised in steam at 500^oC to 1000^oC for 10 min. The conduction band offset obtained is 2.92 eV relative to the SiO_2 conduction band and is 0.14 eV larger than on the Si-face where it is determined earlier to be 2.78 eV. The oxide breakdown field at a current density of $10^{-4} A/cm^2$ with charges is a low value of 6.22 MV/cm and without charges is 8.24 MV/cm when having the MOS device in accumulation. The higher CBO on the carbon face is confirmed by observing the difference of Si-2p core electron peaks by XPS on the Si-face and C- face oxidised 4H-SiC. This experiment is performed by another research group. A 1-D double-well potential energy function for the electrons in the Si-C bond of 4H-SiC computed by density functional theory also corroborates this energy difference of 0.14 eV.*
Keywords: *Band Offset, Oxide breakdown field, Silicon Carbide, metal-oxide-semiconductor, XPS*

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I. Introduction

4H-SiC (0001) and (000-1) oriented Si- and C-face semiconductor is suitable for high temperature power electronics [1]. Power Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFETs) have been fabricated on both Si-face and C-face that exhibit average surface field effect mobility of about $35 cm^2/V\text{-}s$ [2-3]. The C-face 4H-SiC having (000-1) oriented surface is also used to grow Graphene layers by high temperature vacuum annealing [4-5]. Graphene which was shown to have a high mobility of up to 10000 $cm^2/V\text{-}s$ by Novoselov, Geim (both Nobel laureates) and co-workers [6] can behave as a electronic semiconducting material in the bilayer form having a bandgap that can be tuned up to 250meV by the application of voltage [7]. It has been shown to posses 2-6 times higher electron saturation velocity than in Si [8]. Therefore Graphene can be used to fabricate high frequency and low power MOSFET devices giving a higher unity gain cut-off frequency (f_T) than Si-MOSFET for the MOSFET having the same channel length. The f_T is given by ($v_s/2\pi L$) where v_s is the saturation velocity of electrons and L is the channel length [9].

In this article, the conduction band offset (CBO) in the MOS device fabricated on the C-face of n-4H-SiC has been determined using the slope constant of the Fowler-Nordheim electron tunnelling from the cathode of the MOS device in accumulation. The CBO on the Si-face of the n-type MOS device has already been determined to be 2.78 eV [10-11] and confirmed by other research groups [12-15]. The CBO on the C-face is 0.14 eV more at 2.92 eV which has been confirmed by observing the difference in the peaks of binding energy of Si-2p core electrons on oxidised Si-face and C-face by X-Ray Photoelectron Spectroscopy (XPS) measurements performed in the study by Watanabe and Hosoi [16] and shown in Fig. 4 of the reference. The figure shows about a 0.15 eV larger binding energy on the C-face of oxidised 4H-SiC meaning that the valence band is about 0.15 eV lower on the C-face.

II. Theory

Fowler-Nordheim (FN) electron and hole tunnelling has been observed in Si and SiC MOS devices and in organic light emitting diodes [10, 11, 17-22]. The FN equation models the current-voltage characteristics across a MOS device in accumulation at high fields. It is given by the classical equation [10]:

$$J = AE_{ox}^{2} \exp\left(\frac{-B}{E_{ox}}\right) \qquad (1)$$

where J is the current density through the MOS device in accumulation in A/cm^2, E_{ox} is the oxide electric field in V/cm and the pre-exponent A and the slope constant B are given by:

$$A = \frac{e^3 m}{16\pi^2 \hbar m_{ox} \phi_0} \qquad (2)$$

$$A = 1.54x10^{-6} \frac{m}{m_{ox}} \frac{1}{\phi_0} \qquad (A/V^2)$$

$$B = \frac{4}{3} \frac{(2m_{ox})^{1/2}}{e\hbar} \phi_0^{3/2} \qquad (3)$$

$$B = 6.83x10^7 \left(\frac{m_{ox}}{m}\right)^{1/2} \phi_0^{3/2} \qquad (V/cm)$$

In A and B, e is the electronic charge, m is the free electron mass, m_{ox} is the electron or hole mass in the oxide, $\hbar$ is the Planck's constant and ϕ_0 is the electron or hole barrier height expressed in electron volts. A plot of ln (J/E_{ox}^2) versus $1/E_{ox}$ called the FN plot, gives the value of the slope constant B, from which $(m_{ox}/m)^{1/2}\phi_0^{3/2}$ product can be obtained. Then, with a known effective mass, ϕ_0 can be calculated and with a known ϕ_0, the effective mass can be calculated. The slope constant B is very sensitive to the oxide field as it is in the exponential and therefore precise determination of the oxide field is decisive in the evaluation of the tunneling parameters. The ln (J/E_{ox}^2) term is relatively less sensitive to the oxide field as it is in the natural logarithm. The slope constant B can be independently used to determine the carrier effective masses, band offsets at the insulator/semiconductor interface and the unknown bandgap of the amorphous insulators and possibly wide bandgap crystalline semiconductors such as hex-BN and AlN having a bandgap of 6.2 eV, without the knowledge of band offsets from the photoemission spectroscopic measurements [11, 23]. It is to be noted that ϕ_0 and ϕ_0 mean the same thing as 'barrier height'

A. Calculation of the slope constant

The slope constant B is given in equation (3) above. It is determined from the I-V characteristics using equation (1). The $\Delta\ln(J/E_{ox}^2)$ versus $\Delta(1/E_{ox})$ is determined by taking at least two points on the I-V characteristics in the high field FN region with the oxide voltage corrected for the flatband voltage [11]. It can be observed that $\Delta\ln(J/E_{ox}^2)$ can be evaluated as $\Delta\ln(I/V^2)$ in the numerator without causing any error. This means that the area of the device can be ignored. However, the oxide thickness needs to be exact as it appears in the Δ (1/E) term in the denominator. A report highlights the importance of exact oxide thickness [24]. In the second method of computing the CBO which is described below, the precise area of the C-V dot is also necessary.

B. Calculation of the flatband voltage

The flatband voltage V_{fb}, is calculated based on the formula developed by Jakubowski and Iniewski for the Si technology [25]. It has been used by the author in his earlier studies on Si-MOS device [26]. The formula is presented below for convenience, where first the normalized Fermi potential u_F is calculated as:

$$u_F = 1.167 + 2.174 \ln\left(\frac{C_i C_{min}}{C_i - C_{min}} \frac{1}{A}\right) \qquad (4)$$

Here, C_i is the insulator (oxide) capacitance with the MOS device in accumulation, C_{min} is the minimum capacitance of the MOS device with the semiconductor in strong inversion, and A is the area in mm^2. The C_i and C_{min} capacitances are in pF. Since the 4H-SiC MOS device undergoes deep depletion at room temperature due to the low generation rate of minority carriers, and therefore the C_{min} is taken at the onset of deep depletion during a high frequency (1MHz) C-V trace. Next, the flatband capacitance C_{fb} is calculated using the formula:

$$\frac{C_{fb}}{C_i} = \frac{1}{\frac{1}{2.06\sqrt{u_F}}\left(\frac{C_i}{C_{min}} - 1\right) + 1} \qquad (5)$$

From the flatband capacitance, the flatband voltage is seen on the voltage axis of the high frequency C-V plot.

III. Results and Discussion

A. MOS device data

The n-4H-SiC/SiO_2/Al MOS device data is described in the author's collaborative study with Prof. M. E. Zvanut [27]. The device was fabricated on the C-face of the (000-1) oriented 4H-SiC surface. In this study, an ac conductance measurement system was configured along with the I-V/C-V measurement system. These systems provide the I-V/ C-V data for the present study as well [27].

B. Calculation of the flatband voltage

For the MOS device under study [27], C_i = 235 pF, C_{min} = 115 pF, A = 0.50 mm^2, u_F =14.45, $C_{fb} = 0.88C_i$ = 207 pF, resulting in the flatband voltage of 16 V that indicates negative charges in the oxide.

C. Determination of the CBO in the MOS device fabricated on the C-face of the 4H-SiC.

Method 1

Two points on the I-V curve in the high field region where V_1 and V_2 are cathode voltages in volts and I_1 and I_2 are currents in Amperes (A) through the n-MOS device in accumulation, are [27]:

$(V_1, I_1) = (-30, 10^{-10})$
$(V_2, I_2) = (-50, 10^{-5})$

After correcting the cathode voltages (negative) for the positive flatband voltage of 16 V (negative charges present), the two points become [11, 23]:

$(V_1-V_{fb}, I_1) = (-46, 10^{-10})$
$(V_2-V_{fb}, I_2) = (-66, 10^{-5})$

The average oxide thickness, d = 74 nm.
E_{ox1} = 46/7.4 = 6.22 MV/cm, $1/E_{ox1}$ = 0.161 cm/MV
E_{ox2} = 66/7.4 = 8.92 MV/cm, $1/E_{ox2}$ = 0.112 cm/MV
Delta $(1/E_{ox1}-1/E_{ox2})$ = 0.049 cm/MV
1/ (Delta $(1/E_{ox1}-1/E_{ox2})$) = 20.41 MV/cm.
Delta (ln (I/E_{ox}^2) = -26.68-(-15.89) = -10.79
The slope constant B = Delta (ln (I/E_{ox}^2))/ Delta $(1/E_{ox})$ = 20.41 x 10.79 = 220.22 MV/cm

$B = 68.3 \times (0.42)^{1/2} \phi_0^{3/2} = 220.22$; $\phi_0^{3/2} = 220.22 / (68.3 \times 0.648) = 4.976$; $\phi_0 = (4.976)^{2/3} = 2.915$ or 2.92eV.

Here, 0.42 is the relative electron effective mass in the thermal oxide. So, the CBO of the C-face 4H-SiC MOS device equals 2.92 eV. It is to be noted that the area of the C-V dot does not affect the results, but the thickness of the oxide will affect the results. Therefore, the thickness of the oxide has to be accurate. Also, the slope ideally should be calculated from the Fowler-Nordheim plot which is delta $(\ln(J/E_{ox}^2))$ versus delta $(1/E_{ox})$ plot, where 'delta' represents 'change in value'. The CBO of the Si-face 4H-SiC MOS device is 2.78 eV [10-11]. The difference in the two CBOs is equal to 2.92-2.78 = 0.14 eV

Method 2

The C-V dot having a diameter of 0.8 mm gives a dot area of 0.50 mm^2 or 5 x 10^{-3} cm^2.
The low field current at the onset of FN tunnelling of electrons from the cathode of the n-MOS device in accumulation is 10^{-10} A or a current density of 2×10^{-8} A/cm^2. The onset electric field after correcting for the flatband voltage of 16 V is 46/7.4 =6.22 MV/cm for a oxide thickness of 74 nm after re-oxidation in steam at 1000°C for 10 min where 6 nm oxide grew from 68 nm to 74 nm [27]. Applying the formula for the FN current density of $J = A E_{ox}^2 \exp(-B/E_{ox})$ to a current density of 2×10^{-8} A/cm^2 and an onset oxide field of 6.22 MV/cm results in the equation for the slope constant as :

-B/6.22 = -35.399, giving B = 220.18 MV/cm.

Using the equation $B = 68.3 \times (0.42)^{1/2} \phi_0^{3/2} = 220.18$ gives the value of ϕ_0 = 2.914 eV, which is the same as obtained by the first method of 2.915 eV.

D. Analysis of the two methods

The CBO is practically the same by both the methods, although Method1 is considered to be more accurate as it takes the slope of the I-V curve in the high field region when the area of the dot can be ignored. The chance of error in Method 2 is less because it takes only one point on the I-V curve and the C-V dot area has to be considered which should be accurate. Here, 0.42 is the relative electron effective mass in the thermal oxide. Thus, the CBO on the MOS device fabricated with wet oxidation on the C-face of 4H-SiC is 2.92 eV and is 0.14 eV more than on the Si-face. Observing the Si-2p core level binding energy peaks on oxidised Si and C faces of 4H-SiC surface in Fig.4 of an INTECH 2013 article by Watanabe and Hosoi [16], shows that the binding energy is 0.15 eV (observing in a published article could have small errors) more on the C face as compared to the Si face. Given that the 4H-SiC experimental band gap is same on both faces at 3.23 eV results in the CBO on the C face of oxidised 4H-SiC to be 0.14 eV more. Therefore, the CBO on the oxidised carbon face 4H-SiC MOS device is 2.92 eV as calculated above. The CBO on the oxidised Si face has already been determined to be 2.78 eV in the author's earlier collaborative study [10-11]. This confirms the accuracy of all the three studies, where the samples have been fabricated in three different laboratories—oxidised carbon face 4H-SiC, oxidised Si face 4H-SiC, and the fabrication laboratory of the sample of Watanabe and Hosoi. The band offsets of all the three samples are correlated well and accurately through the combined electrical and physical measurements. It needs to be highlighted that a more careful and controlled experiment involving statistics of mean and standard deviation may inform us about the differences in the two methods of calculations. It is clear that the CBO on the C-face is a bit larger than on the Si-face of the 4H-SiC/SiO_2 interface of the MOS device.

E. Quantum Physics of the 1-D double-well potential energy function

'Particle in a box' with an electron in an infinite potential well is well understood with real life applications such as electrons on a metal or p-i-n laser diode where i is the intrinsic layer forming a quantum well between the p- and n-layers. Si-C bond in 4H-SiC (0001) having a bond length of 1.86 Å have two interacting electrons on the two atoms of Si and C. Therefore, the 1-D potential energy function will be given by a double-well as two electrons cannot stay in the same energy state according to Pauli's exclusion principle. J. Borysiuk et al. in 2011 from Poland [5] have shown the double-well potential energy surface for a Si atom adsorbed on the Si-terminated surface of 4H-SiC (0001) with one well at 0.40 eV minima and the C on top second well with the 0.27 eV minima on the right side giving a difference of 0.13 eV between the two atoms at a distance of 1.79 Å. This is shown in Fig. 1(b) of the reference based on density functional theory (DFT) calculations using the Vienna ab initio software package (VASP) and is archived at the Cornell University run website of arxiv.org. This work corroborates the author's I-V/C-V based measurements and computation discussed above where it is shown that the CBO on the Si-face of the MOS device on 4H-SiC is 0.14 eV less than on the C-face as the electron at the Si atom has 0.13 eV more negative energy in the quantum well than the electron at the C atom on top.

F. CBO plus 4H-SiC bandgap plus VBO

It is to be noted that as the title of the sub-section suggests, 2.78 + 3.23 + 2.92 = 8.93 describes the sum of the CBO on the Si-face of 2.78 eV added to the experimental bandgap of 4H-SiC at 3.23 eV and further added to the valence band offset (VBO) of 2.92 eV giving the total bandgap of the thermal oxide at 8.93 eV [28-30] for the 4H-SiC/SiO_2 interface having (0001) orientation. On the carbon face, the CBO is the VBO of the Si-face and the VBO is the CBO of the Si-face. This order dictates that a MOS device in accumulation on the Si-face will have a larger electron tunnelling current from the n-4H-SiC semiconductor cathode as the CBO is less than the VBO and on the carbon face the MOS device will have the larger hole tunnelling current from the p-4H-SiC semiconductor anode, larger than the electron tunnelling with both the MOS devices in accumulation.

G. A New Memory Device is Proposed with stoichiometric SiO_2

After thinking over the sub-section F above, a new memory device is proposed having stoichiometric wet SiO_2. Consider two n-type MOS capacitor devices in accumulation , one on the Si-face having a CBO of 2.78 eV and one on the C-face having CBOs of 2.92 eV. The MOS capacitors in accumulation will give different currents at high fields of say 7 MV/cm. These currents can be converted to voltages giving two voltage levels---the higher voltage for a '1' and the lower voltage for a '0'. That is, the MOS device on the Si-face in accumulation will provide a '1' and the MOS device on the C-face in accumulation will provide a '0'.

H. Oxide breakdown electric fields with and without charges

The barrier dependent electrical breakdown field in the thermal silicon dioxide with and without charges in the oxide is calculated based on the current density of 10^{-4} A/cm^2 through the MOS device in accumulation. It equals 46/7.4 = 6.22 MV/cm with charges and (45+16)/7.4 = 8.24MV/cm without charges in

the oxide. The breakdown field without charges is little lower than 9.5MV/cm on $Si/SiO_2/Al$ device [30], where the CBO is 3.2 eV instead of 2.92 eV in the present device for the same current density of 10^{-4} A/cm^2 through a thick thermal oxide considered to be a current density at which the oxide can be declared to have an electrical breakdown. These values in general reflect the slightly lower reliability of the 4H-SiC based MOS device. However, the oxide field for a long channel power MOSFET switch is very small during the on-state of the switch having a maximum gate to source voltage minus the threshold voltage of 40 V for example, for a 150 nm thick oxide and therefore giving an oxide field of 2.67MV/cm only [31]. The author's earlier collaborative study [27] shows in Fig.4 that more than 70% C-V dots exhibit 2 x 10^{-8} A/cm^2 current density at 3MV/cm oxide field.

IV. Conclusions

It is concluded through this extension of the author's earlier collaborative study, that the conduction band offset in the MOS device fabricated on the C-face of the 4H-SiC is 2.92 eV. It is 0.14 eV larger than the CBO on the Si-face of 2.78 eV. The CBO on the Si-face becomes the VBO on the C-face due to this 0.14 eV difference keeping the experimental bandgap of 4H-SiC at 3.23 eV. The higher CBO on the C-face is confirmed by XPS measurements of Si-2p core electron peaks by XPS. The oxide breakdown field with charges is lower at 6.22 MV/cm and at 8.24 MV/cm without charges. The breakdown field without charges is slightly lower than on the $Si/SiO_2/Al$ device indicating a relatively lower reliability, although the 4H-SiC power MOSFET switch operating in the on-state has a low oxide field of 2-3MV/cm only. The method of characterising MIS devices based on I-V/C-V measurements can be quite accurate. A new memory device is possible on Silicon Carbide that can work at higher temperatures than Silicon.

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