

Comparative Study of FPGA Performance Over ASIC and DSP Processors

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Abstract:

Field programmable gate array FPGA proposals an unconventional explanation for the computationally-intensive functions establish in Digital Signal Processing (DSP). DSP organization performance can be improved by using programmable logic device as well as reducing total system cost. Programmable logic syndicates the elasticity of a general-purpose DSP desirable the speed, density, and low cost of an ASIC (Application-Specific Integrated Circuit, commonly called a gate array) implementation. In several presentations, programmable logic substitutes the DSP processor completely. In other applications, it accomplishes in conjunction with the DSP processor, relieving of the computationally-intensive function and releasing the processor for other functions. In this paper the comparison study was illustrated between FPGA and DSP processor performance.

Analgesia, one of the components of triad of anaesthesia, has now extended to relief of postoperative pain, chronic pain and cancer pain. The spinal cord has taken the center stage in analgesia practice and Spinal anaesthesia is the commonly used technique for lower limb surgeries as it is easy to administer, economical and causes less hemodynamic variation than general anaesthesia. Hence different additives can be used to increase the duration of postoperative analgesia. Since there are no studies comparing Buprenorphine and Nalbuphine, we have selected this study to evaluate the effect of intrathecal Bupivacaine with Buprenorphine compared with Nalbuphine for postoperative analgesia.

Key Word: DSP, FPGA, ASIC, digital filters, FIR, IIR, SDA.

Date of Submission: 21-01-2020

Date of Acceptance: 12-02-2020

I. Introduction

Digital Signal Processing (DSP) is individual of the fastest-growing solicitations in the electronics engineering. It is used in an extensive range of applications including [1]:

- Telecommunications
- Data communications
- Wireless communications
- Image enhancement and processing
- Data acquisition
- Remote sensing
- Radar
- Video processing

There are numerous high-performance DSP processors however they are not appropriate to all DSP solicitations. Their general-purpose structural design creates these DSP processors malleable, on the other hand they may not be sufficient firm or budget effective for all organizations [2].

Field Programmable Gate Arrays (FPGAs) hypothetically afford performance intensifications of an order of magnitude in excess of old-fashioned DSPs with the equivalent plasticity [1].

II. DSP system architecture

1. DSP techniques:

The term DSP smears approximately to uninterrupted mathematical progressions, attempted in real time. These contain occupations such as [3]:

- Digital Filtering
 - Finite Impulse Response (FIR)
 - Infinite Impulse Response (IIR)
- Convolution

- Correlation
- Fast Fourier Transforms

Supreme of these utilities involve the received data to be reproduced or supplementary with numerous interior feedback apparatuses to accomplish the anticipated scientific occupation. This occupation is universally termed Multiply/Accumulate [3].

1-1FIR filtering:

FIR filter is a filter whose response to every limited span input is of determinate interval, for the reason that it resolves to zero in restricted period. The impulse response of the FIR filter is accomplished via configurations consuming no feedback arrangement. The output of the arrangement is determined by solitary on the current plus previous standards of the input only. The response of an Nth-order discrete-time FIR filter survives precisely $N + 1$ samples in advance it then and there resolves to zero. For a fundamental discrete-time FIR filter of order N , every assessment of the output sequence is a weighted sum of the utmost modern input standards [4].

$$y(n) = b_0x(n) + b_1x(n-1) + \dots + b_Nx(n-N) \quad (1)$$

Where $x[n]$ is the input signal, $y[n]$ is the output signal, N is the filter order and b_i is a coefficient of the filter.

1-2IIR filtering:

IIR filter is a filter whose response to every limited spans input does not turned out to be accurately zero as previous convinced point, nonetheless remains indeterminately. The impulse response of the IIR filter is regularly carried out by means of configurations consuming interior feedback organization. The output of the filter at every prearranged period is determined by the existing inputs and previous. IIR filter is recursive in environment and equation is [5]:

$$y(n) = \sum b_k X(n-k) - \sum a_k Y(n-k) \quad (2)$$

Where: N is the filter order, which relates to the amount of delay components a carrying out of the filter would necessitate. The filter quantities are a_k and b_k . IIR filters have quantities a_k , $k > 0$ that are nonzero, which denotes that the instinct response of an IIR filter has unlimited span.

2. DSP implementation

There are three procedures used to appliance these purposes.

1- DSP Processor

Supreme general-purpose DSP processors achieve a multiply/accumulate task in a distinct clock cycle (or fewer). The hardware to implement this occupation is entitled a multiply/Accumulator (MAC). Utmost DSP processors require a fixed-point MAC even though specific ensure a further costly floating-point MAC [6].

2- ASIC technology

As soon as presentation is a feature, numerous inventors go to ASIC technology. ASIC technology proposals the capability to design an institution construction to be precise augmented for the objective application. For instance, digital filtering characteristically has need of numerous MAC cycles—unique MAC cycle for every one filter taps. A customary DSP simply devises a distinct MAC; hence every filter tap must be fulfilled one after the other. An ASIC carrying out of a filter procedure might obligate various MACs to facilitate the completely taps can be treated in corresponding [7].

3- FPGA technology

Nevertheless, FPGA be responsible for a third explanation that syndicates the superlative of mutually DSP and ASIC skills deprived of their relevant boundaries [7].

A Field Programmable Gate Array (FPGA) consumes a malleable structural design that can be modified on behalf of an explicit DSP occupation. Correspondingly, FPGAs obligate adequate aptitude to appropriate compound MACs or procedures into a distinct scheme in conjunction with the interface circuitry obligated via the solicitation—a single-chip explanation associated to a DSP processor.

Similar to general-purpose DSP processors, FPGAs are programmable and unpredictable. The designer can create vicissitudes speedily deprived of the supplementary budget besides extended prime intervals of an ASIC. FPGAs, similar to DSPs, ought to no smallest capacity requests as do ASICs [8].

III. Performance Comparisons

DSP structural design unswervingly touches organization presentation. Since supreme DSP occupations are Multiply/accumulate-based, the presentation of the MAC is fundamental [3].

Approximately every single processor is gifted of execution DSP procedures for the reason that approximately each processor can accomplish additions and multiplies. The solitary dissimilarity among a general-purpose DSP and a microprocessor is in what way fine they implement this task [6].

Every tap of a digital filter involves one MAC cycle. For instance, a 16-tap filter obliges 16 MAC cycles. For the reason that supreme DSPs simply ensure a single MAC component, every one tap is administered in sequence, decelerating global structure presentation [4].

A number of the more influential and individually further costly DSPs obligate numerous MACs. These DSPs accomplish compound MACs in one clock cycle. The equivalent objective is talented through consuming several single-MAC DSPs with communal high-speed memory. In both circumstances, additional presentation is swallowed with advanced unit charge and over board interplanetary [5].

FPGAs suggest a uniform extra dominant structural design one personalized to the precise solicitation. Since the logic in an FPGA is malleable, the DSP purpose can be mapped straightly to the properties accessible on an FPGA. Figure 1 indicates the qualified presentation of numerous carrying out of an 8-bit, 16-tap FIR filter, stabilized to the presentation of a 50 MHz fixed-point DSP processor [7].

The supreme well-organized FPGA putting into practice exposed uses 68% of an XC4003E-3 FPGA, or approximately 1,500 gates [7]. This enactment overtakes a distinct 50 MHz DSP by an issue of 2.6. The fundamental to its good organization is the Sequential Distributed Arithmetic (SDA) procedure [9]. This procedure profits benefit of the XC4000E architectural structures. The multiply utilities are mapped into the FPGA's task initiators, the adders and accumulators habit the XC4000E firm convey logic, also the serial shift registers are fabricated in well-organized, on-chip RAM [10].

The uppermost presentation FPGA carrying out habits nearly 75% of an XC4013E-2 FPGA, or around 9,750 gates. Nevertheless approximately seven times superior to the universe proficient form, the great presentation execution is 22 times more rapidly than a 50 MHz DSP for this request. It habits a Parallel Distributed Arithmetic (PDA) procedure. Even sophisticated presentation is probable if the solicitation can put up with the additional data invisibility initiated by means of pipelining. Presentation will as well be situated sophisticated if the filter is incorporated with additional logic in the equivalent chip thus via passing I/O intervals [9].

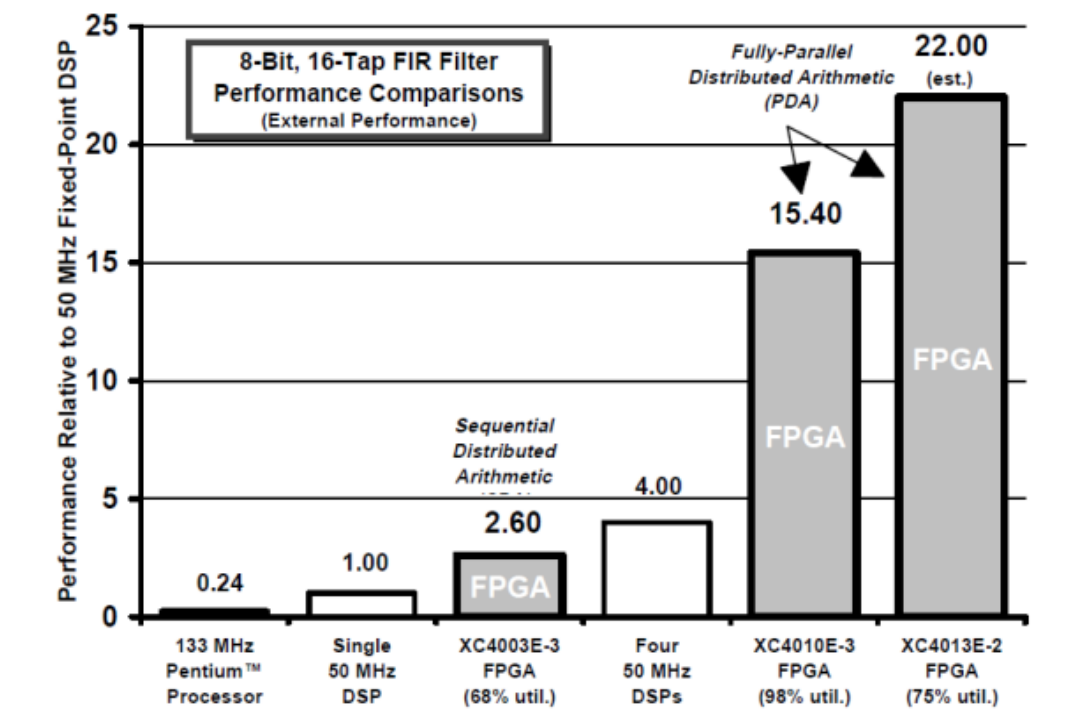


Figure 1 . Relative performance various implementations of an 8-bit , 16-tap FIR

3-1 FPGA Instead of DSP Processor

In various solicitations, a firm plus actual costly DSP processor is used to grip the greatest presentation of a minor quantity of program. A characteristic DSP procedure comprises a lot of monotonous feedback loops as well as parallel configurations as presented in the data flow illustration designed for the 16-tap FIR filter in Figure 2 [11]. The software program intended for such set of rules is not professionally fulfilled in general-purpose DSP structural design. Normally, around 20–40% of the DSP's program makes use of 60–80% of the DSP's processing power [11].

Individual common technique to enhance DSP presentation is to habit compound DSPs in parallel and over great speed memory. For instance, the four-DSP explanation exposed in Figure 1 is hypothetically four times the presentation of the single-DSP explanation.

On the other hand, the budget is further than four times advanced. These multi-chip DSP schemes commonly involve extra board space plus sophisticated presentation memories that increases budget [7].

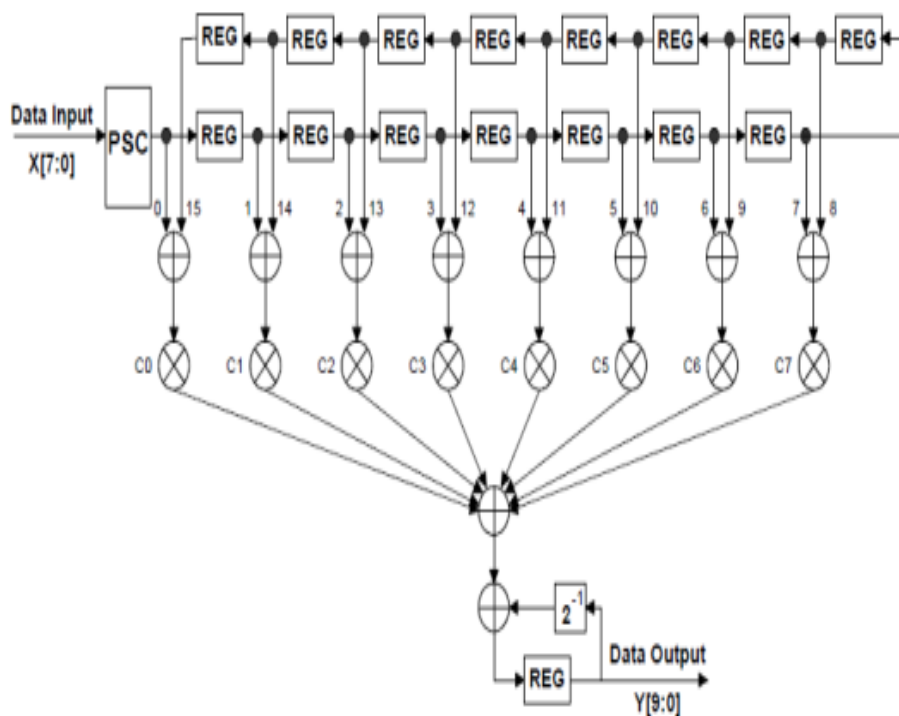


Figure 2 .Data flow diagrams for a 16-tab FIR filter

As a substitute, the finest clarification for these solicitations may possibly be a DSP processor, microprocessor, or micro-controller with an FPGA co-processor. The general-purpose DSP processor handles the organization mechanism besides information association occupations.

The FPGA offers a custom-tailored DSP co-processor to handle the greatest dispensation occupation [8].

Investigating the DSP procedure will make public every parallel configuration plus iterative loops that put away DSP processing influence. Assigning these occupations in the FPGA improves the inclusive presentation.

The FPGA-based DSP accelerator theory is related to a floating-point co-processor functioning with a microprocessor.

Figure 3 demonstrates the block diagram of FPGA chip [9].

It comprises of:

- ❖ Firm, extraordinary concentration FPGA structural design.
- ❖ A well-organized FPGA structural design for mathematics plus data pathway solicitations.
- ❖ An incorporated, extraordinary speed processor interface.
- ❖ A firm arrangement in addition to restricted reconfiguration.
- ❖ Relaxed admittance to interior logic and flip flops.

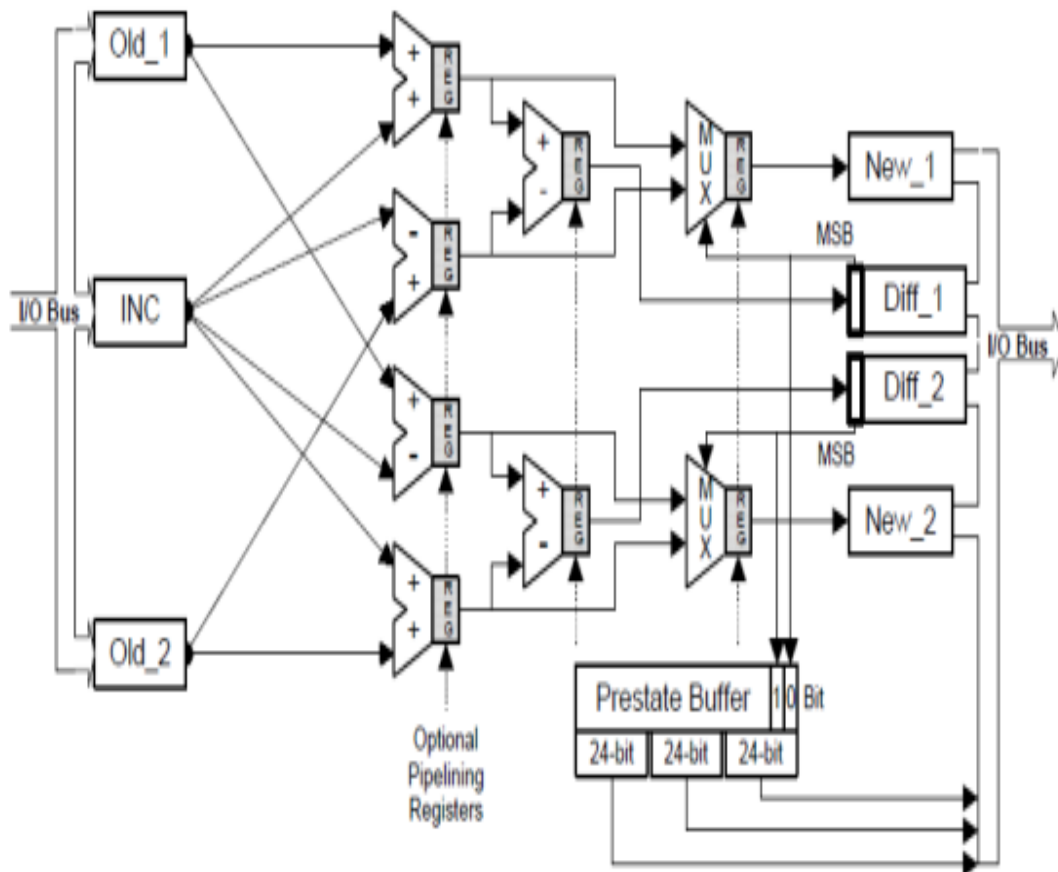


Figure 3 . FPGAs implement the multiple Add/Subtract functions in parallel

3-2 FPGA Instead of ASIC

FPGAs furthermore substitute ASICs in DSP organizations. Engineers pick out ASIC in the previous for two causes [8]:

- They looked-for DSP dispensation power out there the abilities of a general-purpose DSP.
 - The structure had adequately great construction capacities to vindicate a semi-custom explanation.
- Similar to ASICs and FPGAs can arrange for greater presentation to general-purpose DSPs. The least possible capacity requirements plus the extended lead-times, besides possibility of an ASIC are objectionable for low-size assignment. FPGAs afford the presentation besides architectural suppleness of ASICs however are consumers programmable for low improvement rates [8].

Conflicting to general conviction, moreover FPGAs proposal an explanation for extraordinary- size designs. Intention repairing, arrangement certification, in addition to preliminary construction are prepared with FPGAs. As soon as confirmed, the hardwire gate collections be responsible for a low possibility relocation pathway to extraordinary- size, little- budget explanation. A supplementary advantage of SRAM-based FPGAs in excess of ASICs is that they can be re-encoded, on the fly, in the arrangement. As a result, a distinct FPGA can carry out diverse DSP occupations at numerous intervals in a scheme to enhancement global presentation [9].

Discovering the accurate occupation to habit FPGAs to improve the presentation of a DSP solicitation [12]:

- Recognize the parallel information pathways in the procedure.
- The FPGA can gadget these purposes in parallel. A DSP requisite accomplish these one after the other.
- Find processes that involve compound regulator sequences as soon as accomplished in a general-purpose DSP. Once more, proceeds benefit of the FPGA's parallelism.

Figure 4 illustrates the graph performance of FPGA-based DSP vs. one or more DSP processors. Shaded region indicates where FPGA is a better solution.

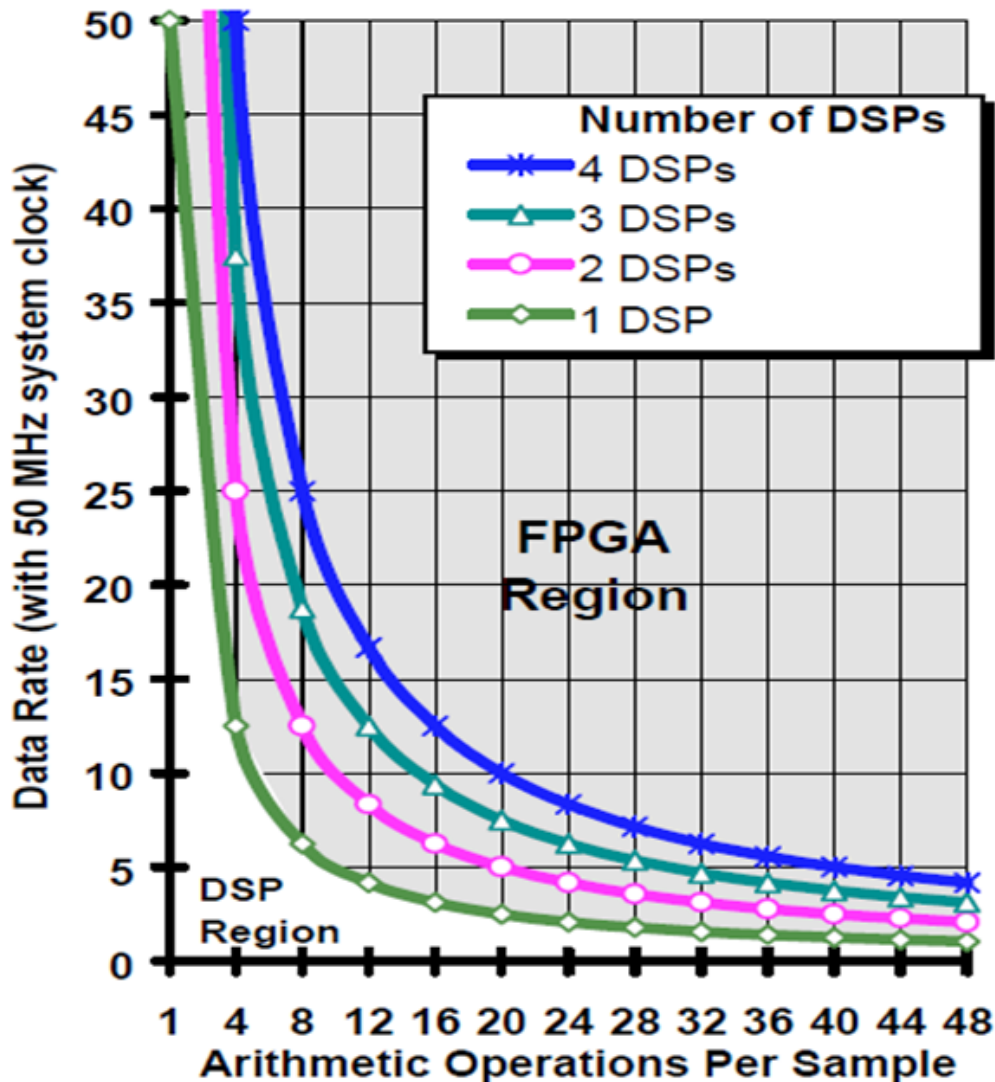


Figure 4: FPGA performance graph

IV. Conclusion

In this paper a comparison study was deliberated to design FIR digital filter. The performance of three methods was considered which are DSP processors, ASIC, and FPGA techniques. It is clear from graph of figure 4 that the DSP performances have advantages using FPGA techniques take account of those demanding:

- ☒ High sample rates: FPGA-based DSP organizations overtake unique or additional general-purpose DSP processors as shown in Figure 4.
- ☒ Low sample rates: at information amounts between 1 kHz to 100 kHz, the DSP occupation can be certainly incorporated alongside with additional scheme logic in a low-rate FPGA by means of a precise well-organized sequential progressive procedure.
- ☒ Short word length: FPGA-based DSP enterprises run more rapidly by way of the word width reductions when using the space-efficient SDA procedure.
- ☒ Lots of filter taps: the quantity of filter taps devises slight consequence on an FPGA-based DSP enterprise when using the space efficient SDA procedure.
- ☒ Single-chip solution required: incorporates the DSP occupation besides completely the arrangement logic in a distinct FPGA.

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Faris Ali Jasim. "Comparative Study of FPGA Performance Over ASIC and DSP Processors." *IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)*, 15(1), (2020): pp. 07-13.