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Multilevel Inverter for Single Phase System with Reduced Number of Switches

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Abstract: *Multilevel inverter has emerged recently as a very important alternative in the area of high-power medium voltage energy control. This project present cascaded multi cell with separate DC sources. Multilevel inverters are promising they have nearly sinusoidal output-voltage waveforms, output with better harmonic profile, less stressing of electronic components. The conventional is a single-phase seven-level inverter for grid-connected photovoltaic systems, with a novel pulse width-modulated (PWM) control scheme .In a conventional paper to get the thirteen level inverter output voltage using a six full bridge cascaded type inverter with 24 switches .The inverter is capable of producing thirteen levels of output-voltage levels from the dc supply voltage. The proposed inverter system is capable of producing thirteen level of output voltage levels dc supply voltage by using three full bridge cascaded topology type inverter. In this project has used to three H-bridge inverter with different dc sources. The multi-level inverters promising the high performance with reduced EMI and harmonics. The proposed project is thirteen-level inverter was designed and results were also shown in the thesis.This project is focused on minimizing the number of semiconductors devices for a given number of levels.*
Index Terms: *Inverter, electrical drives, cascaded, high power, multilevel inverter, reliability.*

I. INTRODUCTION

A single-phase grid-connected inverter is usually used for residential or low-power applications of power ranges that are less than 10 kW. Types of single-phase grid-connected inverters have been investigated. A common topology of this inverter is full-bridge three-level. The three-level inverter can satisfy specifications through its very high switching, but it could also unfortunately increase switching losses, acoustic noise, and level of interference to other equipment. Improving its output waveform reduces its harmonic content and, hence, also the size of the filter used and the level of electromagnetic Interference (EMI) generated by the inverter are switching operation.

Multilevel inverters are promising that they have nearly sinusoidal output-voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact.

Various topologies for multilevel inverters have been proposed over the years. Common ones are diode - clamped, flying capacitor or multi cell, cascaded H-bridge, and modified H-bridge multilevel. This project recounts the development of a novel modified H-bridge single-phase multilevel inverter that has two diode embedded bidirectional switches and a novel pulse width modulated (PWM) technique. The topology was applied to a grid connected photovoltaic system with considerations for a maximum-power-point tracker (MPPT) and a current-control algorithm.

The proposed single-phase thirteen-level inverter was developed from the Seven-level inverter. The H-bridge topology is significantly advantageous over other topologies, i.e., less power switch, power diodes, and less capacitor for inverters of the same number of levels.

II. Basic Concept of Multilevel Inverter

A. Genesis of Multilevel Inverter

In this chapter, the multilevel inverter and its types are discussed. The principle function of the inverters is to generate an ac voltage from a dc source voltage. If the dc voltage is composed by many small voltage sources connected in series, it becomes possible to generate an output voltage with several steps.

Multilevel inverters are significantly different from the ordinary inverter where only two levels are generated. In which each group of devices contribute to a step in the output voltage waveform. The steps are increased to obtain an almost sinusoidal waveform. The number of switches involved is increased for every level increment. Generally the output waveform of the multilevel inverter is generated from different voltage sources obtained from the capacitor voltage sources. In the past two decades, several multilevel voltage source

converters have been introduced. Consider a three phase inverter system . with DC voltage Vdc. Series connected capacitors constitute the energy tank for the inverter, providing some nodes to which the multilevel inverter can be connected. Each capacitor has the same voltage Em, which is given by, Em = Vdc / (m-1) Where m denotes the number of the level is referred to as the number of nodes to which the inverter can be accessible. An m level inverter needs (m-1) capacitors. Output phase voltages can be defined as voltage across output terminals of the inverter and the ground point denoted by 0.

B. Multilevel Inverter Characteristics

Multilevel inverters include an arrangement of semiconductors and dc voltage sources required to generate a staircase output voltage waveform. Fig.Shows the schematic diagram of voltage source-inverters with a different number of levels.

It is well known that a two level inverter, such as the one shown in Fig., generates an output voltage with two different values (levels), V_C and "zero," with respect to the negative terminal of the dc source ("0"), while a three-level module, Fig.Generates three different voltages at the output ($2V_C$, V_C, and "zero"). The different positions of the ideal switches are implemented with a number of semiconductors that are in direct relation with the output voltage number of levels. Multilevel inverters are implemented with small dc sources to form a staircase ac waveform, which follows a given reference template. For example, having ten dc sources with magnitudes equal to 20 V each, a composed 11-level waveform can be obtained (five positive, five negatives, and zero with respect to the middle point between the ten sources), generating a sinusoidal waveform with 100-V amplitude as shown in Fig.1and with very low THD.

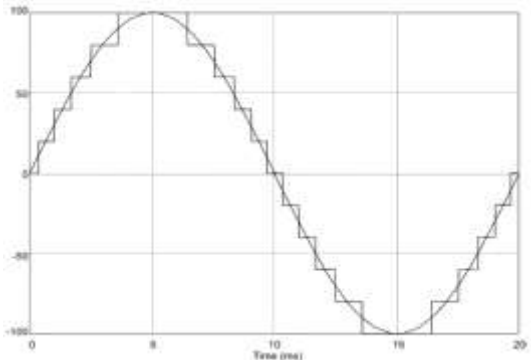

Fig.1 Voltage Waveform from 11-Level Inverter

It can be observed that the larger the number of the inverter dc supplies, the greater the number of steps that can be generated, obtaining smaller harmonic distortion. However, the number of dc sources is directly related to the number of levels through the equation.

n = m-1 . . . . . *(1)*

Where 'n' is the number of dc supplies connected in series and 'm' is the number of the output voltage levels. In order to get a 51-level inverter output voltage, 50-V supplies would be required, which is too much for a simple topology. Besides the problem of having to use too many power supplies to get a multilevel inverter, there is a second problem which is also important, the number of power semiconductors required to implement the commutation circuit.

C. Classification of Multi Level Inverters

i. Diode – Clamped Inverter

This inverter consists of a number of semiconductors connected in series, and another identical number of voltage sources, also connected in series.

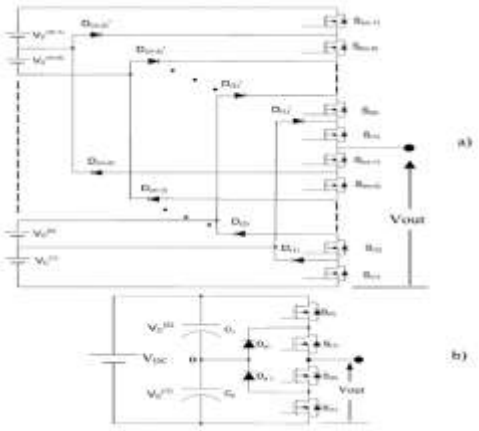

Fig.2 (A) The M-Level (B) Three-Level Diode-Clamped Inverter Topology.

These two chains are connected with diodes at the upper and lower semiconductors as shown inFig.2(A)
For an m -level converter, the required number of transistors is given by

$$T = 2(m-1) \quad \ldots\ldots\ldots \quad (2)$$

Then, for the example of a 51-level converter, 100 power transistors would be required (which is an enormous amount of switches to be controlled). One of the most utilized configurations with this topology is that of the three-level inverter, which is shown in Fig.2.(B) the capacitors act like two dc sources connected in series. Thus, in the diagram, each capacitor accumulates 1/2 V_{dc}, giving voltages at the output of 1/2 V_{dc}, 0, or 1/2 V_{dc} with respect to the middle point between the capacitors.

ii. Capacitor-clamped inverter

This inverter has a similar structure to that of the diode-clamped, however it can generate the voltage steps with capacitors connected as shown in Fig.3.

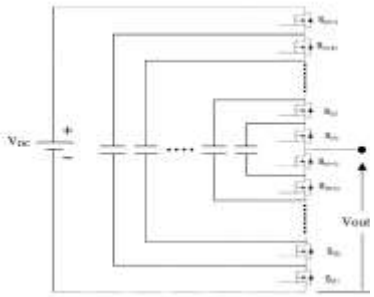

Fig.3The M-Level Capacitor-Clamped Inverter.

The problem with this converter is that it requires a large number of capacitors, which translates to a bulky and expensive converter as compared with the diode-clamped inverter.

Besides, the number of transistors used is the same with the diode-clamped inverter, and therefore, for a 51-level inverter, 100 power transistors are required. In order to overcome all these problems, a third topology, which will be called the "transistor-clamped inverter" will be presented and analyzed.

iii. Transistor-clamped inverter

The transistor-clamped inverter has the advantage of requiring the same number of power transistors as the levels generated, and therefore, half with respect to the previous topologies reduces the semiconductors. A 51-level converter requires 51 transistors (instead of 100 transistors). Fig.4 shows the circuit topology of a -level transistor clamped inverter, which satisfies

$$T = m \quad \ldots\ldots\ldots \quad (3)$$

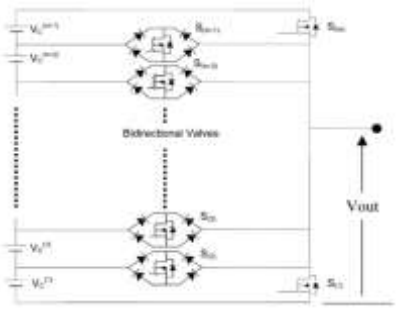

Fig.4The M-Level Transistor-Clamped Inverter.

In this topology, the control of the gates is very simple because only one power transistor is switched-on at a time. Then, there is a direct relation between the output voltage, Vo, and the transistor that has to be turned-on. However, and despite the excellent characteristics of this topology, the number of transistors is still too large to allow the implementation of a practical converter with more than 50 levels.

One solution for increasing the number of steps could be the use of "H" converters, like the one shown in Fig.2.8, which consists of connecting two of the previously discussed topologies in series (two legs). If transistor-clamped inverters are used to build an "H" converter, the number of transistors required for an -level inverter is 1, which means only one more transistor than what is required for a simple leg configuration. However, the number of dc sources is reduced to 50%, which is the most important advantage of "H" converters.

iv. Cascaded multilevel inverter

Another characteristic is that the "H" topology has many redundant combinations of switches' positions to produce the same voltage levels. As an example, the level "zero" can be generated with switches in position S(1) and S(2), or S(3) and S(4), or S(5) and S(6), and so on. Another characteristic of "H" converters is that they only produce an odd number of levels, which ensures the existence of the "0V" level at the load as shown in fig.5. .For example, a 51-level inverter using an "H" configuration with transistor-clamped topology requires 52 transistors, but only 25 power supplies instead of the 50 required when using a single leg. Therefore, the problem related to increasing the number of levels and reducing the size and complexity has been partially solved, since power supplies have been reduced to 50%.

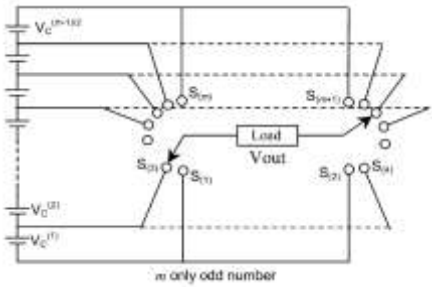

Fig.5The M-level inverter using an H-bridge.

III. PROPOSED CIRCUIT DIAGRAM

a) Circuit descriptions

A cascaded multilevel inverter consists of a series of H-bridge (single phase full bridge) inverter units. The general function of this multilevel inverter is to synthesize a desired voltage from several dc sources (SCDs), which may be obtained from batteries, fuel cells. Fig.6 shows optimized topology of single-phase cascaded inverter. The ac terminal voltages of each bridge are connected in series. Unlike the diode clamp or flying-capacitors inverter, the cascaded inverter does not require any voltage-clamping diodes or voltage balancing capacitors. This configuration is useful for constant frequency applications such as active front-end rectifiers, active power filters, and reactive power compensation. In this case, the power supply could also be voltage regulated dc capacitor. The circuit diagram consists of three cascade bridges. The load is connected in such a way that the sum of output of these bridges will appear across it.

b) Circuit Operations

The required thirteen levels of output voltage were generated as follows:

Mode 1(0Vdc): The switch S2, S4, S6, S8, S10, S12 will be turned ON and all other controlled switches are turn OFF. So the current flows path from S4, load(R), S10, S12, S6, S8 and S2.The voltage applied to the load terminal is zero (0).

Mode 2(6Vdc): The switch S1, S2, S5, S7, S9, S11 will be turned ON and all other controlled switches are turn OFF. So the current flows path from voltage source (V1+ve), S1, load(R), S9, S11, S5, S7, S2 and V1 (-ve).The voltage applied to the load terminal is 6v.

Mode 3(12Vdc): The switch S1, S3, S5, S6, S9 and S11 will be turned ON and all other controlled switches are turn OFF. So the current flows path from S1, load(R), S9, S11, S6, V2, S5 and S3 .The voltage applied to the load terminal is 12V.

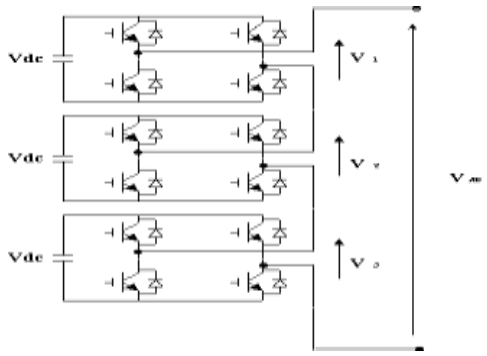

Fig.6 Circuit diagram of proposed MLI

Mode 4(18Vdc): The switch S1, S3, S5, S7, S9 and S10 will be turned ON and all other controlled switches are turn OFF. So the current flows path from S1, load(R), S10, V3, S9, S5, S7 and S3 .The voltage applied to the load terminal is 18V.

Mode 5(24Vdc): The switch S1, S2, S5, S7, S9 and S10 will be turned ON and all other controlled switches are turn OFF. So the current flows path from S1, load(R), S10, V3, S9, S5, S7, S2 and V1.The voltage applied to the load terminal is 24V.

Mode 6(30Vdc): The switch S1, S3, S5, S6, S9 and S10 will be turned ON and all other controlled switches are turn OFF. So the current flows path from S1, load(R), S10, V3, S9, S6, V2, S5 and V3.The voltage applied to the load terminal is 30V.

SWITCHING PATTERNS

V	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	0	1	0	1	0	1	0	1	0	1	0	1
6	1	1	0	0	1	0	1	0	1	0	1	0
12	1	0	1	0	1	1	0	0	1	0	1	0
18	1	0	1	0	1	0	1	0	1	1	0	0
24	1	1	0	0	1	0	1	0	1	1	0	0
30	1	0	1	0	1	1	0	0	1	1	0	0
36	1	1	0	0	1	1	0	0	1	1	0	0
30	1	0	1	0	1	1	0	0	1	1	0	0
24	1	1	0	0	1	0	1	0	1	1	0	0
18	1	0	1	0	1	0	1	0	1	1	0	0
12	1	0	1	0	1	1	0	0	1	0	1	0
6	1	1	0	0	1	0	1	0	1	0	1	0
0	0	1	0	1	0	1	0	1	0	1	0	1
6	0	0	1	1	0	1	0	1	0	1	0	1
-12	0	1	0	1	0	0	1	1	0	1	0	1
-18	0	1	0	1	0	1	0	1	0	0	1	1

-24	0	0	1	1	0	1	0	1	0	0	1	1
-30	0	1	0	1	0	0	1	1	0	0	1	1
-36	0	0	1	1	0	0	1	1	0	0	1	1
-30	0	1	0	1	0	0	1	1	0	0	1	1
-24	0	0	1	1	0	1	0	1	0	0	1	1
-18	0	1	0	1	0	1	0	1	0	0	1	1
-12	0	1	0	1	0	0	1	1	0	1	0	1
-6	0	0	1	1	0	1	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1	0	1	0	1

Table.1Switching pattern for proposed system

Mode 7(36Vdc): The switch S1, S2, S5, S6, S9 and S10 will be turned ON and all other controlled switches are turn OFF. So the current flows path from S1, load(R), S10, V3, S9, S6, V2, S5, S2 and V1.The voltage applied to the load terminal is 36V.

Mode 8(-6Vdc): The switch S3, S4, S6, S8 S10 and S12 will be turned ON and all other controlled switches are turn OFF. So the current flows path from S3, load(R), S10, S12, S6, S8, S4 and V1.The voltage applied to the load terminal is -6V.

Mode 9(-12Vdc): The switch S2, S4, S7, S8, S10 and S12 will be turned ON and all other controlled switches are turn OFF. So the current flows path from S2, S8, V2, S7, S10, S12, load(R), and S4 .The voltage applied to the load terminal is 12V.

Mode 10(-18Vdc): The switch S2, S4, S6, S8, S9 and S10 will be turned ON and all other controlled switches are turn OFF. So the current flows path from S2, S6, S8, S12, V3, S11, load(R), and S4 .The voltage applied to the load terminal is 12V.

Similarly for all other modes in negative output voltages. So, we get output voltages as.-24V,-30V, and -36V.

IV. SIMULATION RESULTS

MATLAB is an interactive system whose basic data element is an array that does not require dimensioning. This allows you to solve many technical computing problems, especially those with matrix and vector formulations, in a fraction of the time it would take to write a program in a scalar non interactive language such as C or FORTRAN.

AC Voltage Source block into the circuit1 window. C components have disappeared so that the icon now shows a single resistor.

A. CASCADED CIRCUIT DIAGRAM

The switching sequence obtained as discussed in the previous chapter. The component values are chosen based on the design requirement.

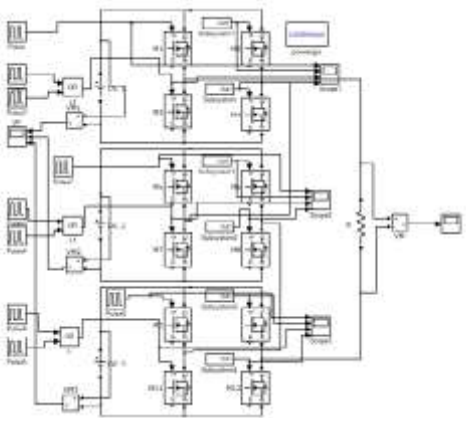

Fig.7 Simulation Diagram of Cascaded thirteen-Level Inverter

4.6.1 Input voltage waveform

The simulated input voltage, which is measured across the input side by connecting a voltage measurement with scope as shown Fig.8 and the input voltage are given to the individual bridges is 6V,12V,18V respectively.

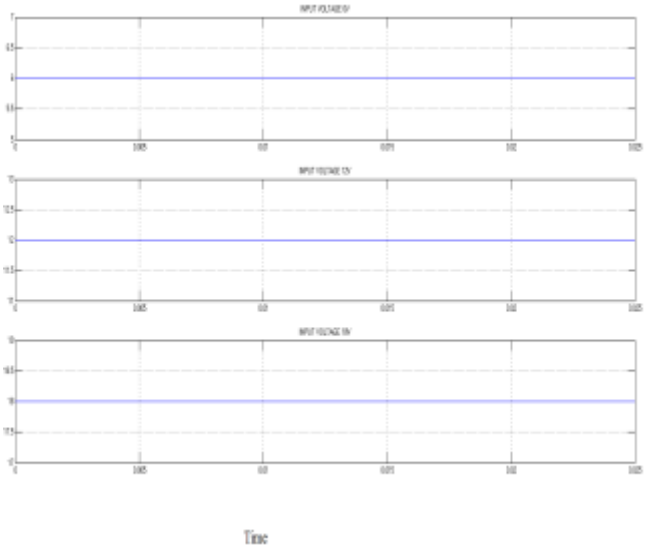

Fig.8 Input voltage waveform

4.6.2 Pulse generation (bridge1)

The simulated gate triggering pulses, which is measured by connecting a single scope measurement as shown in Fig.9 and pulses are given to the switches S1,S2,S3,S4 respectively.

(PULSES FOR S1, S2, S3, S4 SWITCHES)

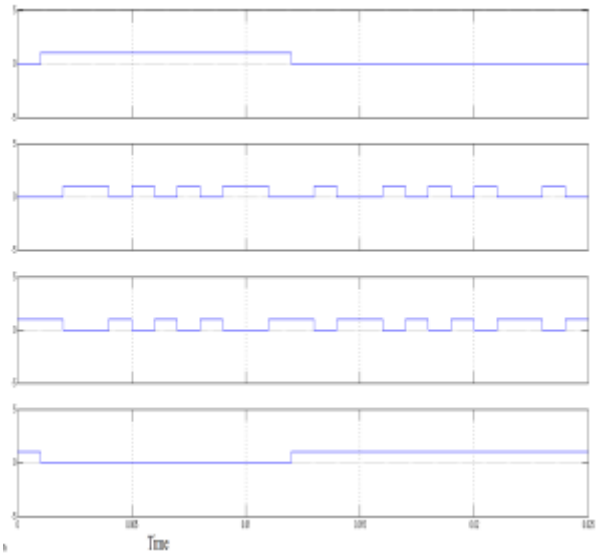

Fig.9 Pulse generation for bridge1

4.6.3 Pulse generation (bridge2)

The simulated gate Triggering pulses, which is measured by connecting a single scope measurement as shown in Fig.10. Pulses are given to the switches S5, S6, S7, and S8 respectively.

(PULSES FOR S5, S6, S7, S8 SWITCHES)

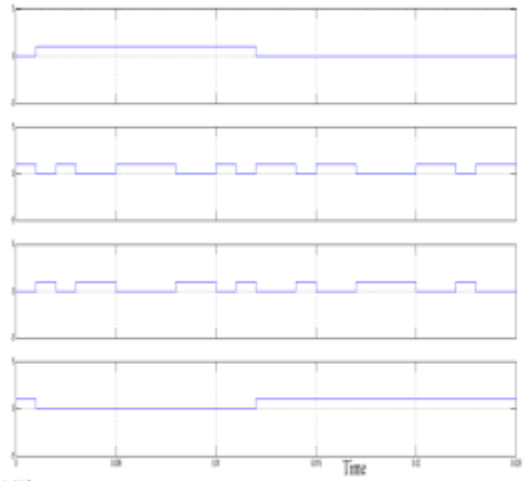

Fig.10 Pulse generation for bridge2

4.6.4 Pulse generation (bridge3)

The simulated gate triggering pulses, which is measured by connecting a single scope measurement as shown in Fig.11. Pulses are given to the switches S9, S10, S11, and S12 respectively.

(PULSES FOR S9, S10, S11, S12 SWITCHES)

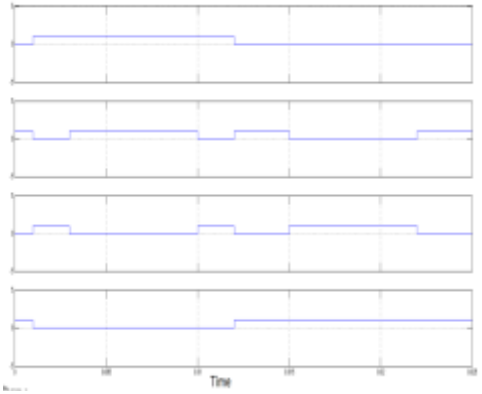

Fig.11 Pulse generation for bridge3

4.6.5 Output voltage of cascaded 13-level inverter

The simulated output voltage, which is measured across the output of resistive loads by connecting a voltage measurement with scope as shown in Fig 4.13 and each an every stepped voltage is 6V difference.

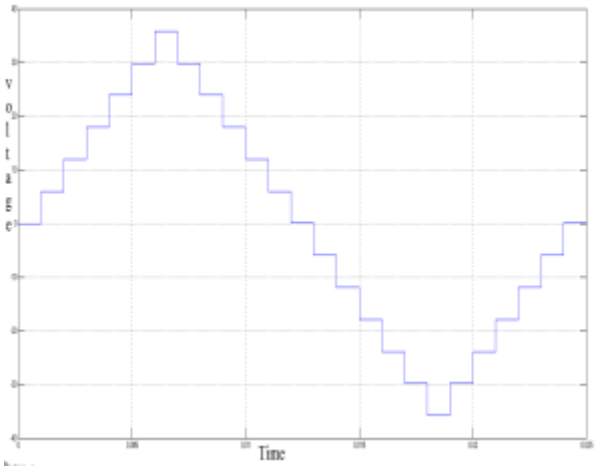

Fig.12 Output voltage waveform

4.7 FFT ANALYSIS

By using multilevel inverter the even harmonics are eliminated due to its symmetrical. And odd harmonics are reduced and input cycle is taken as five for a 50HZ supply as shown in Fig.13.

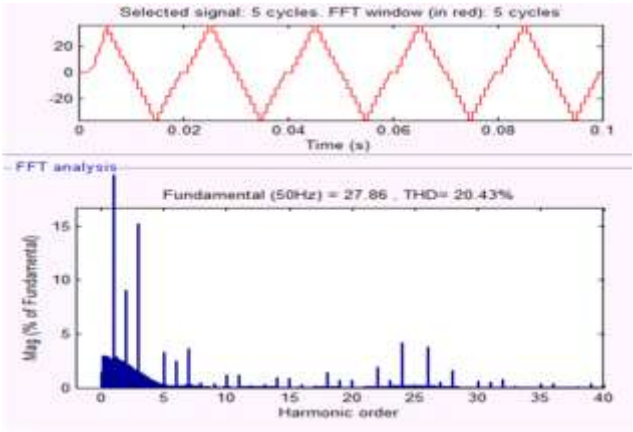

Fig.13 FFT analysis

V. CONCLUSION

A multilevel inverter with individual dc sources has been proposed for use in large electric drives. Simulation and experimental results have shown that with a control strategy operates the switches at the fundamental frequency, these converters have high output voltage, less THD and high efficiency and improved power factor. In the proposed method semiconductor devices are reduced. .In a conventional paper to get the thirteen level inverter output voltage using a six full bridge cascaded type inverter with 24 switches.Thus the proposed method will reduce the cost, and also used only12 switches, harmonic reduction and the heat losses. Therefore the proposed method can be implemented in the inverters than conventional method.

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