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A Soft-Switching DC/DC Converter with High Voltage Gain

Prakash Parvatham, Dr.A.Srujana:

Abstract: *A soft-switching dc/dc converter with high voltage gain is proposed in this paper. The proposed converter reduces switching loss of active power switches and raises the conversion efficiency by using zero voltage switching (zvs) and zero current switching (zcs) techniques. This paper provides the effective solution for reverse recovery problem of the output rectifier by controlling the rate of change of current through diodes with the help of leakage inductance of a couple inductor cell. The proposed converter also provides continuous input current and high voltage gain. Experimental results obtained on 200W prototype are discussed..*
Index Terms: *Boost converter, high voltage gain, soft switching.*

I. Introduction

In the 1970's, conventional PWM power converters were operated in a switched mode operation. Power switches have to cut off the load current within the turn-on and turn-off times under the hard switching conditions. Hard switching refers to the stressful switching behavior of the power electronic devices. The switching trajectory of a hard-switched power device is shown in Fig.i. During the turn-on and turn-off processes, the power device has to withstand high voltage and current simultaneously, resulting in high switching losses and stress. Dissipative passive snubbers are usually added to the power circuits so that the dv/dt and di/dt of the power devices could be reduced, and the switching loss and stress be diverted to the passive snubber circuits. However, the switching loss is proportional to the switching frequency, thus limiting the maximum switching frequency of the power converters. Typical converter switching frequency was limited to a few tens of kilo-Hertz (typically 20kHz to 50kHz) in early 1980's. The stray inductive and capacitive components in the power circuits and power devices still cause considerable transient effects, which in turn give rise to electromagnetic interference (EMI) problems. In late 1980's and throughout 1990's, further improvements have been made in converter technology. New generations of soft-switched converters that combine the advantages of conventional PWM converters and resonant converters have been developed. These soft-switched converters have switching waveforms similar to those of conventional PWM converters except that the rising and falling edges of the waveforms are 'smoothed' with no transient spikes. Unlike the resonant converters, new soft-switched converters usually utilize the resonance in a controlled manner. Soft-switching converters also provide an effective solution to suppress EMI and have been applied to DC-DC, AC-DC and DC-AC converters. Various forms of soft-switching techniques such as ZVS, ZCS, voltage clamping, zero transition methods etc. are addressed. The emphasis is placed on the basic operating principle and practicality of the converters without using much mathematical analysis.

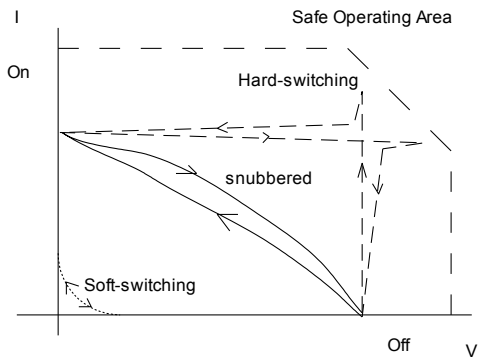


Fig.i Typical switching trajectorie of power switches.

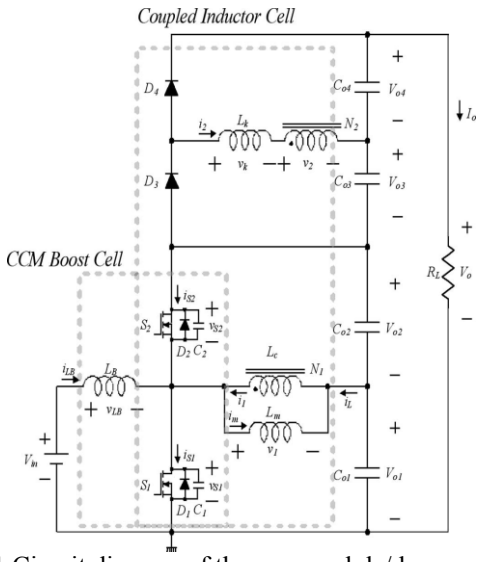


Fig.1.Circuit diagram of the proposed dc/dc converter.

In applications that require a voltage step-up function and a continuous input current, a continuous-conduction-mode (CCM) boost converter is often used due to its advantages such as continuous input current and simple structure. However, it has a limited voltage gain due to its parasitic components. Moreover, the reverse-recovery problem of the output diode degrades the system's performances. At the moment when the switch turns on, the reverse-recovery phenomenon of the output diode of the boost converter is provoked. The switch is submitted to a high current change rate and a high peak of reverse-recovery current. The parasitic inductance that exists in the current loop causes a ringing of the parasitic voltage, and then, it increases the voltage stresses of the switch and the output diode. These effects significantly contribute to increase switching losses and electromagnetic interference. The reverse-recovery problem of the output diodes is another important factor in dc/dc converters with high voltage gain]. In order to overcome these problems, various topologies have been introduced. In order to extend the voltage gain, the boost converters with coupled inductors are proposed. Their voltage gains are extended, but they lose a continuous input current characteristic and the efficiency is degraded due to hard switchings of power switches. For a continuous input current, current-fed step-up converters are proposed i. They provide high voltage gain and galvanic isolation. However, the additional snubbers are required to reduce the voltage stresses of switches.

In order to increase the efficiency and power conversion density, a soft-switching technique is required in dc/dc converters. A soft-switching dc/dc converter with high voltage gain, which is shown in Fig. 1, is proposed. A CCM boost cell provides a continuous input current. To increase the voltage gain, the output of the coupled inductor cell is laid on the top of the output of the CCM boost cell. Therefore, the high voltage gain is obtained without high turn ratio of the coupled inductor, and the voltage stresses of the switches are confined to the output voltage of the CCM boost cell.

A zero-voltage-switching (ZVS) operation of the power switches reduces the switching loss during the switching transition and improves the overall efficiency. The theoretical analysis is verified by a 200 W experimental prototype with 24-to-360 V conversion.

II. Analysis Of The Proposed Converter

Fig. 1 shows the circuit diagram of the proposed soft switching dc/dc converter with high voltage gain. Its key waveforms are shown in Fig. 2. The switches S1 and S2 are operated asymmetrically and the duty ratio *D* is based on the switch S1.

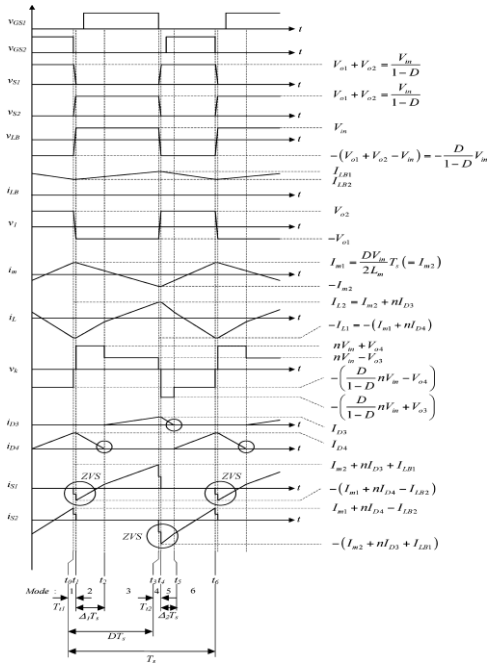


Fig.2. Key waveforms of the proposed converter.

D1 and D2 are intrinsic body diodes of S1 and S2 . Capacitors *C*1 and *C*2 are the parasitic output capacitances of S1 and S2 . The proposed converter contains a CCM boost cell. It consists of *LB* , S1 , S2, *Co*1 , and *Co*2 . The CCM boost cell provides a continuous input current. When the switch S1 is turned on, the boost inductor current *iLB* increases linearly from its minimum value *ILB*2 to its maximum value *ILB*1 . When the switch S1 is turned off and the switch S2 is turned on, the current *iLB* decreases linearly from *ILB*1 to *ILB*2 . Therefore, the output capacitor voltages *Vo*1 and *Vo*2 can be derived easily as

$$Vo1 = Vin \qquad (1)$$

$$Vo2 = D/(1-)D\ Vin\ . \qquad (2)$$

To obtain ZVS of S1 and S2 and high voltage gain, a coupled inductor *Lc* is inserted. The coupled inductor *Lc* is modeled as the magnetizing inductance *Lm*, the leakage inductance *Lk* , and the ideal transformer that has a turn ratio of 1:*n* (*n* = *N*2/*N*1). The voltage doubler consists of diodes D1 ,D2 and the output capacitors *Co*3, *Co*4 , and the secondary winding *N*2 of the coupled inductor *Lc* is on the top of the output stage of the boost cell to increase voltage gain. The coupled inductor current *iL* varies from its minimum value −*IL*1 to its maximum value *IL*2 . The operation of the proposed converter in one switching period *Ts* can be divided into six modes. Fig. 3 shows the operating modes. Before *t*0 , the switch S2 and diode D4 are conducting.

Mode 1 [t0, t1]: At *t*0 , the switch S2 is turned off. Then, the boost inductor current *iLB* and the coupled inductor current *iL*
start to charge *C*2 and discharge *C*1 . Therefore, the voltage *v*S1 across S1 starts to fall and the voltage *v*S2 across S2 starts to rise. Since the output capacitances *C*1 and *C*2 of the switches are very small, the transition interval *Tt*1 is very short and it can be neglected. Therefore, the inductor currents *iLB* and *iL* can be considered to have constant values during mode 1.

Mode 2 [t1, t2]: At *t*1 , the voltage *v*S1 across the lower switch S1 becomes zero and the lower diode D1 is turned on. Then, the gate signal is applied to the switch S1 . Since the current has already flown through the lower diode D1 and the voltage *v*S1 becomes zero before the switch S1 is turned on, zero-voltage turn-ON of S1 is achieved.

Since the voltage across the boost inductor *LB* is *V*in , the boost inductor current increases linearly from *ILB*2 .

Mode 3 [t2, t3]: At *t*2 , the secondary current *i*2 changes its direction. The diode current *i*D4 decreases to zero and the diode

D4 is turned off. Then, diode D3 is turned on and its current increases linearly. Since the current changing rate of D4 is controlled
by the leakage inductance of the coupled inductor, its reverse-recovery problem is alleviated. Since $v1$ is $-Vin$ and
vk is $nVin - Vo4$.

Mode 4 [t3, t4]: At $t3$, the lower switch S1 is turned off. Then, the boost inductor current iLB and the coupled inductor current iL start to charge $C1$ and discharge $C2$. Therefore, the voltages vS1 and vS2 start to rise and fall in a manner similar to that in mode 1.

Mode 5 [t4, t5]: At $t4$, the voltage vS2 across the upper switch S2 becomes zero and the diode D2 is turned on. Then, the gate signal is applied to the switch S2 . Since the current has already flown through the diode D2 and the voltage vS2 becomes
zero before the switch S2 is turned on, zero-voltage turn-ON of S2 is achieved. Since the voltage across the boost inductor LB is $-(Vin/(1 - D) - Vin)$, the boost inductor current decreases linearly from $ILB1$. Since $v1$ is $DVin/(1 - D)$ and vk is $-Vo3 - nDVin/(1 - D)$.

Mode 6 [t5, t6]: At $t5$, the secondary current $i2$ changes its direction. The diode current iD3 decreases to zero and the diode
D3 is turned off. The reverse-recovery

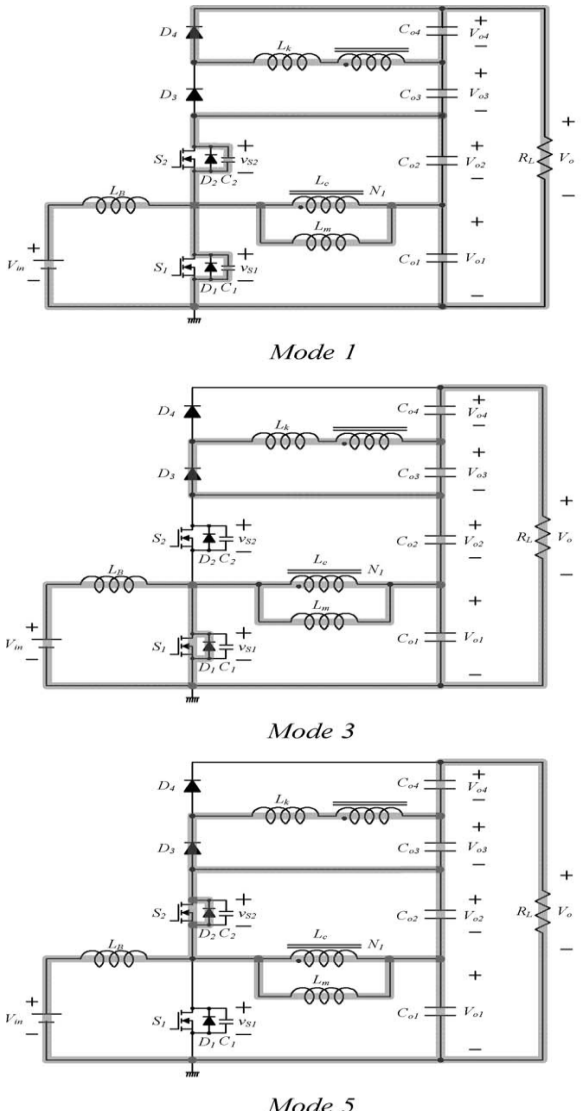
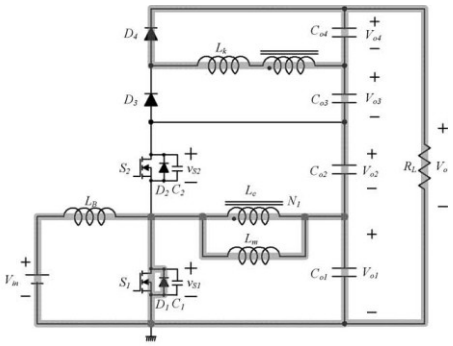
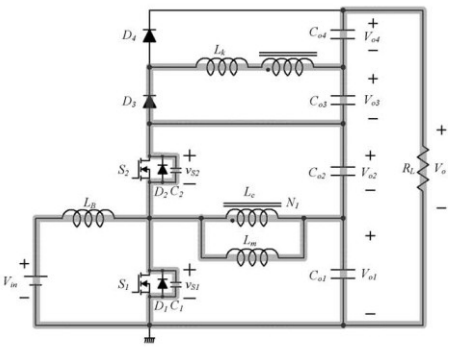


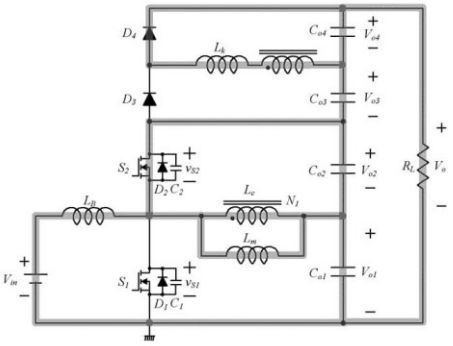
Fig. 3. Operating modes.



Mode 2



Mode 4



Mode 6

problem of D3 is also alleviated due to the leakage inductance of L_c . Then, the diode D4 is turned on and its current increases linearly. Since $v1$ is $DV\text{in}/(1-D)$ and vk is $Vo4 - nDV\text{in}/(1-D)$.

III. Characteristic And Design Parameters

A. Input Current Ripple

The input current ripple ΔILB can be written as

$$\Delta ILB = ILB1 - ILB2 = DV\text{in}Ts/LB \quad . \qquad (3)$$

To reduce the input current ripple ΔILB below a specific value $I*$, the inductor LB should satisfy the following condition:

$$LB > DV\text{in}Ts/I* \qquad (4)$$

B. Voltage Gain

the voltage gain of the proposed converter is obtained by

$$Vo/V\text{in}=(1/1-D)+ (nD\,(1-\alpha)/(D-\alpha\,(2D-1))\,(1-D+\alpha\,(2D-1))). \qquad (5)$$

Fig. 4 shows the voltage gain according to duty cycle D: (a) the voltage gain according to$D$ under α=0.1 and several n values;

(b) the voltage gain according to$D$ under n = 3 and several α values. As α increases, the voltage gain decreases. Namely, larger Lk reduces the voltage gain. On the assumption that α is small, the voltage gain of (34) can be simplified as follows:

$$Vo/V\text{in}=(1 + n)/(1 – D) \quad (6)$$

C. ZVS Condition

The ZVS condition for S2 is given by $Im2 + nI\text{D}3 + ILB1 > 0$ (7) Fig. 5. Normalized voltage stresses according to duty cycle. (a) Under $\alpha = 0.1$ and different n values. (b) Under $n = 3$ and different α values. from where, it can be seen that the ZVS of S2 is easily obtained. For ZVS of S1 , the following condition should be satisfied:

$$Im1 + nI\text{D}4 > ILB2 \quad (7)$$

On the assumption that α is small, ID4 and $ILB2$ can be simplified as follows:

$$I\text{D}4 =2Io/1 – D \quad (8)$$

$$ILB2 =(n + 1)\, Io/1 − D− \Delta ILB/2 . \quad (9)$$

From (8) and (9), the inequality (7) can be rewritten by

$$Im1 + 2nIo/(1 – D)>(n + 1)\, Io/(1 – D)− \Delta ILB/2 . \quad (10)$$

Since $Im1$, Io , and $DILB$ are all positive values, the inequality (40) is always satisfied for n>1. From (7) and (8), it can be seen that ZVS conditions for S1 and S2 are always satisfied. Moreover, dead times of two switches S1 and S2 should be considered.

the gate signal should be applied to the switch before the current that flows through the anti parallel diode changes its direction. Namely, the leakage inductance Lk should be large enough for the current to maintain its direction during dead times of two switches, S1 and S2 . This condition can determine the minimum value of the leakage inductance., the leakage inductance Lk should satisfy the following condition:

$$Lk > nV\text{in}DTs\,(1 –(1 − 2\Delta*1/D)\text{^}2)\,/8I \quad (11)$$

Where $\Delta* 1$ is a predetermined minimum value of$\Delta 1$. The leakage inductance of the coupled inductor also alleviates the reverse recovery problem of output diode. Large leakage inductance can remove the reverse-recovery problem but it reduces the voltage gain as shown in Fig. 4(b).

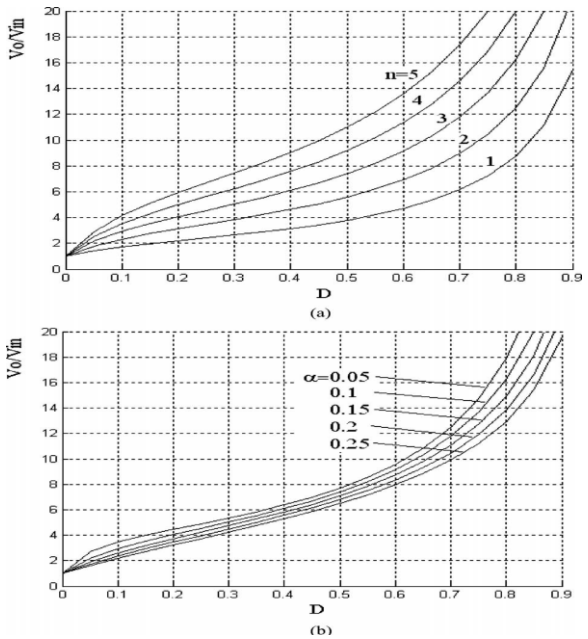


Fig..4 Voltage gain according to duty cycle. (a) Under $\alpha = 0.1$ and different values. (b) Under $n = 3$ and different α values.

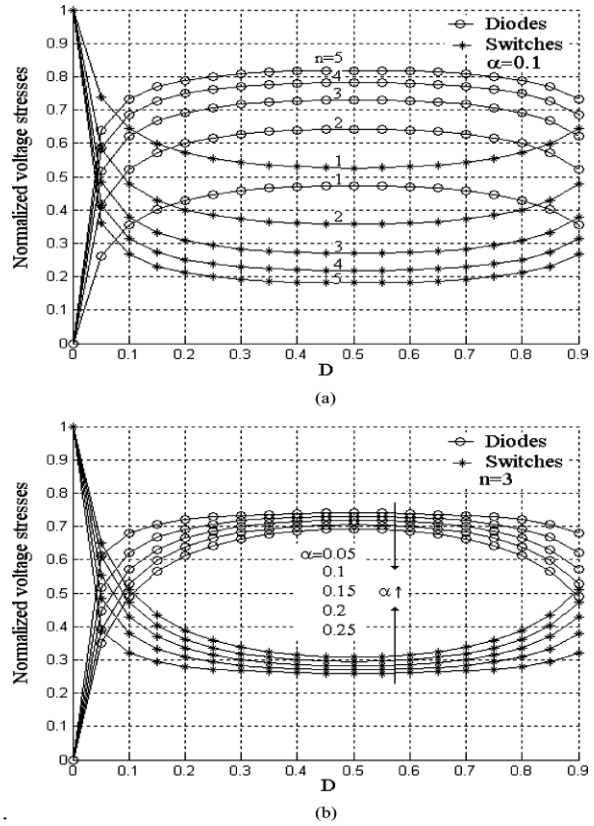


Fig.5 Normalized voltage stresses according to duty cycle. (a) Under $\alpha = 0.1$ and different n values. (b) Under $n = 3$ and different α values.

D. Voltage Stress of Devices

Generally, high output voltage will impose high-voltage stress across the switching devices in dc/dc converters. In the proposed dc/dc converter, the voltage stresses across the switching devices are smaller than the output voltage. Maximum values of vS1 and vS2 are confined to the output of the CCM boost cell as follows:

$$v\text{S1,Max} = v\text{S2,Max} = Vo1 + Vo2 = V\text{in}/(1 - D) \quad (12)$$

The maximum voltage stresses vD3,Max and vD4,Max of the output diodes are given by

$$v\text{D1,Max} = v\text{D2,Max} = Vo3 + Vo4 = Vo - V\text{in}/(1 - D) \quad (13)$$

Fig. 5 shows the voltage stresses of the power switches and the output diodes that are normalized with Vo .

IV. Experimental Results:

The prototype soft-switching dc/dc converter with high voltage gain is implemented with specifications of $n = 5$, $V\text{in} = 24$ V, $Vo = 360$ V, $LB = 154$ μH, $Lk = 74$ μH, $Co1 = Co2 = Co3 = Co4 = 47$ μF, $Lm = 105$ μH, $fs = 100$ kHz, and $Po = 200$ W. Fig. 6 shows PSPICE simulation results. Fig. 7 shows the experimental waveforms of the prototype of the proposed converter. Fig. 7(a) shows the inductor currents iLB and iL , and the voltage vS1. It can be seen that the experimental waveforms agree with the theoretical analysis and the simulation results in Fig. 6. The input current is continuous.

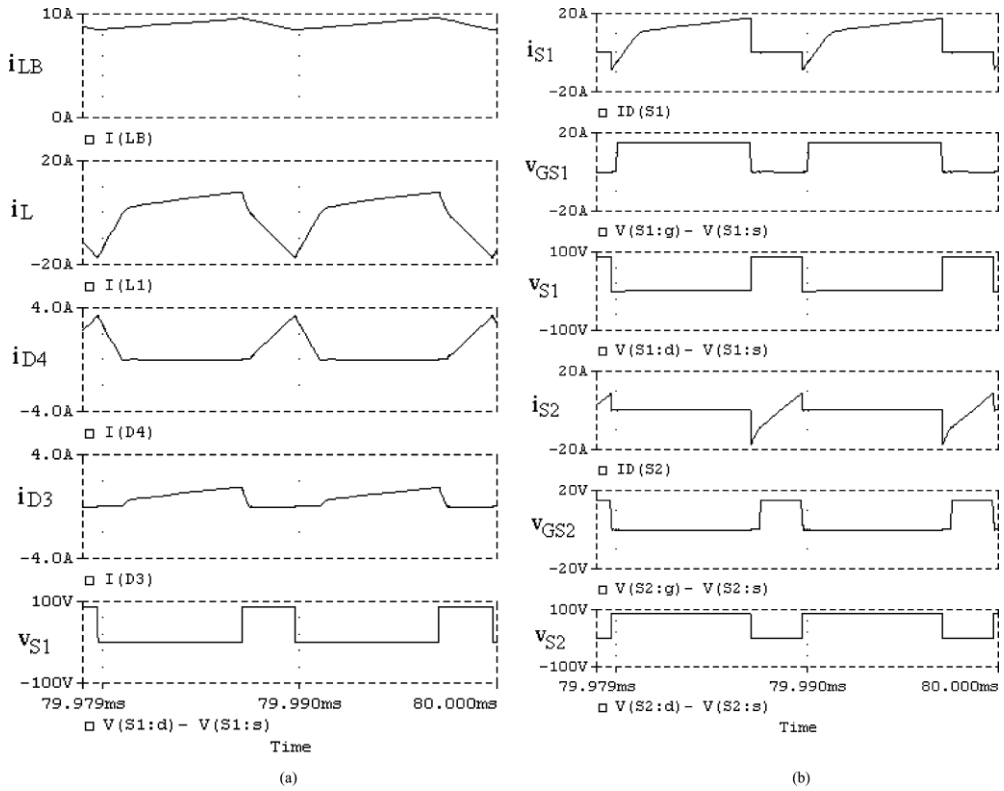


Fig. 6 Simulation results. (a) *iLB*1 , *iL* , *i*D3, *i*D4, and *v*S1 . (b) *i*S1 , *vG*S1 , *v*S1 , *i*S2 , *vG*S2, and *v*S2 .

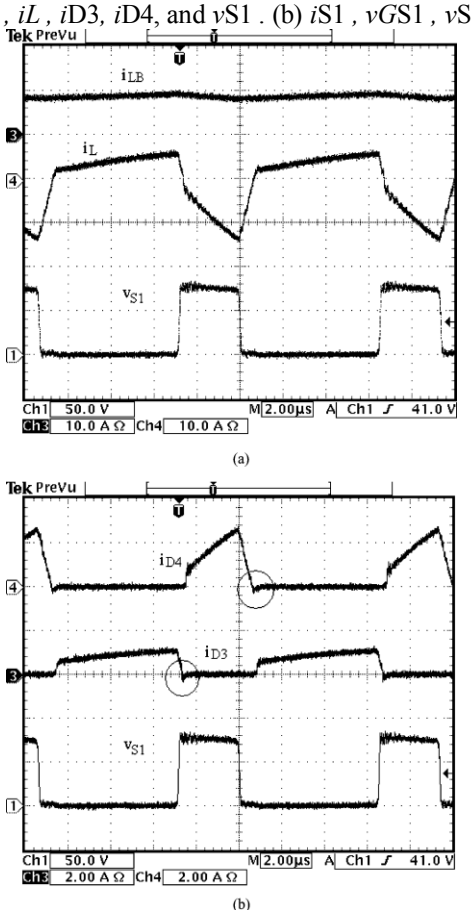


Fig. 7 Experimental waveforms. (a) *iLB*1 , *iL* , and *v*S1. (b) *i*D3, *i*D4, and *v*S1 .

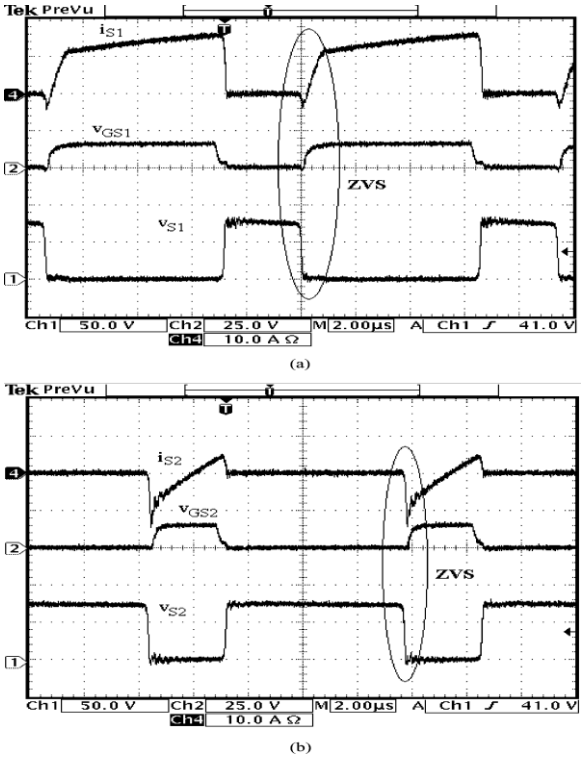


Fig. 8. ZVS of S1 and S2 . (a) *i*S1 , *vG*S1, and *v*S1 . (b) *i*S2 , *vG*S2, and *v*S2 .

The ripple component of the input current can be controlled by *LB*. Fig. 7(b) shows the experimental results of the turn-OFF current of diodes D3 and D4 . It is clear that the reverse-recovery current is significantly reduced and the reverse-recovery problem is alleviated dramatically by the leakage inductance of the coupled inductor *Lc*. Fig. 8. Shows the ZVS of S1 and S2 . (a) *i*S1 , *vG*S1, and *v*S1 . (b) *i*S2 , *vG*S2, and *v*S2 . Fig. 8 shows the ZVS of S1 and S2. In Fig. 8(a), the voltage *v*S1 across the switch S1 reaches zero before the gate pulse *vG*S1 is applied to S1 . Fig. 8(b) shows the ZVS of S2 . Fig. 9 shows the measured efficiency of the proposed converter. It exhibits an efficiency of 96.4% at full-load condition. Due to its soft-switching characteristic and alleviated reverse-recovery problem, the overall efficiency was improved by around 2%compared with the conventional high step-up boost converter with a coupled inductor.

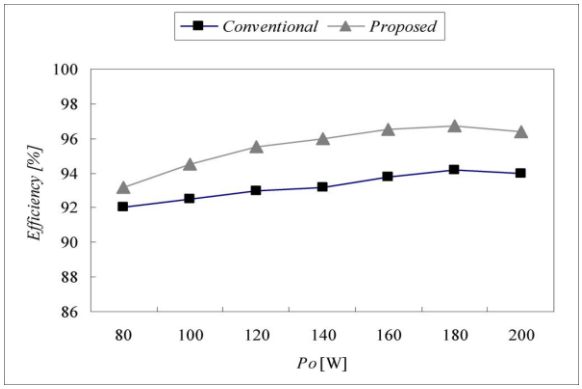


Fig. 9 Measured efficiency.

V. Conclusion

A soft-switching dc/dc converter with high voltage gain has been proposed in this paper. A simple and effective method to alleviate rectifier reverse- recovery problems in CCM boost converters is proposed in this paper the proposed converter can minimize the voltage stresses of the switching devices and lower the turn ratio of the coupled inductor. It provides a continuous input current, and the ripple components of the input current can be controlled by using the inductance of the CCM boost cell. Soft switching of power switches and the alleviated reverse-recovery problem of the output rectifiers improve the overall efficiency.

References:

[1] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1184–1194, Sep. 2004.

[2] R. J. Wai, W. H. Wang, and C. Y. Lin, "High-performance stand-alone photovoltaic generation system," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 240–250, Jan. 2008.

[3] C. Wang and M. H. Nehrir, "Power management of a standalone wind/photovoltaic/fuel cell energy system," *IEEE Trans. Energy Convers.*, vol. 23, no. 3, pp. 957–967, Sep. 2008.

[4] R. J. Wai and W. H. Wang, "Grid-connected photovoltaic generation system," *IEEETrans. CircuitsSyst. I, Reg. Papers*, vol. 55, no. 3, pp. 953–964, Apr. 2008.

[5] R. J.Wai, C. Y. Lin, R. Y. Duan, and Y. R. Chang, "High-efficiency power conversion system for kilowatt-level distributed generation unit with low input voltage," *IEEE Trans. Ind. Electron.*, vol. 55, no. 10, pp. 3702–3714, Oct. 2008.

[6] K. Kobayashi, H. Matsuo, and Y. Sekine, "Novel solar-cell power supply system using a multiple-input DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 53, no. 1, pp. 281–286, Feb. 2006.

[7] S. K. Mazumder, R. K. Burra, and K. Acharya, "A ripple-mitigating and energy-efficient fuel cell power-conditioning system," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1437–1452, Jul. 2007.

[8] C. Wang, Y. Kang, B. Lu, J. Sun, M. Xu, W. Dong, F. C. Lee, and W. C. Tipton, "A high power-density, high efficiency front-end converter for capacitor charging application," in *Proc. IEEE APEC*, Mar. 2005, vol. 2,pp. 1258–1264.

[9] Z. Qun and F. C. Lee, "High-efficiency, high step-up DC–DC converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 65–73, Jan. 2003.

[10] X. Kong and A. M. Khambadkone, "Analysis and implementation of a high efficiency, interleaved current-fed full bridge converter for fuel cell system," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 543–550, Mar. 2007.

[11] S. Pradhan, S. K. Mazumder, J. Hartvigsen, and M. Hollist, "Effects of electrical feedbacks on planar solid-oxide fuel cell," *ASME J. Fuel Cell Sci. Technol.*, vol. 4, no. 2, pp. 154–166, May 2007.

[12] W. Choi, P. N. Enjeti, and J. W. Howze, "Development of an equivalent circuit model of a fuel cell to evaluate the effects of inverter ripple current," in *Proc. IEEE APEC*, 2004, vol. 1, pp. 355–361.

[13] G. Fontes, C. Turpin, S. Astier, and T. A. Meynard, "Interactions between fuel cells and power converters: Influence of current harmonics on a fuel cell stack," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 670–678,Mar. 2007.

[14] S. K. Mazumder, S. K. Pradhan, J. Hartvigsen, M. R. von Spakovsky, and D. F. Rancruel, "Effects of battery buffering on the post-load-transient performance of a PSOFC," *IEEE Trans. Energy Convers.*, vol. 22, no. 2, pp. 457–466, Jun. 2007.

Prakash Parvatham : II-M.Tech at Sri Venkateshwara Engineering College ,Suryapet his interested in Power Electronics and power systems.

Dr.A.Srujana:
B.Tech(Electrical),M.Tech(PE),ph.D(HVDC).**:** Working as Professor& Head of EEE at Sri Venkateshwara Engineering College ,Suryapet her interested in Power Electronics and Power Systems .