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Assessing Cracks And Interconnect Reliability In Flipchips

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Abstract: *One of the most common forms of failures observed in flipchips brittle thin films subjected to stress is cracking. The crack growth rate depends on intrinsic film properties, stress and some environmental factors. In part 1 of this paper, we investigate central crack on different material planes. The planes are made from silicon, copper, aluminum, polyamide and silicon nitride. Each plane is 1.0m x 0.4m and has a crack length of 0.04m. Because of symmetry only 0.5m and o.2m of the plate is used. They are subjected to a normal stress of 100MPa. A 2D FEA model is developed and ANSYS software is used to calculate the MODE I Stress Intensity Factor (SIF) on each material plane. The SIF of the materials are compared and a result is arrived at which creates room for recommendation. In part 2, the same material types and sizes are used but with central holes of diameter 0.2m each. Each plate is subjected to a normal stress of -1N/m2. Ansys, GUI was used in the computation of the displacements, maximum and minimum stresses. From the results we noted that different materials have different displacements and stress levels.*
Keywords: *ANSYS, Displacement, Flipcchip, Interconnect, Stress Intensity Factor.*

I. INTRODUCTION

With the continued market need of low cost, portable consumer electronic products with greater functionality there is increasing demand for electronic packaging that is smaller, lighter and less expensive. Flip chip is important in that it is an enabling technology for these products. The term "Flip Chip" is commonly used to refer to an assembly method used to make a direct electrical connection by placing the chip face down onto a substrate, circuit board, or carrier. The electrical connection between the chip I/O and substrate is achieved using conductive materials, such as solder, conductive epoxy, metallurgy bump for example gold and anisotropic conductive adhesives. Among these materials, solder is the most commonly used in flip chip assemblies. In flip chip technology, the interconnection between the die and carrier in flip chip packaging is done using a conductive bump placed directly on the die surface. The bumped die is then flipped and placed face down so that the bumps connect directly to the carrier. This is not the case with wire-bond technology.

Engineers strive to optimize chip geometry in flip chips by designing the thinnest possible chips because it not only reduces the weight of the package but also its reliability. Being able to determine the stress intensity factor enables the designers come up with ways of minimizing the cracking of the chip. This is done during chip processing and packaging.

Carter, Wawryznek and Ingraffea developed a time saving method to replace the tedious and repetitive work of crack growth simulation and coded in the computer program FRANC3D [1]. However, the code has limited stress analysis capability and must be used in conjunction with finite element method program such as ANSYS. The software used for stress analysis in this study is ANSYS Release 14.0. It is a popular code used by many experts in various industries for finite element analysis. We opted for ANSYS Release 14.0 because it can design a 2D model. Dr. Paul Wawryznek developed the early FRANC codes in Cornell Fracture Group to simulate the process of nucleation and crack propagation in a structure; and to compute the stress intensity factor. Today, his students in the same group continue to research and update the codes [2].

Apart from cracks, holes also exist in flipchip packages**.** Via are normally fitted through the holes on the chips. These holes experiences stresses and deformations near them and this can result in the cracking of the chips. The uniform, homogenous plates used in this simulation are symmetric about the horizontal axis in both geometry and loading. Because of this, the state of stress and deformation below the horizontal centerline is a mirror image of what is above the centerline. This is the same for vertical centerline. Boundary conditions enabled us use only a quarter of the plate for finite element model.

II. CALCULATION OF STRESS INTENSITY FACTORS (SIF) USING THE FINITE ELEMENT METHOD

When a crack exists in a structure, stress is concentrated at the tip of the crack but the stress concentration do not account for the fracture behavior at the tip of a crack since as the radius of the curvature of the crack tip approaches zero, the stress level could become infinity, which is not a real property of a loaded structure. As an alternative to describe the structural strength at the crack tip appropriately, the stress-intensity factor, K, is a parameter to characterize "the stress field ahead of a sharp crack in a test specimen or a structural

member". The parameter, K, is related to the nominal stress level (σ) in the structural member and the size of the crack (a), and has units $[GPa\sqrt{mm}]$.

In general, the relation is represented by

$$K = \sigma\sqrt{a}\,P \quad \ldots\ldots (1)$$

Where P is a geometrical parameter which depends on the structural member and crack. According to Barsom [3], "all structural members or test specimens that have flaws can be loaded to various levels of K. This is analogous to the situation where unflawed structural or mechanical members can be loaded to various levels of stress, σ".

The stress field near crack tips can be categorized as: Mode I: tension/opening mode, Mode II: sliding mode and Mode III: tearing mode. Each one of them is characterized by a "local mode of deformation". This is illustrated in Figure 26. The opening mode, I, is related to local displacement in which the crack surfaces move directly apart . Although these three modes can be superposed to "describe the most general case of crack tip deformation and stress fields" [4], Mode I is the primary focus of this paper.

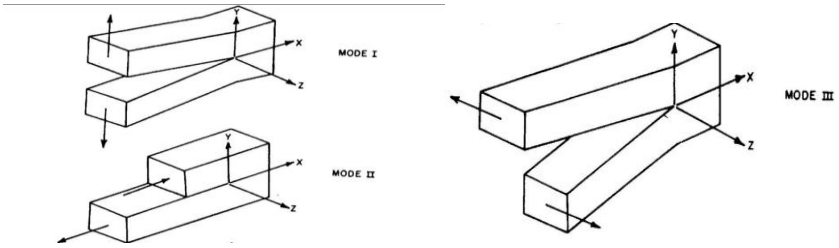

Fig.1 Local mode of deformation.

In general, stress intensity factor depends on: The stress induced on a structure, the crack size and the geometry of the crack.

2.1 Fracture toughness (K_{IC})

Fracture toughness is a property which describes the ability of a material containing a crack to resist fracture, and is one of the most important properties of any material for many design applications. It is a measured material property found using standard specimens that are loaded until the crack extends. K is a function of the crack geometry and the applied loading. If $K>K_{IC}$, the crack will propagate. Fracture toughness can also combine fracture with fatigue to determine cycles of repeated loading until crack will propagate to failure.

2.2 Analysis approach (Included crack in the finite element model)

This is considered the most accurate approach since it includes stress redistribution. For crack propagation would need to evaluate the initial crack, then extend the crack and re-analyze to obtain K versus crack length. The process becomes more difficult if the crack length is not known ahead of time

2.3 Linear Elastic Stress Analysis of 2D cracks.

Homogeneous and isotropic materials with cracks have stress surrounding the crack tip analyzed assuming linear elastic material behavior. Linear Elastic Fracture Mechanics (LEFM) method assumes the plastic region near crack tip is much smaller than the dimensions of the crack and the structural member. This is a very important concept, scientists and engineers call it small-scale yielding [5], since it simplifies stress analysis near the tip.

The coordinates (r, θ) for the stress components are shown in Figure 2 below.

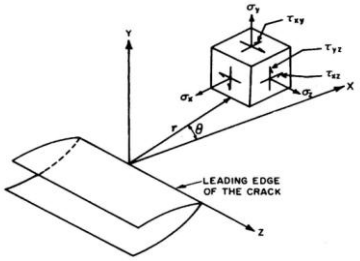

Fig. 2 Coordinate systems for the stress components [5].

III. METHODOLOGY

3.1Simulation 1

ANSYS Tutorial, 2D fracture analysis release 7.0 by Dr. A.-V. Phan, University of south Alaba helped us develop new ideas about central cracks in chips. The chips are made from different materials namely; silicon, copper, aluminum, silicon nitride and polyamide. They are rectangular plates each 1m x 0.4m but because of symmetry only 0.5m x 0.2m part of plate is used in simulation and central crack lengths of 0.04m each. Each plate is subjected to a normal stress of 100MPa

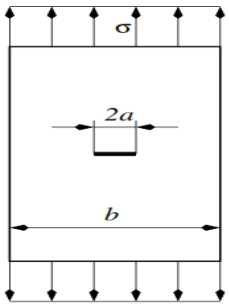

Fig.3 Through-thickness crack.

Here, **a** is the crack length and **b** plate width. **σ** is the stress applied on the plate.

3.2 Simulation 2

Holes exist in flipchip packages**.** Via are normally fitted through the holes on the chips. These holes experiences stresses and deformations near them and this can result in the cracking of the chips.

The uniform, homogenous plates used in this simulation are symmetric about the horizontal axis in both geometry and loading. Because of this, the state of stress and deformation below the horizontal centerline is a mirror image of what is above the centerline. This is the same for vertical centerline. Boundary conditions enabled us use only a quarter of the plate for finite element model. This is shown in figure below. It also facilitated remeshing the problem. During remeshing, the geometry does not change but the number and location of nodes and elements do. Symmetry is not important for small problems.

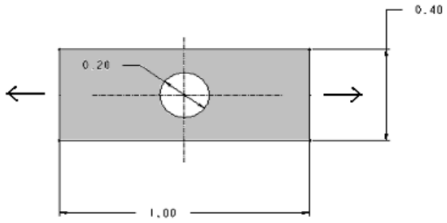

Fig.4 plate with a central hole

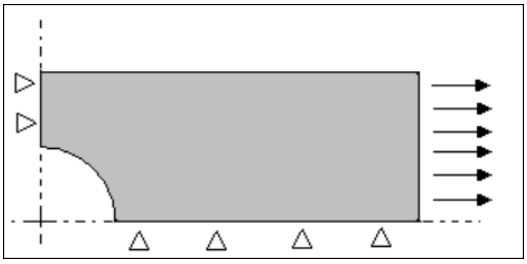

Fig.5 Quadrant used for analysis

ANSYS Tutorial, 2D fracture analysis release 14.0 helped us develop new ideas about stress development and deformation around the holes accommodating the via which may result to cracks in chips in multilevel flipchip packages. The chips are made from different materials namely; silicon, copper, aluminum, silicon nitride and polyamide. They are rectangular plates each 1m x 0.4m but because of symmetry only 0.5m x 0.2m part of plate is used in simulation and central holes of diameter 0.2m each. Each plate is subjected to a normal stress of -1N/m^2. These dimensions are clearly shown in the figure above.

IV. RESULTS AND DISCUSSIONS

TABLE 1: mechanical and thermal properties of materials

Material	Young's modulus (Gpa)	Poisson's ratio	Density (x1000kg/m^3)	Fracture toughness (mpa-$m^{1/2}$)	Melting point (˚c)	Boiling point(˚c)	CTE (x10^{-6})
Silicon	150	0.17	2.329	0.62-1.25	1420	3265	2.6
Copper	110	0.33	8.94	N/A	1085	2562	16.6-17.6
Aluminum	70	0.33	2.71	14-28	660.3	2519	23
Polyamide	2.1	0.4	1.1	0.7-1.1	190-350	N/A	75-100
Silicon nitride	166	0.23	3.29	5.7, 6.1	1900	N/A	3.2

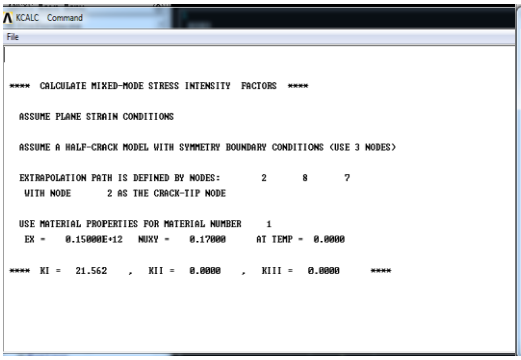

Fig.6 Calculated mode I SIF in silicon

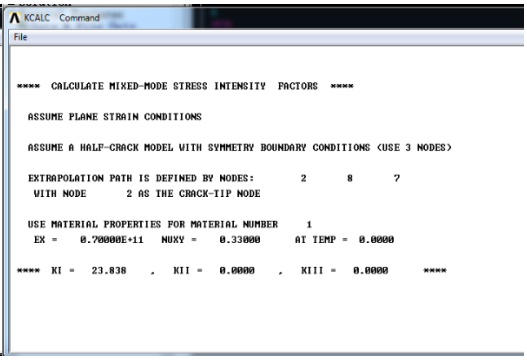

Fig.7 Mode I SIF for aluminum

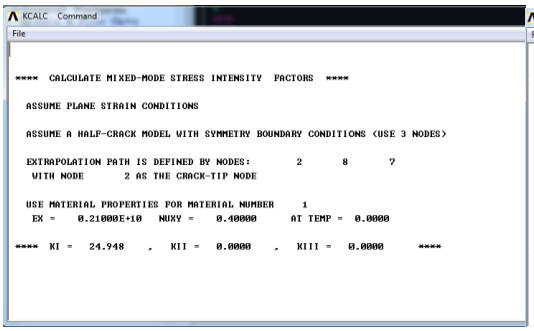

Fig.8 Mode I SIF for polyamide

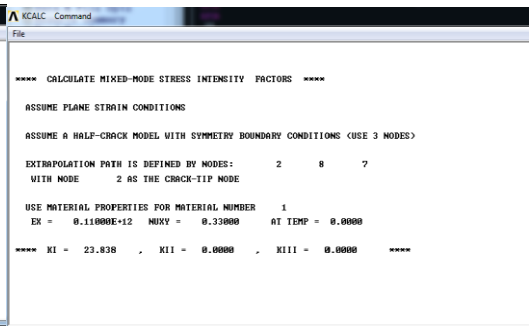

Fig.9 Mode I SIF of copper

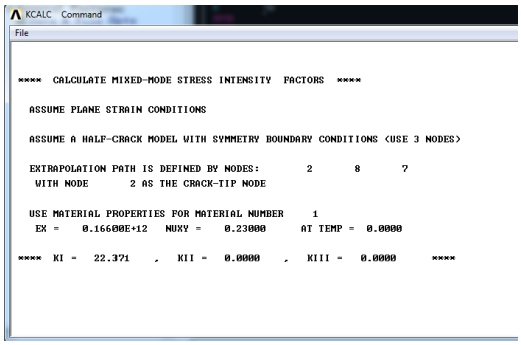

Fig.10 Mode I SIF of cracked silicon nitride

It was observed that different materials used have different MODE I SIFs. Silicon material had the lowest MODE I SIF of 21.562 while polyamide which is a dielectric material had the highest MODE I SIF of 24.948. It was noted that copper and aluminum had the same values of MODE I SIF of 23.838 each, therefore we recommend that they are used interchangibly where mechanical properties are concerned. Silicon nitride has a SIF of 22.371. These values are greater than the fracture toughness values in table 1 above, therefore crack propagation will occur leading to open circuits in flipchips hence lowering the reliability of products.

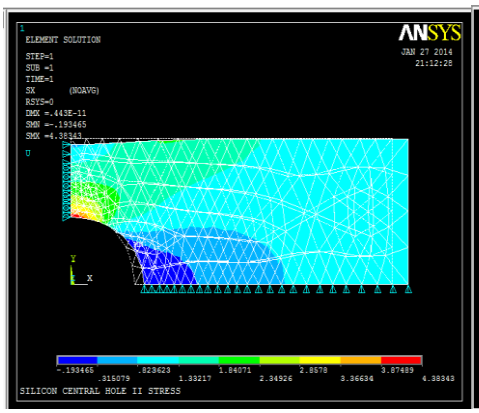

Fig.11 Silicon's central-hole results.

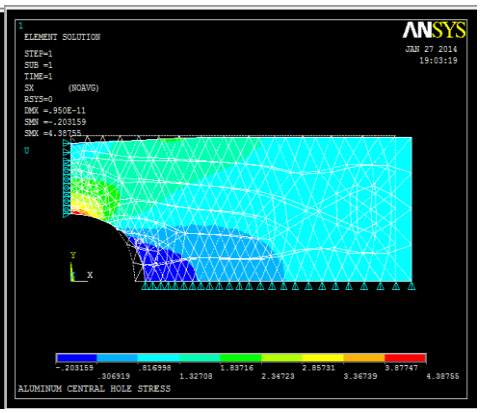

Fig.12 Aluminum's central-hole results

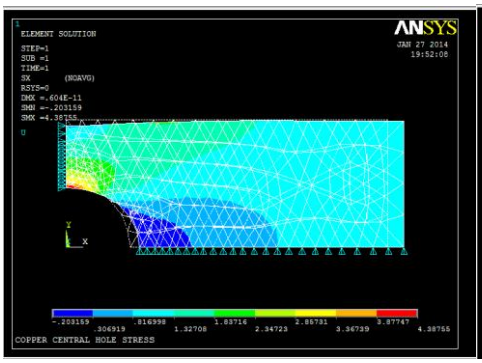

Fig.13 Copper's central-hole results

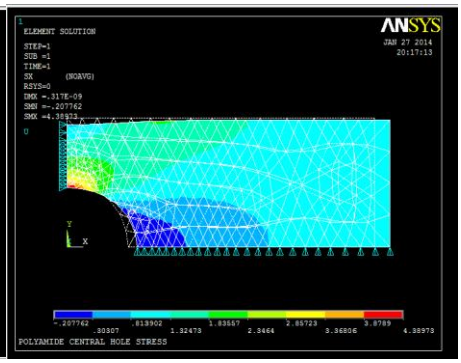

Fig.14 Polyamide central-hole results

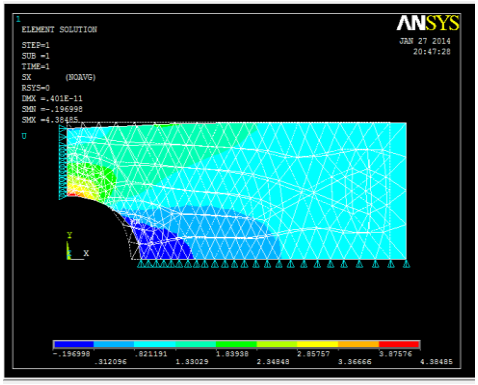

Fig.15 Silicon nitride central hole results

Differences in displacements, minimum and maxium stresses for different materials are evident on the figures. Polyamide had the highest stress difference while silicon nitride had the lowest.

V. Conclusion

It was observed that different materials used had different MODE I SIFs.

Silicon material had the lowest MODE I SIF of 21.562 while polyamide which is a dielectric material had the highest MODE I SIF of 24.948. It was noted that copper and aluminum had the same values of MODE I SIF of 23.838 each .From simulation 2 different materials have different displacements, maximum and minimum stresses. Copper and aluminum had the same values of minimum and maximum stresses of -0.203159 and 4.38755 respectively.

TABLE 2: summary of results for central hole planes.

Material	Young's modulus(GPa)	Poisson's ratio	MODE I SIF	Displacements(m)	Minimum stress(SMN)	Maximum stress(SMX)	Δ stress
Silicon	150	0.17	21.562	0.443E-11	-0.193465	4.38343	4.576895
Aluminum	70	0.33	23.838	0.950E-11	-0.203159	4.38755	4.590709
Copper	110	0.33	23.838	0.604E-11	-0.203159	4.38755	4.590709
Polyamide	2.1	0.4	24.948	0.317E-9	-0.207762	4.38973	4.597492
Silicon nitride	166	0.23	22.371	0.401E-11	-0.196998	4.38485	4.581848

The advantages of this paper include: all the required results were obtained from one diagram, different stress levels are clearly shown especially in simulation 2 and the simulator ANSYS was simple to use. The limitations were: there was no undo command in the software and this lead to long time simulation, work had to be saved at each step not to be lost and this was time consuming too. This paper can be used to determine the strength of materials especially when cracks develop. Proper ways can be put in place to ensure the cracks does not propagate and lead to failure in electronic devices where flipchip technology has been used. This has not been discussed in this paper.

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