IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)
e-ISSN: 2278-1676,p-ISSN: 2320-3331, Volume 9, Issue 3 Ver. I (May – Jun. 2014), PP 98-103
www.iosrjournals.org

Voltage Unbalance Mitigation Using Positive Sequence Series Compensator

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Abstract: *Voltage Unbalance is a common type of power quality problem. Sequence components occur during unbalance in three phase system. For this reason unbalance is assessed with respect to the sequence components present in the system. Voltage unbalance may adversely affect power system components connected to the system. In this paper, for symmetric and asymmetric faults, positive sequence voltage is taken as reference to generate PWM pulses and is given to the VSI to mitigate the unbalance present in the power system.*
Keywords: *Faults, Poly-phase system, Positive Sequence voltage, Series Compensator, Voltage Unbalance.*

I. Introduction

The primary source of voltage unbalance of less than 2 percent is single-phase loads on three-phase circuits [1]. Voltage unbalance can also be the result of blown fuses in one phase of a three phase capacitor bank. Severe voltage unbalance (greater than 5%) can result from single phasing conditions. Symmetrical and asymmetrical faults are also major sources of unbalance.

Unbalance in a power system is related to the power system stability problem. Unbalance may cause excessive drawl of reactive power, mal-operation of equipment, inaccurate measurement in measuring instruments and shortening of life span of different appliances [2]. Reactive power compensation is required for individual phase will differ from each other. Performance of FACTs controller degrades during voltage unbalance. During current unbalance negative sequence component appears. It increases net current in some phase and decreases net current in other phase. This results in unequal loss in phases and unequal heating [3]. Three phase motors draw unbalanced current from unbalanced current from unbalanced supply system. In such situation, unequal heating and oscillation in torque hamper motor performance. In ungrounded system, unbalance causes neutral shifting. This hampers accurate operation of relays and circuit breakers along with other related problems.

IEC Standards restrict the permissible voltage unbalance on induction motors to 1 percent [4] and require a deratingof a machines, if unbalance is greater. ANSI, NEMA and IEC proposed limits for both current and voltage unbalance [4] as

- Continuous voltage unbalance - 5%
- Continuous current unbalance – 10%

Supply unbalance compensation can be achieved by different means. One approach to balance and regulate the voltage at critical load terminals is to use series compensators known as Dynamic Voltage Restorers (DVRs) [3]-[4]. Several control algorithms are applied for the DVR in the literature. The pre-fault method is used to balance the load voltage based on a fault detector to freeze the output from the Phase Locked Loop (PLL) circuit when fault occurs. The frozen angle is then used to restore the old balanced load voltages [5]-[6]. The lack of negative sequence detection in this method leads to the phase-oscillation in case of single line faults. The other control methodology is the post-fault, which is based on the disturbance extraction to reconstruct a three- phase balanced voltage. This approach is achieved by two different ways, the first is by using a synchronized PLL with the post fault voltage [7] and the second is the symmetrical components method [8]. While the post-fault PLL is a fast control algorithm, it cannot avoid phase jumps on the load voltage at fault occurrence, which can disturb the phase-angle controlled rectifier loads. On the other hand, the symmetrical components method suffers from the delay time introduced by Fortescue transform calculation [9], the inaccuracy and parameter dependence of the filter sequence [10]. Yet, this technique is suitable for minimum voltage or minimum energy operation strategies. Moreover, the symmetrical components method can tolerate the effect of phase jump by using the pre-fault phase angle [2]. This paper presents an efficient control for the series compensator based on positive sequence reference voltage extraction method.

II. Voltage Unbalance

Voltage unbalance is sometimes defined as the maximum deviation (V_{max}) from the average of the three phase voltage (V_{avg}), divided by the average of the three phase voltage, expressed in percentage as given in equation (1).

$$\%V_{ub} = \left(\frac{V_{max} - V_{avg}}{V_{avg}}\right) \times 100 \quad \text{……} \quad (1)$$

Unbalance often defined in the standards using symmetrical components. The ration of either negative (V^n) or zero sequence components (V^z) to the positive sequence component (V^p), expressed in percentage as expressed in equations (2a) and (2b).

$$\%V_{ub} = \left(\frac{V^n}{V^p}\right) \times 100 \quad \text{……} \quad (2a)$$

$$\%V_{ub} = \left(\frac{V^z}{V^p}\right) \times 100 \quad \text{……} \quad (2b)$$

where, V_{ub} is the magnitude of voltage unbalance in percentage.

III. System Description

Simplified block diagram of an overall system is depicted in Fig. 1. Here unbalance is created by simulating the symmetrical and asymmetrical faults. $V_{sabc}$is the three phase source voltage. It becomes unbalanced, during fault conditions as shown in Fig. 1. Positive sequence reference voltage controlled series compensator is connected in the power system, in order to prevent unbalance at the load side. Under unbalance condition, there exists positive, negative and zero sequence components. In a balanced system, positive sequence component alone exist.Thus to obtain balanced load voltage (V_{labc}), positive sequence voltage component is taken as reference. From the reference voltage, PWM signals are generated and are given to the VSI, to mitigate the voltage unbalance.

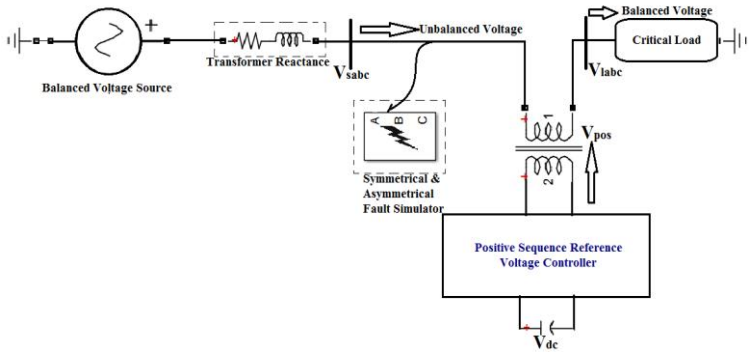

Fig.1. Simplified system block diagram.

IV. Positive Sequence Reference Voltage Generation

Design and implementation of positive sequence reference voltage controller is simple. During asymmetric fault condition, fundamental components are decomposed into positive, negative and zero sequence components asgiven in equation (3).

$$\begin{bmatrix} V^p \\ V^n \\ V^z \end{bmatrix} = \left(\frac{1}{3}\right) \begin{bmatrix} 1 & a & a^2 \\ 1 & a^2 & a \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} \quad \text{……} \quad (3)$$

Here, V^p is a positive sequence voltage component, V^n is a negative sequence voltage component and V^z is a zero sequence voltage component. 'a' is the rotation vector(e^{j120}).V_{sa}, V_{sb} and V_{sc} are the three phase source voltage of phases a, b and c respectively.

Positive sequence three phase voltage (V^p_{abc}) is extracted using sequence analyzer block. Then it is transformed to stationary reference frame as expressed in equation (4).

$$\begin{bmatrix} V^p_\alpha \\ V^p_\beta \end{bmatrix} = \left(\frac{2}{3}\right) \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} V^p_a \\ V^p_b \\ V^p_c \end{bmatrix} \quad \text{……} \quad (4)$$

Using Park Transformation αβ variables are transformed to dq components as expressed in equation (5)

$$\begin{bmatrix} V^p_d \\ V^p_q \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ (-)\sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} V^p_\alpha \\ V^p_\beta \end{bmatrix} \quad \text{……} \quad (5)$$

Here, ωt is the angular displacement of Park Transformation. Then, direct axis of the positive sequence voltage is compared with the compared with the reference voltage. Consequently, V^p_{dq} is transformed to the αβ reference frame $V^p_{\alpha\beta}$ as given in equation (6).

$$\begin{bmatrix} V_{\alpha}^{p} \\ V_{\beta}^{p} \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & (-)\sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} V_{d}^{p} \\ V_{q}^{p} \end{bmatrix} \quad \text{(6)}$$

Then, $V_{\alpha\beta}^{p}$ are transformed into a-b-c frame (V_{abc}^{p}), as expressed in equation (7).

$$\begin{bmatrix} V_{a}^{p} \\ V_{b}^{p} \\ V_{c}^{p} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -1/2 & \sqrt{3}/2 & 1 \\ -1/2 & -\sqrt{3}/2 & 1 \end{bmatrix} \begin{bmatrix} V_{\alpha}^{p} \\ V_{\beta}^{p} \\ V_{0}^{p} \end{bmatrix} \quad \text{(7)}$$

Lastly, V_{abc}^{p} is compared with the actual source voltage (V_{sabc}) as given in equations (8).

$$er_{(a)} = V_{a}^{p} - V_{sa} \quad \text{(8a)}$$

$$er_{(b)} = V_{b}^{p} - V_{sb} \quad \text{(8b)}$$

$$er_{(a)} = V_{c}^{p} - V_{sc} \quad \text{(8c)}$$

Subsequently, error ($er_{(abc)}$) is compared with the high frequency carrier signal and PWM signals to the VSI are generated.

V. Positive Sequence Controller Design

Implementation of block diagram of a Positive Sequence Voltage Component Extraction based controller for Matlab simulation is shown in Fig 2. Under unbalanced or fault condition, source voltage (V_{sabc})is decomposed into positive, negative and zero sequence voltage as given in equation (3). From this, positive sequence voltage component (V_{abc}^{p}) is extracted and is transformed to αβ reference variables. Then, $V_{\alpha\beta}^{p}$ is transformed to dq reference frame variables (V_{dq}^{p}) as shown in Fig. 2. As direct axis of the voltage component is proportional to its magnitude, it is easy to obtain required magnitude for voltage unbalance mitigation. Direct axis voltage magnitude is compared with the positive sequence reference voltage (V_{ref}^{p}). Error of the reference voltage is summed with the actual fundamental magnitude in direct axis. Thus, peak magnitude is obtained at any fault condition. Then, V_{dq}^{p} is transformed to a-b-c reference frame variables (V_{abc}^{p}). Consequently, V_{abc}^{p} is compared with the actual source voltage (V_{sabc}). Error voltage ($er_{(abc)}$) is compared with the carrier signal to obtain PWM signals.

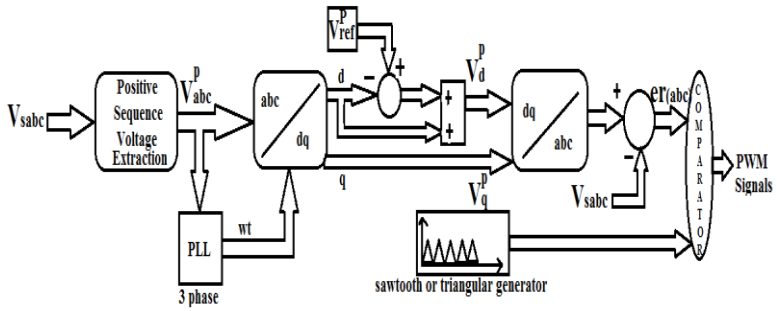

Fig.2. Positive sequence reference voltage controller.

VI. Simulation Study

Simulation circuit of mitigating the voltage unbalance using positive sequence reference voltage method is shown in Fig 3. Here, series compensator is used for voltage unbalance mitigation. Balanced three phase voltage with rms phase voltage magnitude of 300 V is used for simulation. Critical passive load is taken for analysis. During fault condition, three phase voltage becomes unbalanced, ie., either voltage magnitude or its phase sequence may not be equally distributed. Also, voltage will be lesser than fundamental positive magnitude due to ground fault. This unbalanced voltage is not intended to use for all domestic, industrial and some critical loads. This can be eliminated here, with a positive sequencereference voltage based series compensator as shown in Fig.3.

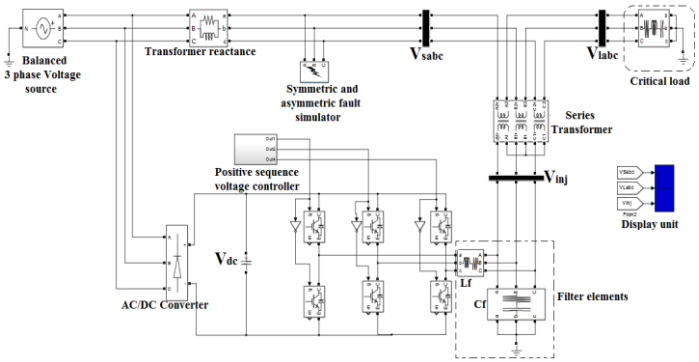

Fig.3. Positive sequence reference voltage based compensation.

When fundamental magnitude (V_{sabc})is lesser thanpositive sequence reference voltage (V_{ref}^{p}), series compensator injects the difference in voltage(V_{inj}). As a result, load voltage (V_{labc})get balanced. As positive sequence component alone is used for compensation technique, overall response of the system is very fast and accurate in computational process. Capacitor voltage(V_{dc}) is maintained constant by drawing energy from the source through AC/DC converter.Thus at any instant of fault condition, load voltage get compensated with this capacitor.

VII. Simulation Results

Here, voltage unbalance mitigation is done for both symmetric and asymmetric faults, with a ground fault resistance of 0.001Ω.

A. Single line to ground fault

Simulated source voltage during single line to ground fault is shown in Fig.4a. Single line to ground fault is initiated in phase B at time t = 100 ms. At once, voltage magnitude of Phase B is reduced to 41V from 244.9 V as shown in Fig.4a. Also, it is observed that there exist negative sequence component with $68\angle -59.68$ and zero sequence components with $68\angle 60$. Difference in the voltage between positive sequence reference voltage (V_{ref}^{p}) and actual source voltage (V_{sabc}) is injected from DVR as shown in fig.4b. At last, load voltage is compensated as shown in Fig.4c.

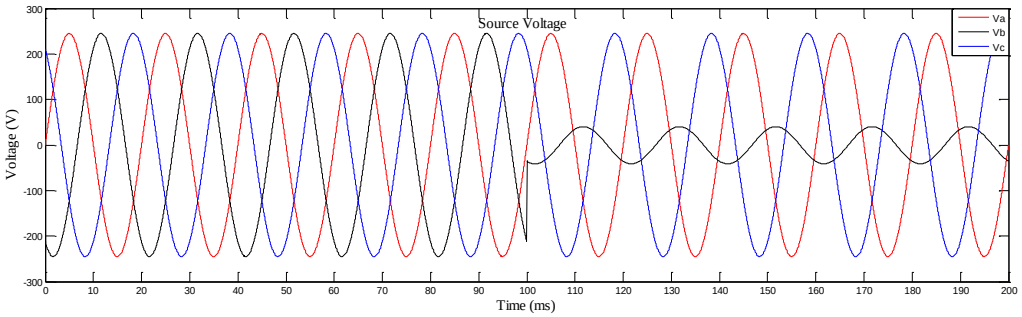

Fig.4a. Source voltage with single line to ground fault.

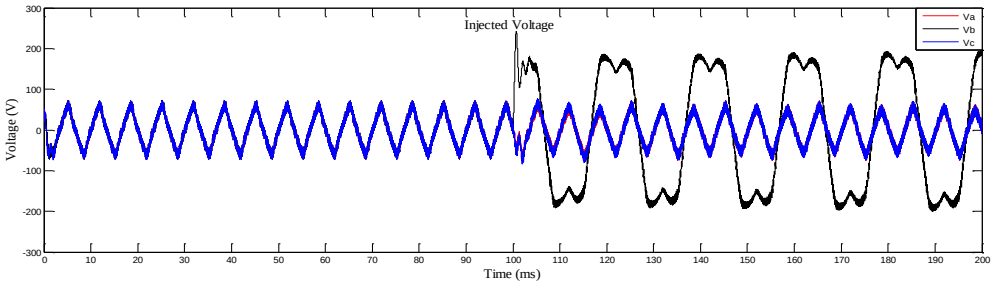

Fig.4b. DVR injected voltage during single line to ground fault.

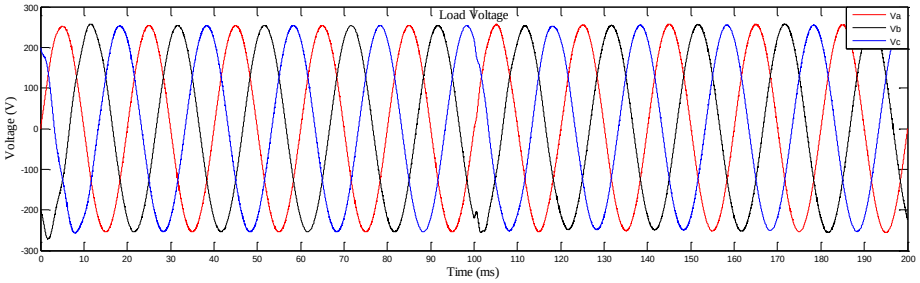

Fig.4c. Compensated load voltage during single line to ground fault.

B. Double line to ground fault

Simulated source voltage during double line to ground fault is displayed in Fig.5a. Double line to ground fault is initiated in phase Aand B, at time t = 100 ms. At once, voltage magnitude of Phase A is reduced to 36V from 244.9 V and Phase B is reduced to 34 V from the fundamental magnitude of 244.9, as shown in Fig.5a. Also, it is observed that the magnitude of positive sequence component is reduced to 22.5∟-1.69 from 244.9∟0. As known under unbalanced voltage condition, additional to positive sequence component, there exists negative and zero sequence components. Thus for the simulated double line to ground fault, there exist negative sequence component with 79.9∟-120 and zero sequence components with 62.8∟120. Difference in the voltage between positive sequence reference voltage (V_{ref}^{p}) and actual source voltage (V_{sabc}) is injected from DVR as shown in fig.5b. At last,load voltage gets compensated as shown in Fig.5c. Also, existence of positive and negative sequence component are completely eliminated at load side.

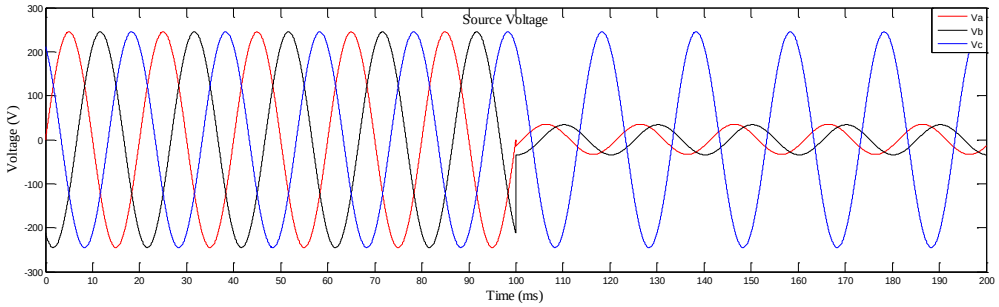

Fig.5a. Source voltage with double line to ground fault.

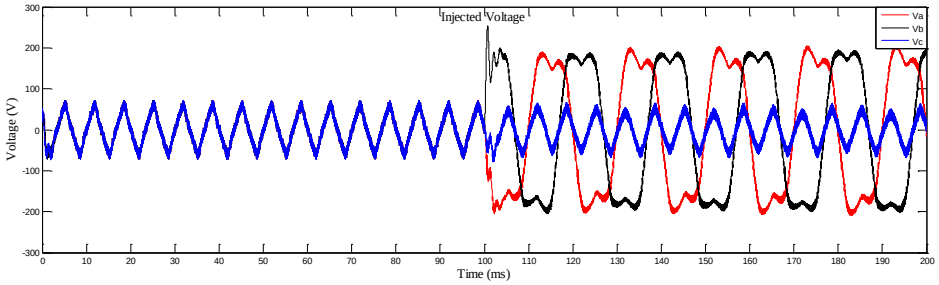

Fig.5b. DVR injected voltage during double line to ground fault.

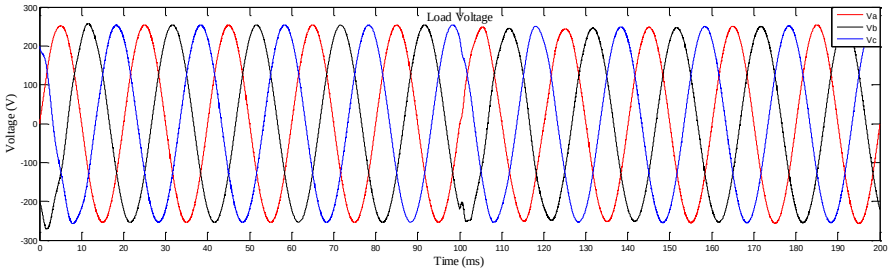

Fig.5c. Compensated load voltage during double line to ground fault.

C. Symmetric fault

Simulated source voltage during symmetricfault is shown in Fig.6a. Symmetric fault is initiated in at time t = 100 ms. At once, voltage magnitude of all the phases A, B and C is reduced to 22.5 V from 244.9 V as shown in Fig.6a. Due to symmetric fault, there will not be existence of negative and zero sequence components. Difference in the voltage between positive sequence reference voltage (V_{ref}^{p}) and actual source voltage (V_{sabc}) is injected from DVR as shown in fig.6b. At last, load voltage gets compensated as shown in Fig.6c.

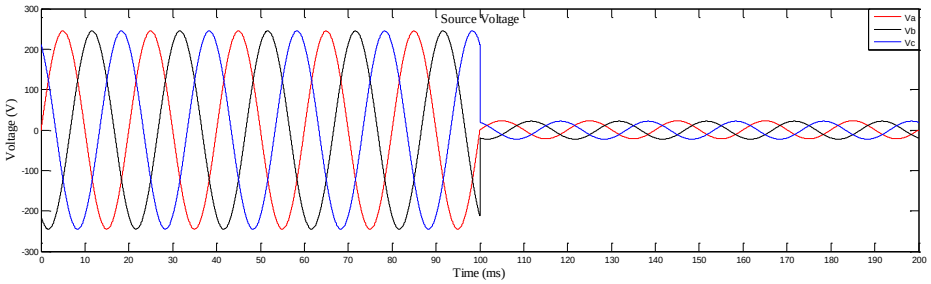

Fig.6a. Source voltage with symmetric fault.

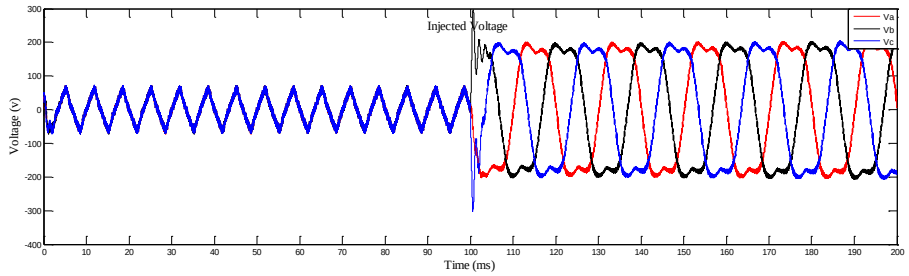

Fig.6b. DVR injected voltage during symmetric fault.

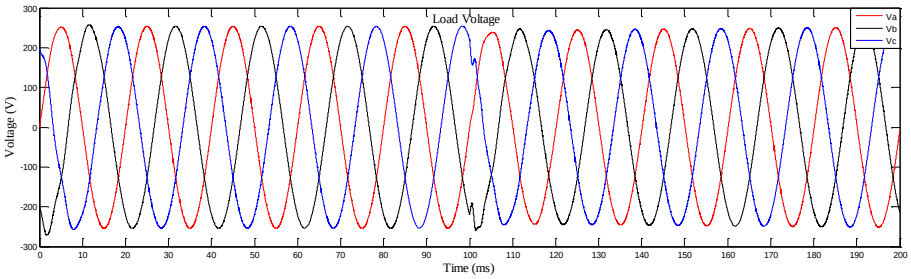

Fig.6c. Compensated load voltage during symmetric fault.

VIII. Conclusion

A method to compensate the voltage unbalance is developed and implemented using MATLAB Simulink.With this positive sequence component extraction method, voltage unbalance is completely eliminated as per European Standard EN 50160 (1994).

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