# Performance Analysis of Hybrid Ge-Si Based Mosfet with **Different Gate Oxide Thickness and Material**

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Abstract: In this paper we have designed and simulated Hybrid MOSFET(with two substrate material) and compared the drain characteristics with basic MOSFET( single substrate material ). Here we observed that drain current starts saturating at much earlier time for hybrid MOSFET than basic MOSFET but the drain current value is very low in hybrid MOSFET. To increase the drain current value in the hybrid MOSFET different measures like gate oxide material  $(HFO_2)$  and variable oxide thickness have been used which leads better performance. Design, Simulation and analysis have been done with the help of Visual TCAD. Keyword: N channel MOSFET, Hafnia(HFO<sub>2</sub>), Hybrid MOSFET, Visual TCAD

#### I. Introduction

MOS (Metal-Oxide-Semiconductor), transistor is looks like a "sandwich" which consist of a semiconductor layer (usually a slice wafer from a single crystal of silicon), a layer of silicon dioxide (the oxide) and a layer of control electrode which can be either metal or polysilicon. The conducting region is known as the "channel". The channel exists between the source(S) and drain(D).[1]

Silicon dioxide has traditionally been used as the gate insulator. The gate oxide serves as insulator between the gate and channel, which should be made as thin as possible to increase the conductivity of the channel and performance of the transistor when transistor is on and to reduce subthreshold leakage when the transistor is off.[2]Silicon dioxide has moderate value of dielectric constant. The capacitance of oxide layer is proportional to the dielectric constant and inversely proportional to dielectric thickness. A higher dielectric thickness reduces the quantum tunneling[3] current through the dielectric between the gate and the channel.

The reduction in dimension of the gate dielectric, results the increase of capacitance and speed of the device. Further, reduction in thickness of SiO<sub>2</sub> above acceptable limit will cause increase in subthreshold leakage current. High dielectric constants materials can resolved this problem. Hafnium Dioxide has relatively large energy band gap and a good thermal stability as compared to Si [4]. Hafnium dioxide is a high-dielectric, low absorption material usable for coatings in UV (~250 nm) to IR (~10µm) regions.HfO2 or Hafnia is the inorganic colorless solid and stable compounds of hafnium and also an intermediate which provides Hf metal. It has relatively large energy band-gap and a good thermal stability as compared to Si. It is an electrical insulator with a band-gap of 5.8eV [5-7]. HfO<sub>2</sub> is inert and respond with strong acids and strong bases and dissolves slowly in HF acid to give fluorohafnate anions. The use of  $HfO_2$  results in many advantages over SiO<sub>2</sub> [8].

#### **Design And Simulation** II.

The general processes to design 180nm MOSFET involving simulation of fabrication process, structure and mesh and electrical testing. The first step for designing the MOSFET is to draw the 'device drawing' using Visual TCAD, further meshing is done. The structure of the hybrid MOSFET is shown in figure 1.



Figure. 1 Simulated Hybrid MOSFET structure

It has the single Npolysilicon gate with two substrates material silicon and germanium. The doping profiles used in the designis listed as bellow :

Name	Profile	Туре	Peak Conc. / cm <sup>-3</sup>	Char. L / µm
Substrate	uniform	Acceptor	$5 \times 10^{16}$	-
Channel	gaussian	Acceptor	$1 \times 10^{18}$	0.1
LDD_S/LDD_D	gaussian	Donor	$2 \times 10^{19}$	0.02
Source/Drain	gaussian	Donor	$1 \times 10^{20}$	0.04

# III. Result And Analysis

We have simulated and listed drain current value for single substrate (Si substrate ) MOSFET and Hybrid MOSFET which is as follow:

Table. 1 Comparison of Drain current for Hybrid MOSFET and basic MOSFET					
	Drain current for	Drain Current For Si			
Gate Voltage	Hybrid MOSFET	substrate			
0	-1.48E-06	-1.92E-16			
0.2	4.84E-07	0.0003137			
0.4	5.78E-07	0.00054992			
0.6	6.45E-07	0.00068657			
0.8	6.88E-07	0.00073882			
1	7.12E-07	0.00075449			
1.2	7.26E-07	0.00076305			
1.4	7.36E-07	0.00076988			
1.6	7.46E-07	0.00077586			
1.8	7.55E-07	0.00078129			
2	7.64E-07	0.00078627			

Table. 1 Comparison of Drain current for Hybrid MOSFET and basic MOSFET

The drain characteristic curve for both the MOSFETs based of above listed table are shown below:









From the above results we find that the drain saturation current level for Hybrid MOSFET is lower than the single substrate MOSFET. For high speed and power electronics application the drain current should be at high level saturation value. This can be achieved by reducing the thickness of gate oxide layer upto acceptable limit which give the simulated result graph as follows :

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Drian Voltage	Drain current for tox = 4nm	Drain Current for tox = 3nm	Drain Current for tox = 2nm	Drain Current for tox = 1nm		
0	-1.48E-06	-1.92E-06	-2.77E-06	-5.49E-06		
0.2	4.84E-07	6.62E-07	9.19E-07	1.76E-06		
0.4	5.78E-07	8.00E-07	1.11E-06	2.09E-06		
0.6	6.45E-07	9.04E-07	1.26E-06	2.36E-06		
0.8	6.88E-07	9.78E-07	1.38E-06	2.58E-06		
1	7.12E-07	1.02E-06	1.46E-06	2.77E-06		
1.2	7.26E-07	1.05E-06	1.51E-06	2.90E-06		
1.4	7.36E-07	1.06E-06	1.54E-06	2.98E-06		
1.6	7.46E-07	1.07E-06	1.55E-06	3.01E-06		
1.8	7.55E-07	1.08E-06	1.56E-06	3.02E-06		
2	7.64E-07	1.09E-06	1.57E-06	3.03E-06		

### Table 2: Drain Current of Hybrid MOSFET for different Oxide thickness



Figure 4: Drain Characteristics curve of Hybrid MOSFET with variation in oxide thickness

From the above result we find that by reducing thickness of oxide layer upto acceptable limit the drain current increases. Now we can also increase the drain current value by using high dielectric constant material oxide  $HFO_2$  layer in the place of  $SiO_2$  layer as mentioned above. The Simulated results are given as follows:

Drian Voltage	Drain Current for HfO2	Drain Current for SiO2
0	-7.32E-06	-1.48E-06
0.2	2.07E-06	4.84E-07
0.4	2.33E-06	5.78E-07
0.6	2.57E-06	6.45E-07
0.8	2.76E-06	6.88E-07
1	2.89E-06	7.12E-07
1.2	2.99E-06	7.26E-07
1.4	3.06E-06	7.36E-07
1.6	3.09E-06	7.46E-07
1.8	3.10E-06	7.55E-07
2	3.11E-06	7.64E-07

## Table 3: Drain current of Hybrid MOSFET with different gate oxide material



Figure 5: Drain characteristics curve with different gate oxide material

From above we analysis that by using high dielectric constant material oxide like HFO<sub>2</sub> layer drain current value increases.

# IV. Conclusion

We have investigated that the hybrid substrate MOSFET provide a much earlier saturating low valued drain current as compared to single substrate MOSFET. In many application we need earlier saturating higher valued drain current. Our Simulation and analysis reflect that the desirable outcome of drain current can be achieved by reducing the gate oxide  $(SiO_2)$  layer thickness upto threshold limit and/or replacing the  $SiO_2$  with HfO<sub>2</sub> layer.

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# References

- [1]. Stanley Wolf and Richard N. Tauber, "Silicon processing for the VLSI ERA VOLUME III", Lattice Press, 1986
- [2]. Neil H. E. Weste, David Money Harris, "CMOS VLSI Design ", fourth edition, Addison-Wesley, 2011.
- [3]. Razavy, Mohsen (2003). Quantum Theory of Tunneling. World Scientific. ISBN 981-238-019-1.
- [4]. J. C. Lee, "Single-layer thin HfO2 gate dielectric with n+ polysilicon," Proc. of IEEE Symposium on VLSI Technology, NJ, June 2000, pp. 44-45.
- [5]. H. S. Baik and S. J. Pennycook, "Interface structure and nonstoichiometry in HfO2 dielectrics," IEEE Applied Physics Letter, vol. 85, 2009, pp. 672- 674.
- [6]. A. P. Huang, Z. C. Yang, and Paul K. Chu, "Hafnium based Highk gate dielectrics," Proc. of Advances in Solid State Circuits Technologies, April 2010, pp. 333-350.
- [7]. 'A Product catalogue,' READE Advances Materials, England, 2005.
- [8]. M. Fadel and O. Azim, "A study of some optical properties of hafnium dioxide thin films and their applications," J. of Applied Physics Materials Science and Processing, vol. 66, no. 3, pp. 335- 343, 1997.