# A Novel Approach to Generate Multilevel Current Waveform Using Inductor Cells

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**ABSTRACT:** The paper proposes the multilevel current waveform generation with a new configuration Hbridge Current Source Inverter (CSI) from a single DC power source. In this new topology, the H-bridge inverter acts as main circuit and the inductor cells acts as an auxiliary circuit in the generation of multilevel current waveform. This paper describes five level current waveform generation & the sinusoidal pulse width modulation (SPWM) technique is associated with three level shifted multicarrier is introduced in these topology to control the intermediate levels of multilevel current waveform. The main and auxiliary circuits are connected in parallel to generate a multilevel current waveform. The design and performance is evaluated by using MATLAB Simulation.

Keywords - Current-Source Inverter (CSI), H-bridge, Inductor cell, Multi-level current waveform.

## I. INTRODUCTION

RECENTLY energy generated from clean, efficient and environmentally friendly sources has become one of the major challenges for engineers and scientists [1], [2], [3], [8]. In distributed Power generation application, as most renewable energy sources, such as Photo Voltaic (PV) systems, deliver DC (Direct Current) power; the generated power must be converted to ac power and is fed into the grid through grid connected inverters [8],[9],[10]. Recent development of high performance semiconductor power switches such as MOSFETs and IGBTs increases the research interest in high power converters, such as multilevel Voltage Source Inverter (VSIs) and its dual, multilevel Current Source Inverter (CSIs) [11],[12],[13]. Various international standards, like IEEE 1547, IEEE929, and EN-61000-3-2, impose requirements on the inverter's output power quality, i.e., harmonic currents and Total Harmonics Distortion (THD) of the output current. Multilevel CSI is one of the effective solutions to tackle such problems. Control of the grid connected CSI is comparatively simpler than its Counterpart, VSI. A grid-connected CSI can buffer the output current from the grid-voltage fluctuation, generates a predetermined current to the power grid without ac-current-feedback loops, and can achieve a highpower-factor operation. Its output current is less affected by a grid voltage, and the CSI has inherent short-circuit protection abilities [7], [8]. Moreover, the discrete diodes connected in series with the power switches to obtain unidirectional power switches in the CSI will be unnecessary because new IGBTs with reverse-blocking capability (reverse-blocking IGBTs) are emerging [4], [5]. Few topologies of the multilevel CSIs have been proposed by researchers and engineers. A conventional method to generate the multilevel current waveform is by paralleling some three-level H-bridge CSIs, as shown in Fig. 1 [9]–[11].

This topology is a dual circuit of a cascade multilevel VSI [9]. However, the requirement of many isolated dc-current sources with their complex, bulky, and costly isolation transformers and inductors is a problem introduced by this configuration.

Another topology of the multilevel CSI is obtained by applying a multi-cell topology of the CSI (or multi-rating inductor multilevel CSI [9]), which is a dual converter of a flying-capacitor-based full- bridge multilevel VSI [12]–[14]. However, this topology has a drawback with its bulky intermediate inductors and complexity for balancing control of the intermediate-level currents. Some control methods have been proposed for balancing control of the intermediate-level currents in [13] and [14], but very large in size of the intermediate inductors (100 mH) are still used. These cumbersome inductors will be costly and limit the application of the inverter.



Bai and Zhang [9] presented the configuration of a single-rating inductor multilevel CSI that is the dual structure of an improved diode-clamped multilevel VSI. Noguchi and Suroso [15], [16] presented a commonemitter configuration of the multilevel CSI obtained by connecting two-level CSI modules in parallel with the three-level common-emitter CSI. This configuration has a great advantage over conventional approaches because all of the power switches are connected at a common-emitter point or an identical potential line. This topology needs only a single isolated gate-drive circuit to drive all power switches of the inverter; hence, the complexity of the gate drive circuits can be moderated. Unfortunately, the requirement of many split dc-current sources is an apparent disadvantage of this topology.

This paper proposes a new circuit configuration of Cascaded Current Source H-Bridge Inverter. In this new topology a basic H-bridge CSI working as a main circuit is connected in parallel with inductor cells working as auxiliary circuits. The inductor cells generate the intermediate levels of the multilevel output-current waveform, with no additional external dc-power sources. The operational performance of the proposed H-Bridge CSI is examined MATLAB software simulations.





Fig. 2. Proposed inductor cell circuit.

Fig. 2 shows a configuration of the proposed inductor cell circuit composed by four unidirectional power switches  $Q_{C1}$ ,  $Q_{C2}$ ,  $Q_{C3}$  and  $Q_{C4}$ , and an inductor  $L_C$  connected across the cell circuit. The newly proposed configuration of the CSI can be obtained by connecting in parallel with a single or more inductor cells, as shown in a schematic diagram of the proposed H-bridge CSI in Fig. 3. A five-level current waveform is obtained by connecting a single inductor cell in parallel with the main three-level H-bridge CSI.



It is necessary to connect a capacitor across the load, because the inverter works as a current source and the load usually has an inductive component. The capacitor also functions to filter the harmonic components, e.g., switching harmonic components, of the PWM multilevel output current [17].

#### III. OPERATION PRINCIPLE

The relation between the level number of the output current waveform (M) and the number of the inductor cells (N) can be formulated as follows:

 $M = 2^{(N+1)} + 1 \tag{1}$ 

Fig. 6 shows the configuration of five level CSIs using the proposed strategy. For M-level current waveform, if the dc current source of the main H-bridge CSI is assumed to have an amplitude I, the current flowing through the Nth inductor cell  $I_{Lc (i)}$  is expressed as follows:

$$I_{Lc(i)} = I / 2^{i}$$
, where  $i = 1, 2, 3, .... N$  (2)

The output five current levels are +I, +I/2,0, -I/2, and –I. The inductor cells generate intermediate-level currents of the multilevel output waveform from the basic three-level current of the H-bridge CSI. It utilizes the charging and the discharging operation modes of the inductor. The charging operation mode of the inductor  $L_C$  is conducted when the switches  $Q_{C1}$ ,  $Q_{C3}$  are turned on, while the switches  $Q_{C2}$ ,  $Q_{C4}$  are turned off. A current  $I_{Lc} = I/2$  flows through the power switches  $Q_{C1}$ ,  $Q_{C3}$  and  $Q_{C4}$  and by Turing off  $Q_{C1}$  and  $Q_{C3}$ . The stored energy in the inductor is discharged to the load as a current I/2. The circulating current modes occurred when the inductor cell deliver a null current to keep a constant current in the inductor cell. Similar operation modes occurred for the negative cycle of the output current waveform.

Table-I lists switching states in proposed five level current waveforms. Power device utility and average switching frequency between  $Q_{C1}$ ,  $Q_{C2}$  and  $Q_{C3}$ ,  $Q_{C4}$  in circulating modes of the inductor cell current is one of the considerations to use redundant switching states for I, 0, and –I output current generation.

#### i. DC-Current Source

In the proposed Cascaded H-Bridge CSI, the dc-current source is in dispensable. In order to test the proposed Cascaded H-Bridge CSI, the dc-current source is obtained by employing a chopper with a smoothing inductor ( $L_i$ ) connected with the H-bridge CSI. The chopper consists of a controlled switch ( $Q_c$ ) that regulates the dc current flowing through the smoothing inductor as the dc input current  $IL_i$ .

A free-wheeling diode  $(D_j)$  is used to keep continuous current flowing through the smoothing inductor. The chopper works as a regulated dc-current source. Fig. 6 shows the five level current waveform generated CSI configuration with the chopper based dc-current source. The power source  $(V_{in})$  may be batteries system, photovoltaic (PV) modules, a fuel cell, or a rectifier. A simple proportional-integral (PI) regulator is applied to control the dc current flowing through the smoothing inductor, which determines the amplitude of the pulse width modulation (PWM) output-current waveform  $I_{PWM}$  simultaneously. Making the smoothing inductor current follows the reference current is an objective of this current regulator. The switching gate signals of the chopper switch  $Q_C$  is generated by comparing the error signal of the detected inductor current in the steady state and a triangular waveform after passing through the PI regulator.

#### ii. PWM Technique and Inductor Cell Control

In order to achieve a lower distortion of the output-current waveform, a PWM technique is applied. In this paper, a level shifted multicarrier-based sinusoidal PWM technique is employed to generate gate signals for the CSI power switches and to obtain the PWM current waveforms. A schematic control diagram, including the current controller of the chopper and the inductor cell for the H-Bridge CSI, is shown in Fig. 4. The control circuit of the inductor cell functions to control the operation modes, i.e., the charging, the discharging, and the circulating modes, of the inductor cell  $L_c$ . The current flowing through the inductor cell ILC is kept constant. It generates the intermediate-level currents based on the output-current waveform of the H-bridge CSI.



Fig. 4. Control diagram of proposed SPWM Technique.

A PI regulator is applied to zero the error between the detected current flowing through the inductor cell and the reference current to obtain stable and balanced intermediate-level currents. The amplitude of the inductor cell current is half of the dc input current  $I_L$ . The output of the PI regulator is modulated by a triangular carrier to generate the control signal i[0], determining the operation mode of the inductor cell.

During the maximum and zero levels of the output current generation, there is only circulating current mode, no charging and no discharging operation modes in the inductor cell, as listed in Table I.

TABLE - I SWITCH STATES OF FIVE LEVEL CSI									
									Operation Mode of Inductor
<b>Q</b> 1	Q2	Q3	Q4	Qc1	Q <sub>c2</sub>	Q <sub>c3</sub>	Q <sub>c4</sub>	Output	Cell
1	0	1	0	1	1	0	0	+I	Circulating mode
1	0	1	0	0	0	1	1	+I	Circulating mode
1	0	1	0	1	0	1	0	+I/2	Charging of inductor cell
1	0	0	1	0	1	0	1	+I/2	Discharging of inductor cell
1	0	0	1	0	0	1	1	0	Circulating mode
1	0	0	1	1	1	0	0	0	Circulating mode
1	0	0	1	0	0	1	1	-I/2	Charging of inductor cell
0	1	0	1	0	1	0	1	-I/2	Discharging of inductor cell
0	1	0	1	0	0	1	1	-I	Circulating mode
0	1	0	1	1	1	0	0	-I	Circulating mode

TABLE - I SWITCH STATES OF FIVE LEVEL CSI

The frequency of the triangular carrier waveform determines the switching frequency of the inductor cell's power switches, which also regulates the charging and the discharging modes of the inductor cell. The discharging mode means that the inductor cell injects power to the load, and during the charging mode, the main H-bridge inverter injects power to the load.

IADLE – II IESI PAKAMETEKS						
PARAMETERS	RANGE					
Smoothing inductor $(L_i)$ and inductor cell $(L_c)$	1 mH and 5 mH					
Inverter switching frequency	22kHz					
Filter capacitor C <sub>f</sub>	5μF					
Load	R=8 Ω. L=1.2 mH					

TABLE – II TEST PARAMETERS





Fig. 7. PV System output voltage waveform.

Fig. 5 shows the PV system output voltage applied to the H-bridge inverter as a DC supply. Fig. 6 shows a computer simulation result of the proposed five-level current waveform generating CSI, where the five-level current, load current, the current flowing through the filter capacitor, the dc input current, and the inductor cell current waveforms are presented. The inductor cell current has been driven to the balanced condition of 50% of the 8-A dc input current. From equation (2) the value of the current flowing in inductor cell is 4A and the mean value of the current flowing in the H-bridge CSI is 8A all these mathematical value are equal to simulation results as shown in fig. 8. The %THD value is shown in fig. 9 with RL.



Fig. 8. Five-level current, Load current, Filter capacitor current, DC input current, and Inductor cell current.



Fig. 9. RL Load current with FFT analysis.

## V. CONCLUSION

The paper presented design & implementation of five level current waveform generation with a low Total Harmonic Distortion percentage (%THD) in load current RL load. Typically the THD in output current in load is 1.09%. The inductor cells are connected in parallel with the main H- Bridge CSI to generate multilevel output current waveforms without additional external DC power sources. The usage of the logical operations results in reduced transient period. All these results are verified through MATLAB/SIMULINK.

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