

4-Unit Cascade Dual Buck Inverter Using Control Systems

G. Manasa¹, Ch. Santosh Kumar², & Dr. D. Padmavathi³

¹M.Tech Student, Power Electronics,

² Assistant Professor

³ Professor, Head of the department,

^{1,2,3} EEE Department, Sridevi Women's Engineering College/ Jawaharlal Nehru Technological University,
Telangana, India

Abstract: This paper presents different series concept cascading four single units of dual buck inverter based on dual buck topology with phase-shift control using control systems. The dual buck type inverters are still VSI, but with the unique topology and operation, they do not have the shoot-through worries, which lead to greatly enhanced reliability. With phase-shifted PWM fed to different cascade units, zero crossing distortion is eliminated. The phase-shift control increases the equivalent switching frequency by N times that of single-unit inverter, which leads to lower current ripple. A 1 kW, 120 V ac output cascade dual buck inverter system has been built to validate the proposed topology and by comparing the results of single unit dual buck inverter, 2-unit, 3-unit and 4-unit cascade dual buck inverter at 1kW. The THD is reduced for 4-unit cascade inverter when compared with 3-unit cascade inverter. This is proved by using FFT analysis in MATLAB SIMULINK.

Keywords: Cascade unit, dual buck inverter, phase-shift control, shoot-through worries, zero crossing distortion

I. Introduction

In types of multilevel inverters, there are diode clamped multilevel inverter, flying capacitor multilevel inverter, cascaded h-bridge multilevel inverter[1-4]. The main concept of diode clamped multilevel inverter is to use diodes and provides the multiple voltage levels through different phases to the capacitor banks which are in series. The main drawback is maximum output voltage is half of the input dc voltage. The main concept of flying capacitor multilevel inverter is to use capacitors. It is of series connection of capacitor clamped switching cells. The output voltage is half of the input dc voltage. It can control both the active and reactive power flow. But due to the frequency switching losses will take place. In cascaded h-bridge multilevel inverter separate dc sources are required for each of the h bridges. The cascade type inverters are capable of reaching higher output voltage level by using commercially standard lower voltage devices and components. They also feature a modular design concept which makes maintenance less burdensome[1-10]. The cascade inverters are well suited for utility interface of various renewable energy sources, such as photo voltaics, fuel cells, battery energy storage, and electric vehicle drives, where separate dc sources naturally exist[11]-[21]. However, because most current cascade inverters are based on a series connection of several single voltage source inverters (VSI) with two active devices in one leg, they suffer from shoot-through problems, the most dominating failure of VSI. In addition, for the hard-switched cascade inverters operating at higher dc bus voltage, they lose the benefit of using power MOSFETs as the active switching devices for efficiency improvement and fast switching speed when they are available at certain voltage and power level. For example, when the cell dc bus voltage goes up to 300 V to 600 V, high voltage power MOSFETs (600 V to 900 V level, like Cool MOS or MD mesh series) cannot be adopted to work at hard-switched situations like traditional cascade H-bridge inverters because of the reverse recovery issues of the body diode [34]-[38] unless soft-switching techniques are employed [39]-[41].

Based on single-unit dual buck inverters a new series of cascade dual buck inverters has been proposed. Compared to traditional cascade inverters, it has much enhanced system reliability [22-24]. Thank to no shoot-through problems and lower switching loss with the help of using power MOSFETs. Compared to conventional VSI-based cascade inverters, cascade dual buck inverter does not have the dead time related issues which can easily push the duty cycle to the theoretical limit and fully transfer the energy to load through total PWM. In addition, the cascade dual buck inverter can be hard-switched while utilizing the benefits of power MOSFETs at certain power levels.

With phase-shift control, it theoretically eliminates the inherent current zero-crossing distortion of the single-unit dual buck type inverter. Phase-shift control is widely used for cascade inverters because it is easy to implement with digital controllers and it equivalently increases the switching frequency by the number of cascade units, which reduces the output voltage and current ripple [25-27]. For the cascade dual buck inverter, phase shift control is adopted as well. Fortunately, with the help of phase-shift control, cascade dual buck inverter theoretically eliminates the zero crossing distortion from zero to full load conditions. In addition, phase-

shift control and cascade topology can greatly reduce the ripple current or cut down the size of passive components by increasing the equivalent switching frequency.

The paper shows topology of the cascade dual buck half bridge inverter and its operation. This paper takes single-phase cascade dual buck half-bridge inverter as the analytical and design subject to demonstrate the feasibility and advantages of cascade dual buck inverters. The closed-loop control for cascade dual buck inverter has been designed and implemented. A cascade dual buck inverter has been designed and tested to demonstrate the feasibility and advantages of the system by comparing single-unit dual buck inverter, 2-unit, 3-unit and 4-unit cascade dual buck inverters at the same 1 kW, 120 V ac output conditions. It shows how much harmonic distortion is reduced for single unit, 2-unit, 3-unit and 4-unit at 1kW and 300 W load conditions.

II. Operating Principle

The single-unit dual buck inverter has two basic forms, dual buck half-bridge inverter [22], [24] and dual buck full-bridge inverter [23]. The proposed cascade dual buck inverter has two types accordingly: cascade dual buck half-bridge inverter and cascade dual buck full-bridge inverter. This paper will discuss on the analysis, design, and testing of the cascade dual buck half-bridge inverter to demonstrate the feasibility and advantages of cascade dual buck inverters.

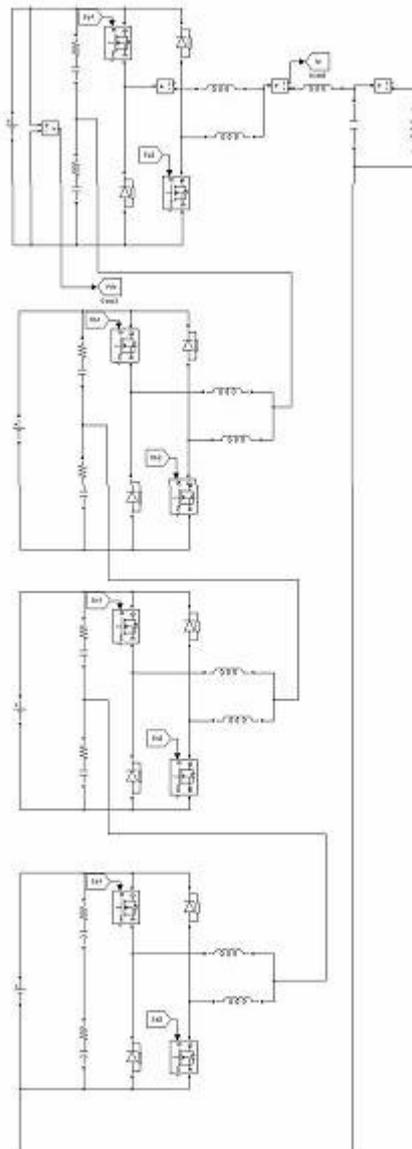


Fig.1. 4-unit cascade dual buck inverter

Fig, 1 shows 4-unit cascade dual buck inverter. It consists of four single units of dual buck half bridge inverter. Each unit is composed of two power MOSFETs and two fast recovery diodes. Each unit has two output ports, i_P and $i_N(i=1,2,\dots,N)$.

In [24], the control strategy for two dual buck half-bridge inverters in series output to obtain higher voltage was proposed. However, the two dual buck inverters shared the same dc power supply, had two sets of filter inductor and capacitor. The proposed inverter in this paper features a different series connection concept, the cascading, which has separate dc power supplies for each cell, and is extended to N unit connection, and shares the same filter components.

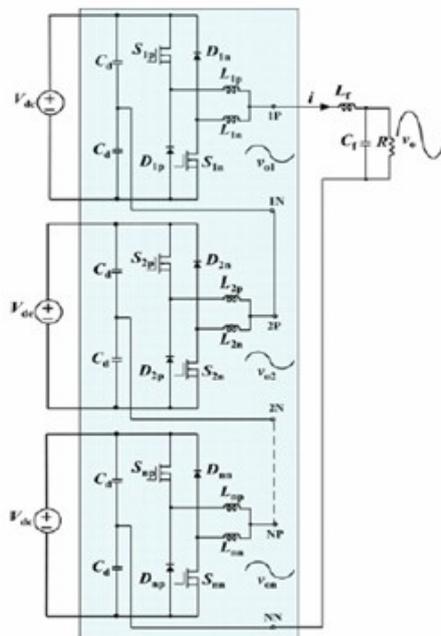


Fig.2. Topology of cascade dual buck half bridge inverter

Fig. 2 shows the topology of the proposed cascade dual buck half-bridge inverter. It consists of N units of single dual buck half-bridge inverter. Each unit is composed of two power MOSFETs and two fast recovery diodes. Each unit has two output ports, iP and iN ($i = 1, 2, \dots, N$). To realize the cascade topology, the iN port of the ith unit is connected with the (i + 1)P port of the (i + 1)th unit, and port 1P and NN are used as the output ports.

S_{1p} and D_{1p} are a working pair, and operate at the positive half-cycle of output current i . S_{1n} and D_{1n} are another working pair, and operate at the negative half-cycle of output current i . The single unit operation modes are shown in Fig 3 [22],[24].

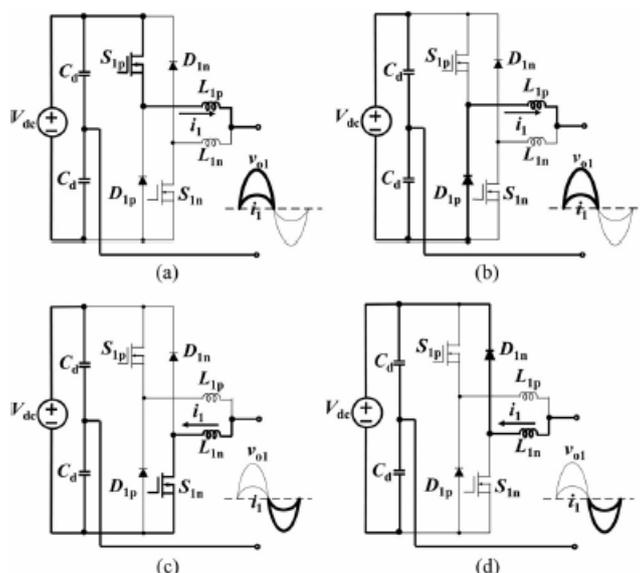


Fig .3. Operation modes of single-unit dual buck half-bridge inverter. (a) Positive current, S_{1p} turned ON. (b) Positive current, D_{1p} free-wheeling. (c) Negative current, S_{1n} turned ON. (d) Negative current, D_{1n} free-wheeling

In single unit operation modes in Fig 3(a) when S_{1p} is turned on we will get positive current and in the second case in Fig 3(b) D_{1p} acts as free wheeling we will get positive current and in the third case in Fig 3 (c) when S_{1n} is turned on we will get negative current and in the fourth case in Fig 3(d) D_{1n} acts as free wheeling and we will get negative current.

For the cascade dual buck inverter, if phase-shift control is not adopted, we can switch all the units exactly the same way as single-unit inverter. This means the PWMs for S_{1p} and S_{1n} are the same. However, this will bring the zero-crossing distortion problem of single-unit dual buck inverters into the cascade topology. In addition, without phase-shift control, the cascade topology loses the benefits of increased equivalent switching frequency and reduced output current ripple.

Therefore, the proposed cascade dual buck inverter utilizes the phase-shift control technique to eliminate the zero-crossing distortion problem of single unit dual buck inverter and at the same time achieve higher equivalent switching frequency thus cutting down output current ripple.

III. Phase-Shift Control Analysis

In single-unit dual buck type inverter based on the direction of output current switch is selected. This operation leads to the drawback current zero crossing distortion. This issue can be reduced by turning on both S_{1p} and S_{1n} near zero-crossing period. However, this remedy is against the operating principle and the best feature of the dual buck type inverter, which is high reliability by avoiding turning on both active switches at the same time. In addition, this passive measure results in higher switching losses because at zero-crossing period two switches are switching while the original goal of dual buck inverter is to have only one switch operating at given time.

With phase-shift control, it theoretically eliminates the inherent current zero-crossing distortion of the single-unit dual buck type inverter. In addition, phase-shift control and cascade topology can greatly reduce the ripple current or cut down the size of passive components by increasing the equivalent switching frequency operating at any given time.

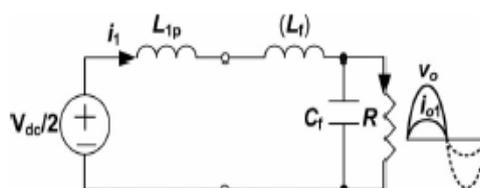


Fig. 4. Equivalent circuit of single-unit half-bridge dual buck inverter when S_{1p} is ON.

In order to illustrate the phase-shift control, single-unit half bridge dual buck inverter and 2-unit cascade half-bridge dual buck inverter are analyzed. Fig. 4 shows the equivalent circuit of single-unit half-bridge dual buck inverter when S_{1p} is ON. Fig. 5 shows the gate signal of S_{1p} and the current through output inductor i_1 . The shaded area of Fig. 5 corresponds to the operation mode shown by Fig. 4.

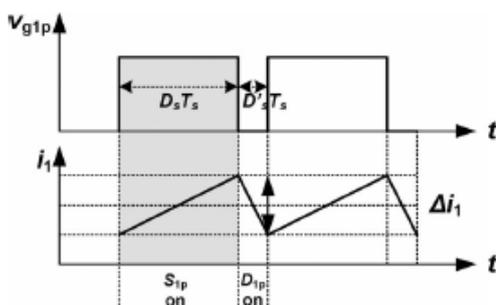


Fig. 5: Gate signal of S_{1p} and current i_1 through output inductor of single-unit half-bridge dual buck inverter.

The current ripple of i_1 can be derived from Fig. 4 and Fig. 5 as follows:

$$\Delta i_1 = \frac{(0.5V_{dc} - v_0) D_s T_s}{L_{1p} + L_f} \quad (1)$$

where D_s is the duty cycle of the switch S_{1p} , $0.5 \leq D_s \leq 1$ (Bipolar SPWM), and $T_s = 1/f_s$ and f_s is the switching frequency of S_{1p} .

At zero-crossing period, D_s is approaching 0.5. Therefore, the current ripple of i_1 at zero-crossing region is not zero. The same analysis applies to the negative half-cycle current. After the two half-cycle current switch switching frequency component are filtered by output capacitor C_f , the current i_{o1} gets its average component. It connects the averages of positive half-cycle current and negative half-cycle current at zero-crossing period. Because both half-cycle current averages at zero crossing are not zero, there is a jump from the negative average to the positive average, which is the current zero-crossing distortion. Since the load is resistive, the output voltage v_o has the same shape as i_{o1} , and thus has the distortion. In light load condition, the resistance is much larger, so the zero-crossing distortion of the output voltage is amplified by the multiplication of the distorted current and the load resistance.

Fig. 6 shows the experimental result of output current i_1 and output voltage v_o across the load at zero-crossing period of single-unit dual buck inverter.



Fig. 6. Experimental result of single-unit half-bridge dual buck inverter at zero crossing period.

Fig. 7 shows the equivalent circuit of 2-unit cascade half bridge dual buck inverter when S_{1p} and S_{2p} are both ON. Fig. 8 shows the gate signals of S_{1p} and S_{2p} , and the current through output inductor i_2 . The shaded area of Fig. 8 corresponds to the operation mode shown by Fig.7. The 2-unit phase-shift angle is 180° (phase-shift angle is $360^\circ/N$). In order to generate the same output voltage v_o , the 2-unit cascade inverter needs two dc sources with $0.5V_{dc}$ each.

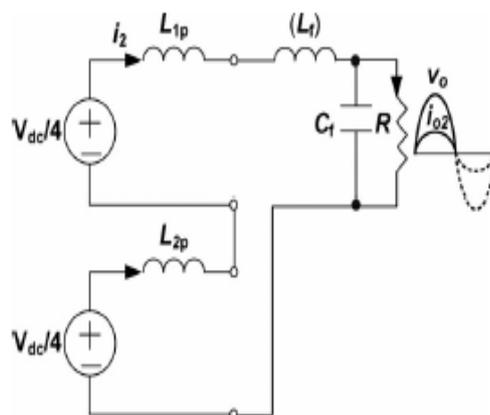


Fig. 7. Equivalent circuit of 2-unit cascade half-bridge dual buck inverter when S_{1p} and S_{2p} are both ON.

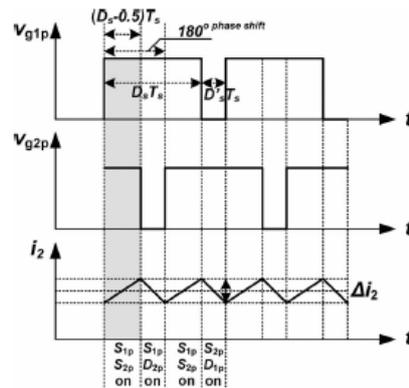


Fig. 8. Gate signals of S_{1p} , S_{2p} , and current i_2 through output inductor of 2-unit cascade half-bridge dual buck inverter.

The current ripple of i_2 can be derived from Figs. 7 and 8 as follows:

$$\Delta i_2 = \frac{(0.25V_{dc} + 0.25V_{dc} - v_0)(D_s - 0.5)T_s}{L_{1p} + L_{2p} + L_f} \tag{2}$$

If $L_{1p} = L_{2p}$, (2) can be rewritten as

$$\Delta i_2 = \frac{(0.5V_{dc} - v_0)(D_s - 0.5)T_s}{2L_{1p} + L_f} \tag{3}$$

In order to find the generalized equation of current ripple with phase-shift control for n-unit cascade half-bridge dual buck inverter, a similar process of derivation has been conducted for a sufficient number of samples, from 3-unit inverter up to 5-unit inverter. The results are shown in Table I and it is under the assumption that $L_{1p} = L_{2p} = L_{np}$.

Table I Current ripple derivation for 3, 4, and 5-unit cascade dual buck inverters

Unit	Current ripple(Δi_j)
3	$\Delta i_3 = \frac{\left(\frac{2}{2.3}V_{dc} - v_0\right)\left(D_s - \frac{1}{3}\right)T_s}{3L_{1p} + L_f}$
4	$\Delta i_4 = \frac{\left(\frac{3}{2.4}V_{dc} - v_0\right)\left(D_s - \frac{2}{4}\right)T_s}{4L_{1p} + L_f}$
5	$\Delta i_5 = \frac{\left(\frac{3}{2.5}V_{dc} - v_0\right)\left(D_s - \frac{2}{5}\right)T_s}{5L_{1p} + L_f}$

From Table I, the generalized form of current ripple for n unit cascade half-bridge dual buck inverter can be derived in the following:

$$\Delta i_n = \frac{\left(\left[\frac{(n+1)}{2}\right]/2n\right)V_{dc} - v_0\left(D_s - \left[\frac{(n-1)}{2}\right]/n\right)T_s}{nL_{np} + L_f} \tag{4}$$

Where $[x]$ is the ceiling function, and is defined as the smallest integer not less than x

$$[x] = \min\{m \in Z | m \geq x\} \tag{5}$$

Where x is a real number, m is an integer, and Z is the set of integers.

As can be seen from (4), at zero-crossing period, D_s is very close to 0.5, and thus the current ripple at zero-crossing region is greatly reduced compared to single-unit inverter. Theoretically, when n is the even number, there is no current distortion at zero-crossing point because $[(n-1)/2]/n$ is equal to 0.5. It is obvious with the increase of the number of cascade units, the current ripple becomes smaller and smaller.

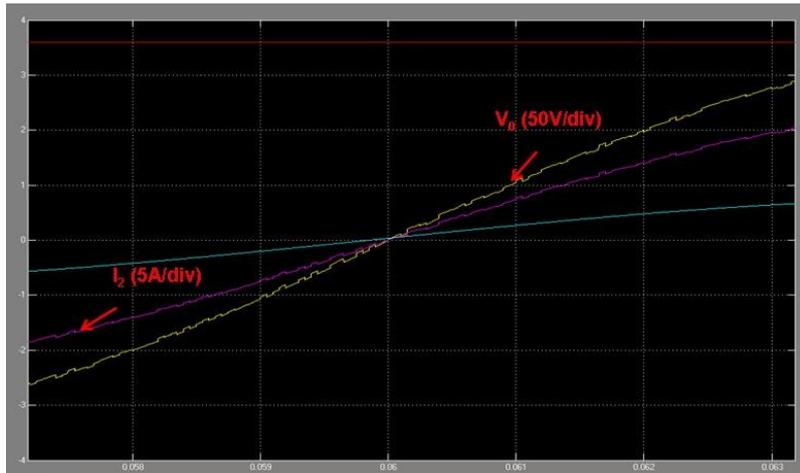


Fig. 9. Experimental result of 2-unit cascade half-bridge dual buck inverter at zero crossing period.

Fig. 9 shows the experimental result of output current i_2 and output voltage v_0 across the load at zero-crossing period of 2-unit dual buck inverter with phase-shift control. The distortion is greatly reduced compared to single unit dual buck inverter.

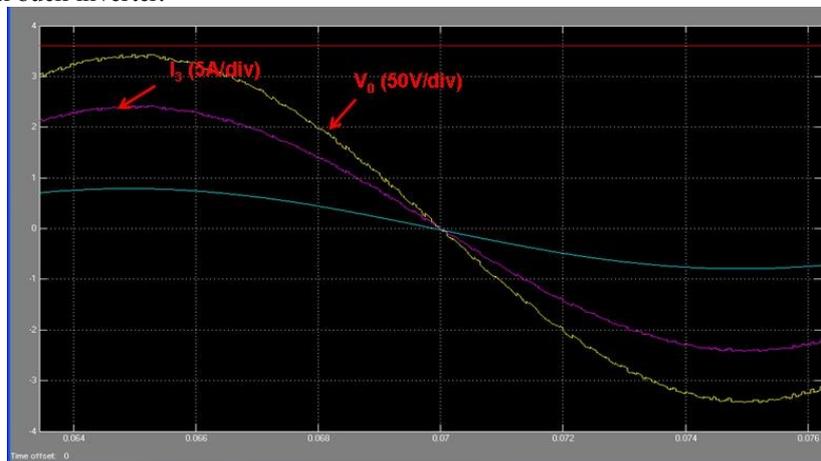


Fig.10 . Experimental result of 3-unit cascade half-bridge dual buck inverter at zero crossing period

Fig 10 shows the experimental result of output current i_3 and output voltage v_0 across the load at zero crossing period of 3- unit dual buck inverter with phase shift control. Compared to 2-unit cascade dual buck inverter the distortion is reduced.

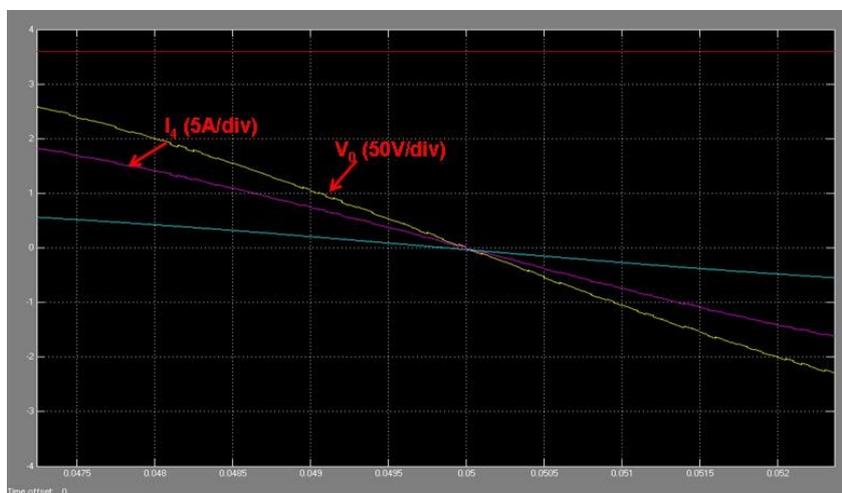


Fig.11. Experimental result of 4-unit cascade half-bridge dual buck inverter at zero crossing period

Fig 11 shows the experimental result of output current i_4 and output voltage v_o across the load at zero crossing period of 4- unit dual buck inverter with phase shift control. Compared to single unit, 2-unit , 3- unit cascade dual buck inverter the distortion is reduced in 4 –unit cascade dual buck inverter.

From Figs. 6 and 9, we can see that the equivalent switching frequency of 2-unit cascade inverter with phase-shift control is doubled, which leads to current ripple cut-down. From (1) and (3), the current ripple ratio is

$$\gamma = \frac{\Delta i_2}{\Delta i_1} = \frac{D_s - 0.5}{D_s} \cdot \frac{L_{1p} + L_f}{2L_{1p} + L_f} \tag{6}$$

Since L_{ip} is already serving as the filter inductor, and if $L_f = 0$, (6) can be analyzed as

$$\gamma = \left(1 - \frac{0.5}{D_s}\right) \cdot 0.5 \leq 25\% \tag{7}$$

We can see that at zero-crossing, the ratio reaches the lowest, zero, and climbs up when D_s increases. Even as D_s approaches 1, the maximum ratio is only 25%.

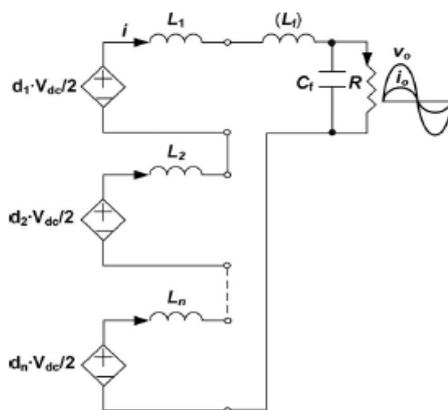


Fig.12. The average model of N-unit cascade half-bridge dual buck inverter.

IV. Control Systems

There are two types of control systems. They are 1) open loop system and 2) closed loop system. Open loop system is used where the calibrated output is already known for a specified input. The systems working on time basis are open loop system. No feedback from output to input.

Closed loop system is that point at which output is measured and given back to feedback. In a feedback control system, information about performance is measured and that information is used to correct how the system performs. In positive feedback closed loop system is used in the design of electronic oscillators. In negative feedback is used for all industrial applications for controlling the temperature, pressure, voltage and power flow.

4.1. Closed-Loop System Control Design

In order to demonstrate the feasibility and advantages of cascade dual buck inverter, the closed-loop control is derived and designed below for a 1 kW, 120 V ac standalone system.

Fig. 12 shows the average model of N-unit cascade half-bridge dual buck inverter. d_j ($j = 1, \dots, n$) is the duty cycle of each corresponding unit and L_j ($j = 1, \dots, n$) is the output inductor of each unit

$$\begin{aligned} L_j &= L_{jp} \quad i > 0 \\ L_j &= L_{jn} \quad i < 0 \end{aligned} \tag{8}$$

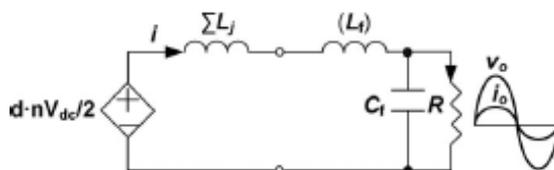


Fig. 13. The equivalent average model of N-unit cascade half-bridge dual buck inverter.

From Fig. 12, we have the following relation

$$(d_1 + d_2 + \dots + d_n) \cdot \frac{V_{dc}}{2} = \frac{d_1 + d_2 + \dots + d_n}{N} \cdot \frac{NV_{dc}}{2} \quad (9)$$

d_j can be different from each other. However, to maintain the power balance of each cascade unit, it is desirable to have equal d_j . So if $d_1 = d_2 = \dots = d_n = d$, (9) can be rewritten as

$$(d_1 + d_2 + \dots + d_n) \cdot \frac{V_{dc}}{2} = d \cdot \frac{NV_{dc}}{2} \quad (10)$$

Define $L = \Sigma L_j + L_f$, and we have the following equation from Fig. 12:

$$d(t) \cdot \frac{NV_{dc}}{2} - v_o(t) = L \frac{di(t)}{dt} \quad (11)$$

Transform (11) to s domain, we have

$$i(s) = \frac{1}{sL} \left(d(s) \cdot \frac{NV_{dc}}{2} - v_o(s) \right) \quad (12)$$

So the transfer functions from duty cycle d to current i and voltage v_o to current i are as follows:

$$G_{id}(s) = \frac{i(s)}{d(s)} = \frac{NV_{dc}/2}{sL} \quad (13)$$

$$G_{iv}(s) = \frac{i(s)}{v_o(s)} = \frac{1}{sL} \quad (14)$$

Where $G_{id}(s)$ is the control-to-output transfer function and $G_{iv}(s)$ is an uncontrolled feed-forward term. By introducing admittance compensation controller $G_{AC}(s)$, shown in Fig. 13, the undesirable term can be cancelled out, which brings in smoother zero-current start-up and reduced current steady-state error [31], [32].

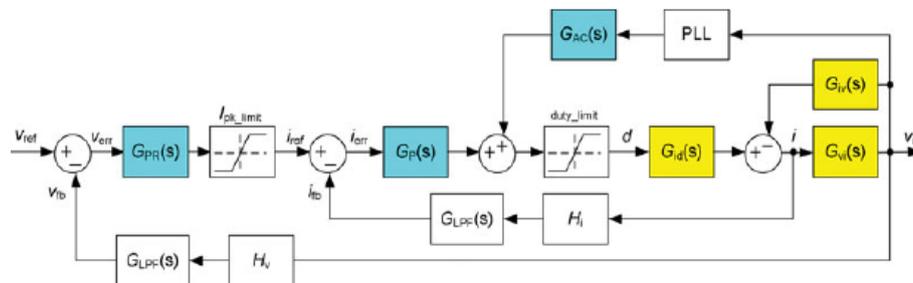


Fig. 14. Control block diagram of N-unit cascade half-bridge dual buck inverter operating at standalone mode.

Fig. 14 shows the control block diagram of N-unit cascade half-bridge dual buck inverter operating at standalone mode. The closed-loop design adopts dual-loop design, the inner current loop with a simple proportional controller $G_P(s)$ to achieve fast dynamic response with enough stability margin and the outer voltage loop with a PR controller $G_{PR}(s)$ to ensure a higher loop gain at fundamental frequency reducing the steady-state voltage error[28]-[30]. For this 1 kW, 120 V ac output cascade inverter system, the controllers are designed as follows.

For the PR controller in (15), k_p is the proportional gain, k_r is the resonant gain, and ω_c is the equivalent bandwidth of the resonant controller. In principle, the bandwidth ω_c needs to be as small as possible to obtain a highly selective bandwidth, but for digital implementation, it is quite difficult to realize a small ω_c . The controller gain at fundamental frequency can be increased by increasing either k_p or k_r .

On the other hand, k_p and k_r cannot be too high because this will impair system stability[29],[30],[42]. With all the considerations above, the parameters for PR controller in this design have been chosen as

$$G_{PR}(s) = k_p + \frac{2\omega_c k_r s}{s^2 + 2\omega_c s + \omega_1^2} \quad (15)$$

Where $k_p = 0.02, k_r = 12, \omega_c = 10$

A current loop in a dual-loop system is designed to have a high loop bandwidth with enough stability margin rather than to reduce the current steady-state error by providing a high gain at fundamental frequency[42]. In this design, a simple proportional controller will meet the requirement

$$G_P(s) = 0.05 \tag{16}$$

In [32], the equivalent dc bus voltage is V_{dc} for single unit inverter system, and thus the outcome of admittance compensation term is the reciprocal of V_{dc} . From Fig. 14, we can clearly see that the equivalent dc bus voltage for the cascade dual-buck inverter is $NV_{dc}/2$. Therefore, the admittance compensation transfer function is obtained as follows:

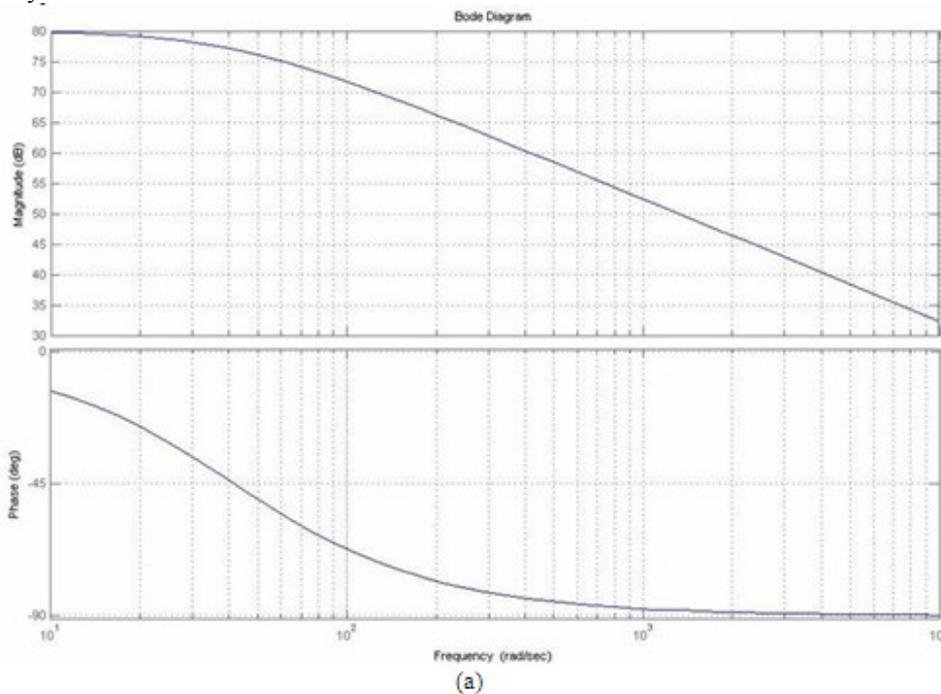
$$G_{AC}(s) = \frac{1}{NV_{dc}/2} \tag{17}$$

In order to close the outer voltage loop, shown in Fig. 14, $G_{vi}(s)$ is derived below based on the model in Fig. 13

$$G_{vi}(s) = \frac{1}{sC_f + 1/R} \tag{18}$$

$G_{LPF}(s)$ is second-order low pass filter with cut-off frequency 5 kHz and a damping ratio 0.7.

With the designed controllers above, the Bode plot of both compensated inner current loop gain and compensated outer voltage loop gain is shown in Fig. 15. As can be seen, the current loop has the cross-over frequency 1.2 kHz with gain margin 15.3 dB and phase margin 70.7° . The voltage loop has the cross-over frequency 209 Hz with phase margin 87.2° , and at 60 Hz fundamental frequency it has a gain of 35.5 dB to reject the steady state error.



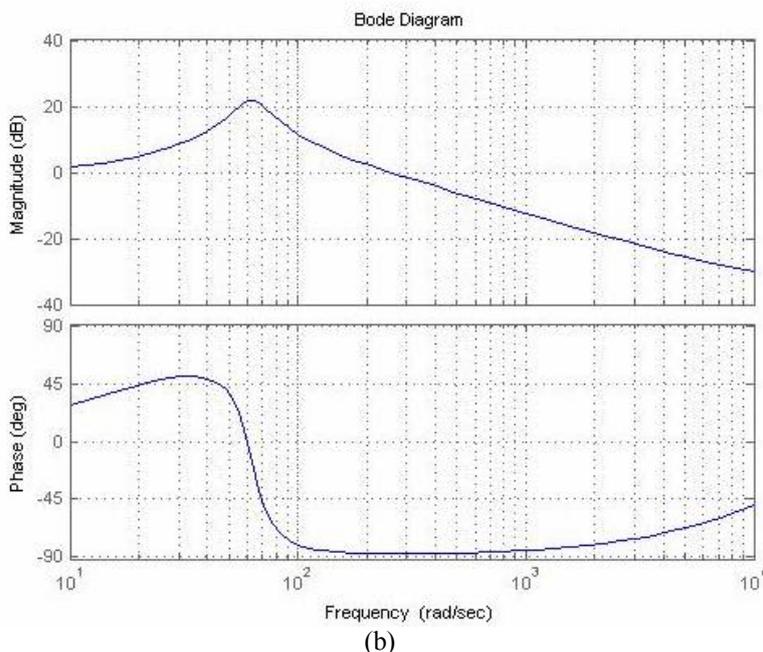


Fig. 15. Bode plot of compensated inner current loop gain and outer voltage loop gain. (a) Bode plot of compensated current loop gain. (b) Bode plot of compensated voltage loop gain.

V. Comparative Simulation Result

To prove the viability and merits of the proposed cascade dual buck inverter with phase-shift control, a 1 kW, 120 V ac output cascade dual buck half-bridge inverter system in standalone operation was designed and tested. The switching frequency of the devices is set to be 20 kHz. The passive components are selected as follows: $L_{jp} = L_{jn} = 250 \mu\text{H}$, $L_r = 1 \text{ mH}$, $C_f = 2.4 \mu\text{F}$, and $C_d = 1.2 \text{ mF}$. The system has the ability of serving as single-unit, 2-unit, 3-unit, 4-unit systems. For comparison, tests were conducted with single-unit, 2-unit, 3-unit, 4-unit systems. All the output power of three tests is 1 kW, and output ac voltage is 120 V RMS. For single-unit system, V_{dc} is 360 V, and for 2-unit cascade system, V_{dc} is 180 V, 3-unit cascade system, V_{dc} is 120 V, 4-unit cascade system, V_{dc} is 120V.

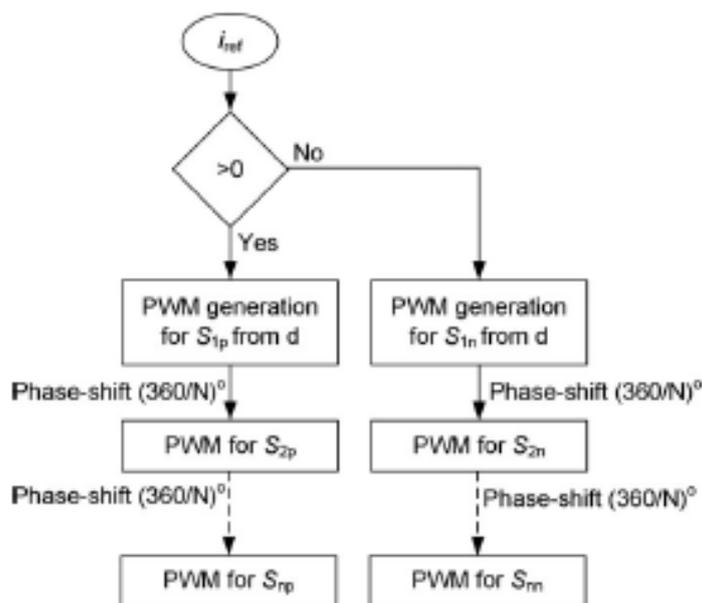
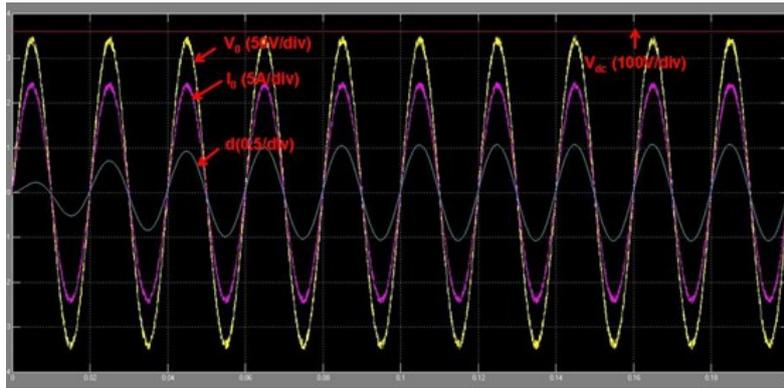
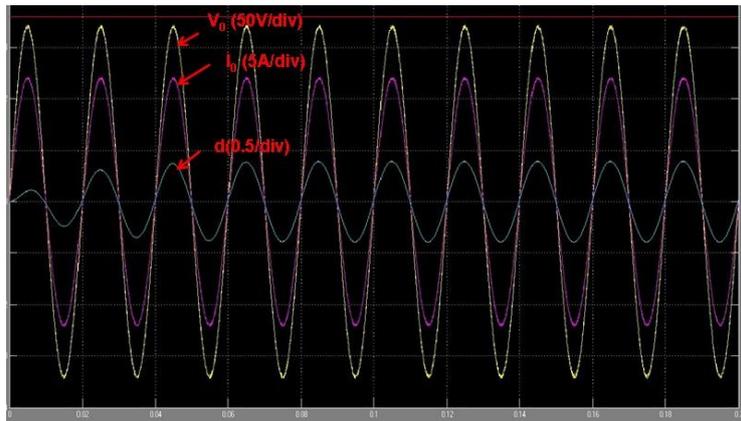


Fig. 16. PWM generation for all switches of N-unit cascade half-bridge dual buck inverter with phase-shift control.

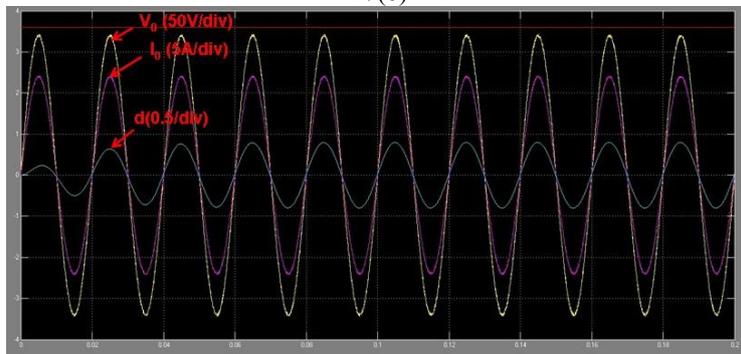
Fig. 16 shows the PWM generation flow chart based on the current reference signal.



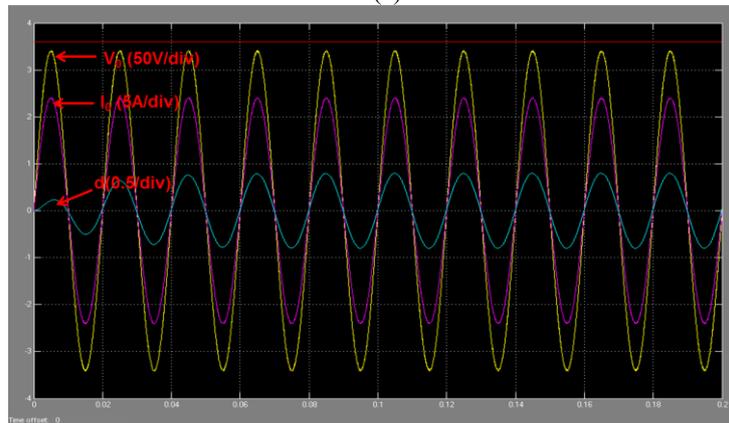
17(a)



17(b)



17(c)



17(d)

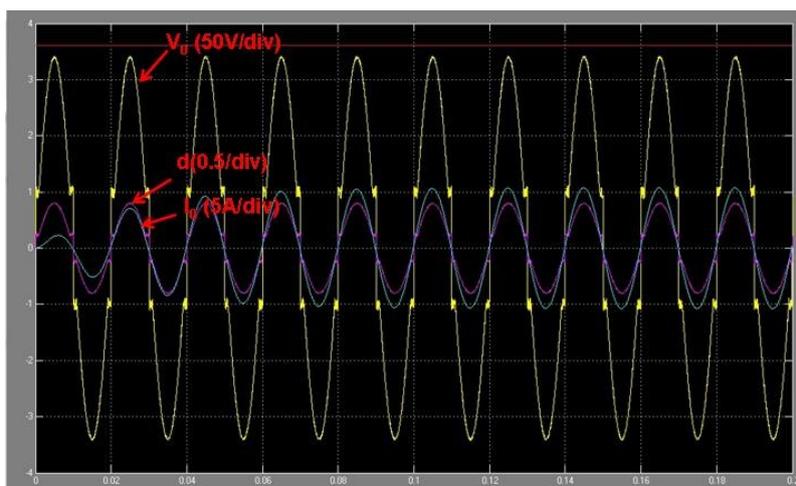
Fig. 17. Output current i_o , ac and dc voltage waveforms for single-unit, 2-unit cascade, 3-unit cascade inverter and 4-unit cascade inverter at 1 kW. (a) Single-unit inverter. (b) 2-unit cascade inverter. (c) 3-unit cascade inverter. (d) 4-unit cascade inverter

Fig. 17 shows the output current i_o through load and voltage waveforms of single-unit dual buck inverter, 2-unit cascade dual buck inverter, 3-unit cascade and 4- unit cascade dual buck inverter at 1kW output. It is clear that with phase-shift control for 2-unit system and 3-unit system, the current zero-crossing distortion was reduced. Compared to 2- unit and 3-unit system the distortion is less in 4-unit cascade dual buck inverter. However, the single-unit zero-crossing is severe. The distortion problem is more obvious in light load conditions for single-unit inverter. Fig. 18 shows the comparison between single-unit inverter, 2-unit cascade inverter and 3- unit cascade inverter at 300 W output. The aggravated current and voltage distortion with very high THD will be intolerable and impose a risk for the load operation. In contrast, the cascade dual buck inverter with phase-shift control does not have this distortion at light load either. The THD is measured for both single-unit inverter and cascade dual buck inverter under full load and light load conditions. As can be seen, the THD at 300 W for single-unit inverter is 10% while for cascade dual buck inverter it is only around 1%.

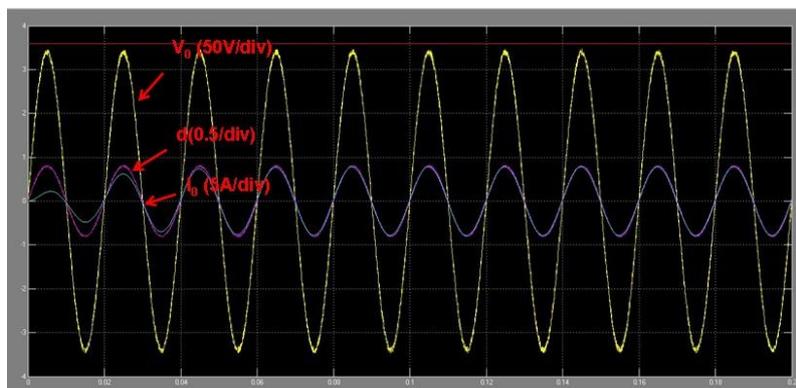
Table II THD measurement for both single-unit and cascade Dual buck inverters

	1kW	
	$V_o(\%)$	$i_o(\%)$
1-unit	2.65	2.69
2-unit	0.91	0.83
3-unit	0.91	0.83
4-unit	0.45	0.41

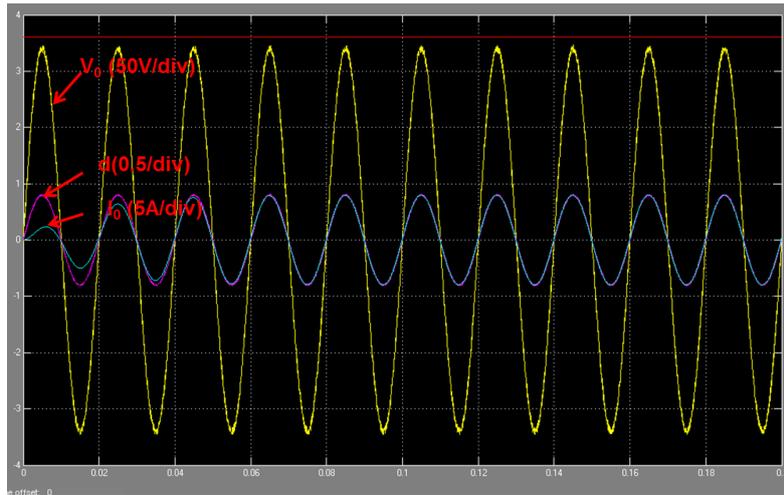
	300W	
	$V_o(\%)$	$i_o(\%)$
1-unit	10.54	10.54
2-unit	1.7	1.5
3-unit	1.52	1.21



18(a)



18(b)



18(c)

Fig.18. Output current i_o , ac and dc voltage waveforms for single-unit, 2-unit, 3-unit cascade inverter system at 300 W. (a) Single-unit inverter. (b) 2-unit cascade inverter. (c) 3- unit Cascade inverter

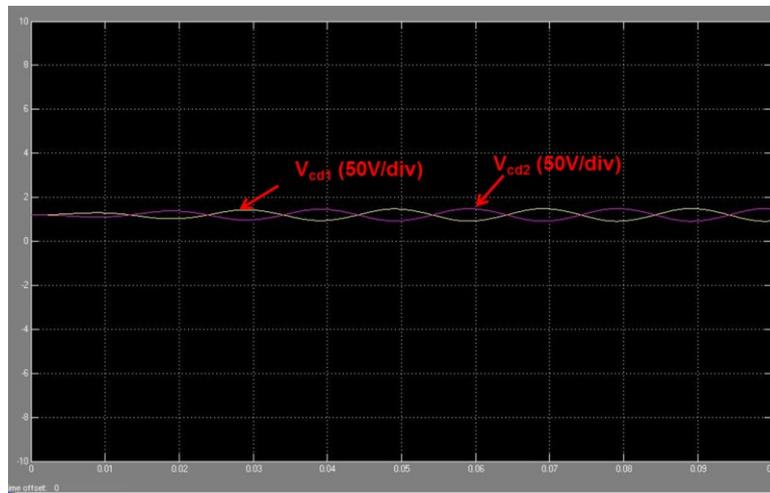
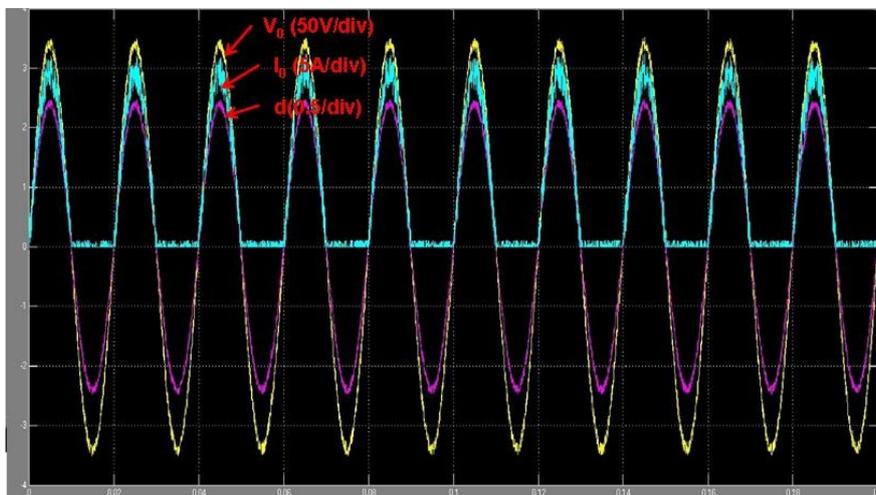
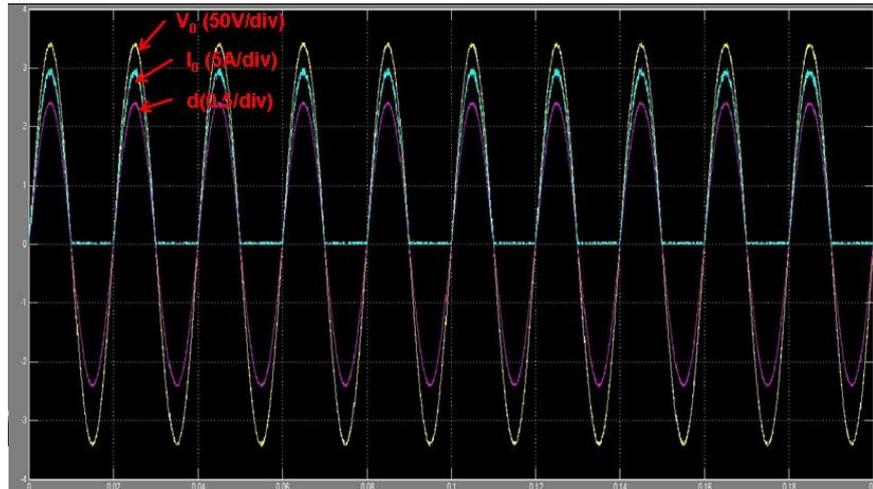


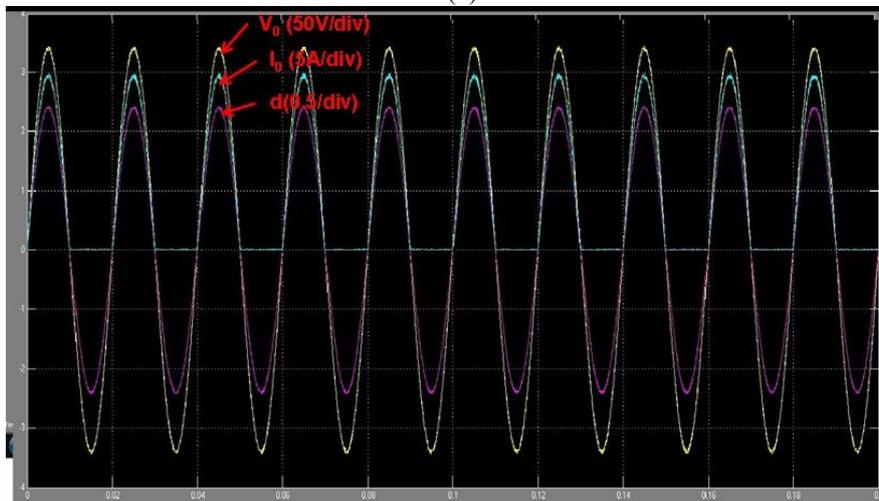
Fig. 19. Voltage waveforms across split capacitors for 3-unit cascade dual buck half-bridge inverter system at 1 kW.



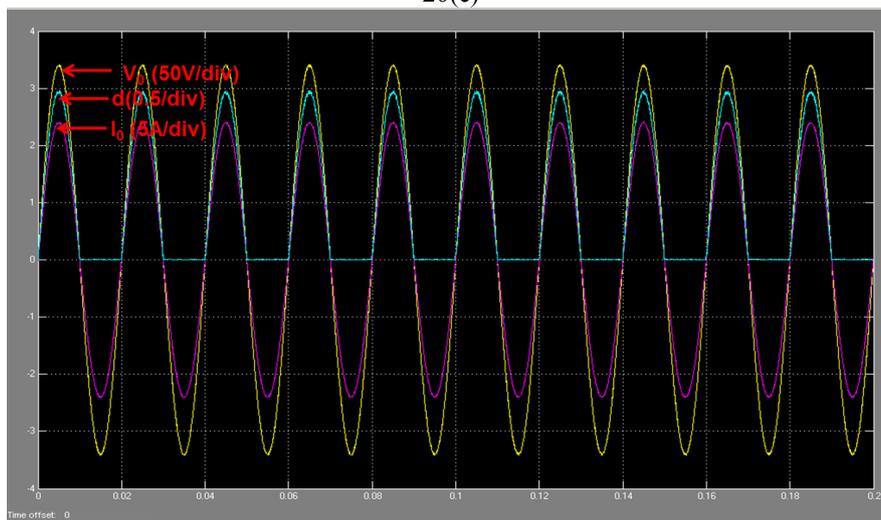
20 (a)



20(b)

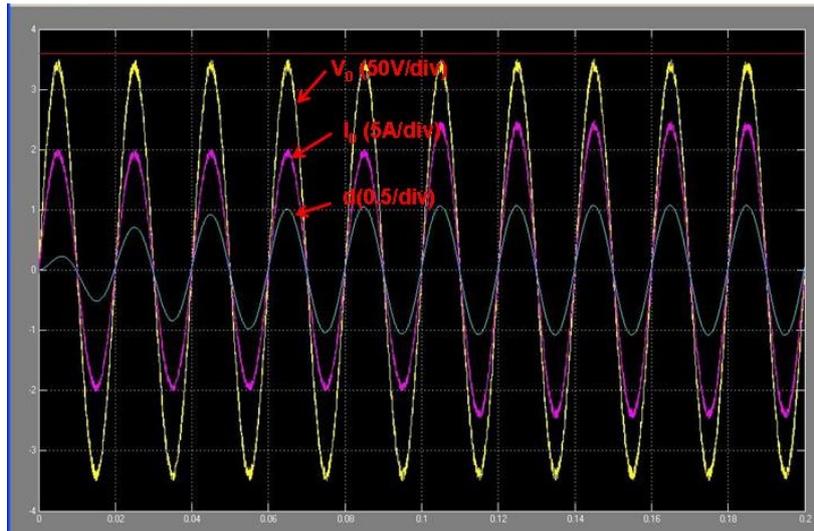


20(c)

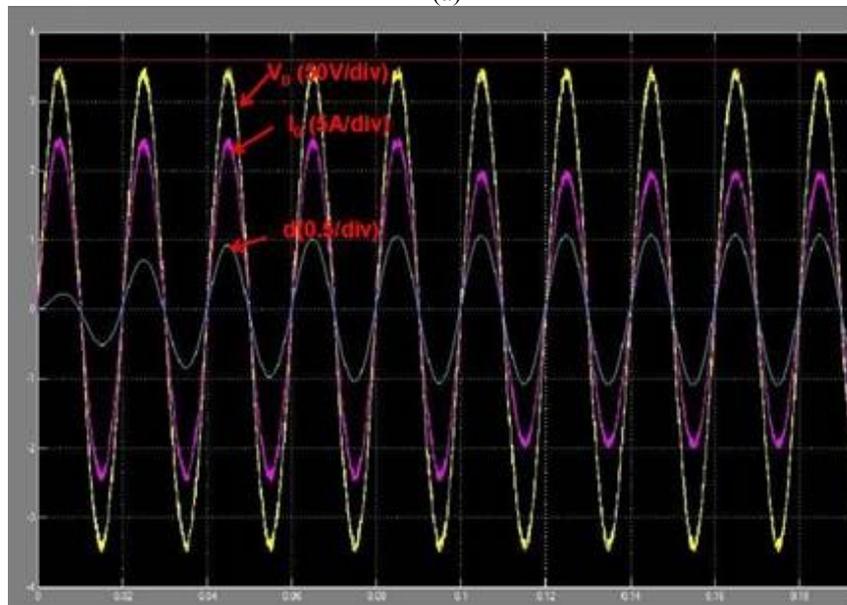


20(d)

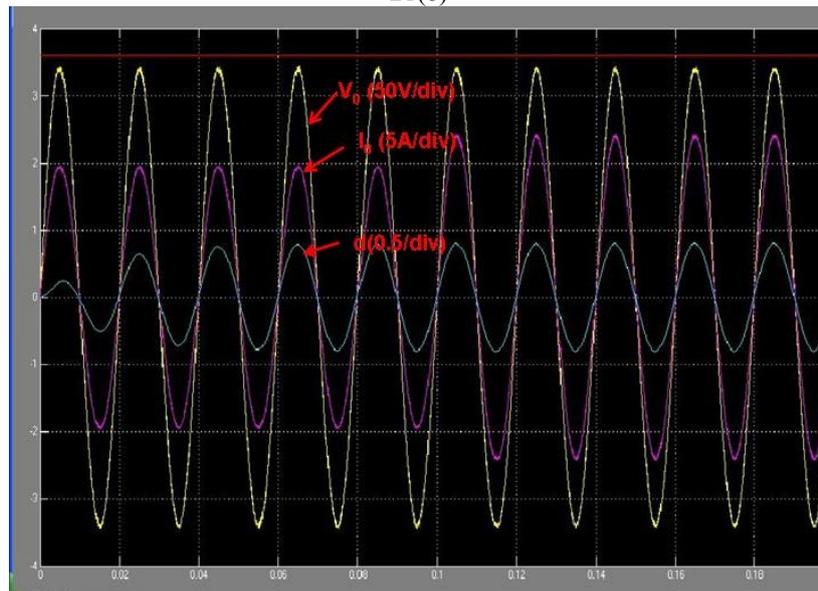
Fig. 20. Output positive half-cycle current i_p , ac and dc voltage waveforms for single-unit, 2-unit cascade, 3-unit and 4-unit cascade inverter system at 1 kW. (a) Single-unit inverter. (b) 2-unit cascade inverter. (c) 3-unit cascade inverter. (d) 4-unit cascade inverter



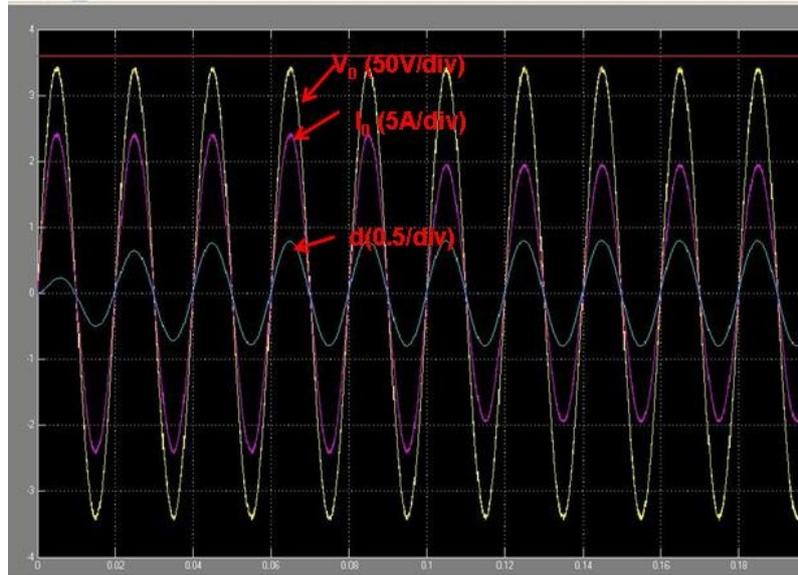
21(a)



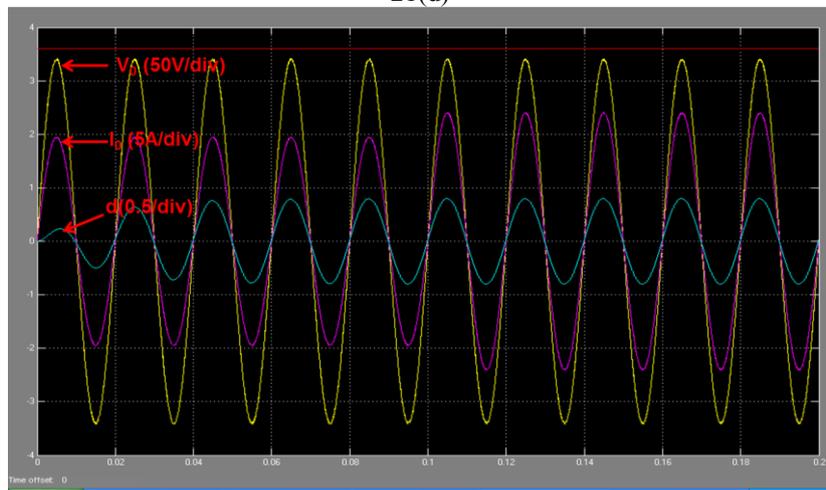
21(b)



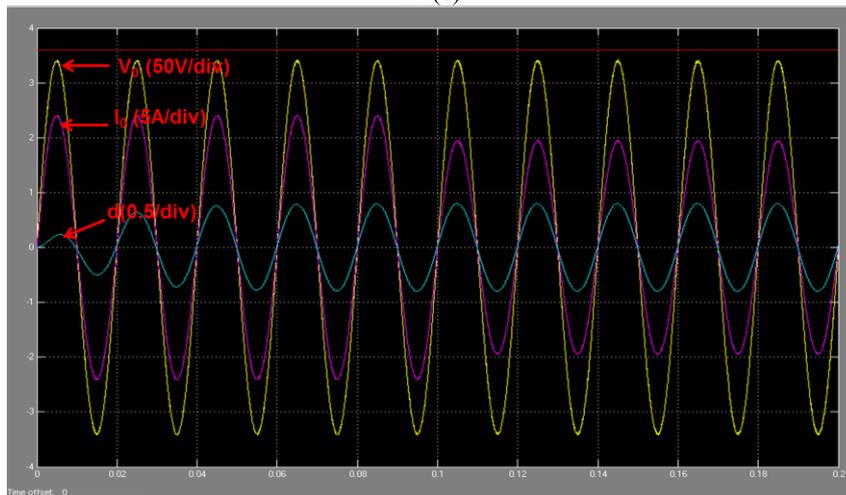
21(c)



21(d)



21(e)



21(f)

Fig. 21. Load step-up and step-down tests for single-unit inverter, 3-unit cascade inverter and 4-unit cascade inverter. (a) Load step-up test for single-unit inverter. (b) Load step-down test for single-unit inverter. (c) Load step-up test for 3-unit cascade inverter. (d) Load step-down test for 3-unit cascade inverter. (e) Load step-up test for 4-unit cascade inverter. (f) Load step-down test for 4-unit cascade inverter

Fig. 19 shows the voltage v_{cd1} and v_{cd2} across the split capacitors from one cell of 3-unit cascade dual buck half-bridge inverter. For the cascade dual buck half-bridge inverter, the split capacitors are needed for each cascade unit. It can be seen that the voltage of the capacitors is naturally balanced. In some cases, if the voltage across the capacitors is unbalanced, due to use of different types of capacitors, different ESR or other factors, a voltage balance compensator might be considered [33] to solve the issue. The cascade dual buck full-bridge inverter is a better alternative to save two split capacitors and totally avoid the issue. Fig. 20 shows the positive half cycle output current i_p through inductor and voltage waveforms of single-unit dual buck inverter, 2-unit cascade dual buck inverter 3-unit and 4-unit cascade dual buck inverter. d_p is the duty cycle for current positive half-cycle. This shows the unique operating feature of single-unit dual buck inverter is inherited by cascade dual buck inverter. Every dual buck unit in the cascade system maintains the no shoot-through characteristic, and thus leads to a more robust and reliable cascade inverter system than traditional voltage source based cascade inverter. Fig. 21 shows the output current and voltage waveforms of single-unit inverter and 3-unit cascade dual buck inverter under load step conditions. Load step-up and step-down tests were done to show the fast dynamics and good stability of the designed control system for cascade dual buck inverter. Even though single-unit system can withstand load change, its inherent zero-crossing distortion will affect the control system and be harmful to the load. Fig 21 (a) shows the step up test for single unit inverter the distortions are more compared with 3- unit cascade inverter 21(b) shows the step down test for single unit inverter. Fig s 21(c),21(d) shows the step-up and step- down tests for three unit cascade inverter. Fig s 21(e), 21(f) shows the step-up and step- down tests for 4- unit cascade inverter. Compared to 3-unit distortion is less in 4-unit.

VI. Conclusion

Based on four single units of dual buck inverter 4-unit cascade dual buck inverter is proposed. The cascade dual buck inverter has all the merits of traditional cascade inverters, and improves on its reliability by eliminating shoot-through worries and dead-time concerns. With the adoption of phase-shift control, the cascade dual buck inverter solves the inherent current zero-crossing distortion problem of single-unit dual buck inverter.

To prove the effectiveness of the proposed topology and control scheme, a cascade dual buck half-bridge inverter system operating at standalone mode with 1 kW, 120 V ac output capability has been designed and tested. Comparing the experimental results of single-unit dual buck inverter, 2-unit,3-unit and 4- unit cascade dual buck inverters at 1 kW the total harmonic distortion is measured and at 300W also the total harmonic distortion is measured.

References

- [1]. J. S. Lai and F. Peng, "Multilevel converters—A new breed of power converter," IEEE Trans. Ind. Electron., vol. 32, no. 3, pp. 509–517, May/Jun. 1996.
- [2]. J. Rodriguez, J. S. Lai, and F. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [3]. M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. P'erez, "A survey on cascaded multilevel inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2196–2206, Jul. 2010.
- [4]. L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," IEEE Ind. Electron. Mag., vol. 2, no. 2, pp. 28–39, Jun. 2008.
- [5]. F. Z. Peng and J. S. Lai, "A multilevel voltage-source inverter with separate dc sources for static VAR generation," in Proc. Conf. Rec. IEEE-IAS Annu. Meeting, Lake Buena Vista, FL, Oct. 8–12, 1995, pp. 2541–2548.
- [6]. F. Z. Peng and J. S. Lai, "Dynamic performance and control of a static VAR compensator using cascade multilevel inverters," in Proc. Conf. Rec. IEEE-IAS Annu. Meeting, San Diego, CA, Oct. 6–10, 1996, pp. 1009–1015.
- [7]. F. Z. Peng, J.W.Mc Keever, and D. J. Adams, "Cascade multilevel inverters for utility applications," in Proc. Conf. Rec. IEEE-IECN Annu. Meeting, New Orleans, LA, Nov. 9–14, 1997, pp. 437–442.
- [8]. M. Hagiwara, K. Nishimura, and H. Akagis, "A medium-voltage motor drive with a modular multilevel PWM inverter," IEEE Trans. Power Electron., vol. 25, no. 7, pp. 1786–1799, Jul. 2010.
- [9]. R. Teodorescu, F. Blaabjerg, J. Pederson, E. Cengelci, and P. Enjeti, "Multilevel inverter by cascading industrial VSI," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 832–838, Aug. 2002.
- [10]. P. Lezana and G. Ortiz, "Extended operation of cascade multi-cell converters under fault condition," IEEE Trans. Ind. Electron., vol. 56, no. 7, pp. 2697–2703, Jul. 2009.
- [11]. H. Ertl, J.W. Kolar, and F. C. Zach, "A novel multi-cell dc-ac converter for applications in renewable energy systems," IEEE Trans. Ind. Electron., vol. 49, no. 5, pp. 1048–1057, Oct. 2002.
- [12]. O. Alonso, P. Sanchis, E. Gubia, and L. Marroyo, "Cascaded H-bridge multilevel converter for grid connected photovoltaic generators with independent maximum power point tracking of each solar array," in Proc. 34th IEEE Power Electron. Spec. Conf., 2003, vol. 2, pp. 731–735.
- [13]. E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a single phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems," IEEE Trans. Ind. Electron., vol. 56, no. 11, pp. 4399–4406, Nov. 2009.
- [14]. F. S. Kang, S. J. Park, S. E. Cho, C. U. Kim, and T. Ise, "Multilevel PWM inverters suitable for the use of stand-alone photovoltaic power grid-connected inverters for photovoltaic modules," IEEE Trans. Energy Convers., vol. 20, no. 4, pp. 906–915, Dec. 2005.
- [15]. L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," IEEE Trans. Ind. Appl., vol. 35, no. 1, pp. 36–44, Jan./Feb. 1999.
- [16]. L. M. Tolbert, F. Z. Peng, T. Cunyngham, and J. N. Chiasson, "Charge balance control schemes for cascade multilevel converter in hybrid electric vehicles," IEEE Trans. Ind. Electron., vol. 49, no. 5, pp. 1058–1064, Oct. 2002.

- [17]. L. Maharjan, T. Yamagishi, H. Akagi, and J. Asakura, "Fault-tolerant operation of a battery-energy-storage system based on a multilevel cascade PWM converter with star configuration," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2386–2396, Sep. 2010.
- [18]. L. Maharjan, S. Inoue, H. Akagi, and J. Asakura, "A transformer less battery energy storage system based on a multilevel cascade PWM converter," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 4798–4804.
- [19]. Q. Song and W. H. Liu, "Control of a cascade STACOM with star configuration under unbalanced conditions," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 45–58, Jan. 2009.
- [20]. L. Maharjan, S. Inoue, H. Akagi, and J. Asakura, "State-of-Charge (SOC)-balancing control of a battery energy storage system based on a cascade PWM converter," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1628–1636, Jun. 2009.
- [21]. J. Liu and Y. Yan, "A novel hysteresis current controlled dual buck half bridge inverter," in *Proc. IEEE PESC*, 2003, pp. 1615–1620.
- [22]. Z. Yao, L. Xiao, and Y. Yan, "Dual-buck full-bridge inverter with hysteresis current control," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3153–3160, Aug. 2009.
- [23]. Z. Yao, L. Xiao, and Y. Yan, "Control strategy for series and parallel output dual-buck half bridge inverters based on DSP control," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 434–444, Feb. 2009.
- [24]. R. Gupta, A. Ghosh, and A. Joshi, "Switching characterization of cascaded multilevel-inverter-controlled systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1047–1058, Mar. 2008.
- [25]. Y.-M. Park, H.-S. Yoo, H.-W. Lee, M.-G. Jung, S.-H. Lee, C.-D. Lee, S.-B. Lee, and J.-Y. Yoo, "A simple and reliable PWM synchronization and phase-shift method for cascaded H-bridge multilevel inverters based on a standard serial communication protocol," in *Proc. Conf. Rec. 41st IEEE IAS Annu. Meeting*, Oct. 2006, vol. 2, pp. 988–994.
- [26]. B. N. Mwinyiwiwa, Z. Wolanski, and B. T. Ooi, "Microprocessor implemented SPWM for multiconverters with phase-shifted triangle carriers," in *Proc. Conf. Rec. IEEE-IAS Annu. Meeting*, New Orleans, LA, Oct. 1997, pp. 1542–1549.
- [27]. F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1398–1409, Oct. 2006.
- [28]. R. Teodorescu and F. Blaabjerg, "Proportional-resonant controllers. A new breed of controllers suitable for grid-connected voltage-source converters," in *Proc. Int. Conf. Optim. Electr. Electron. Equip. (OPTIM)*, 2004, vol. 3, pp. 9–14.
- [29]. C.-L. Chen, Y. Wang, J.-S. Lai, Y.-S. Lee, and D. Martin, "Design of parallel inverters for smooth mode transfer microgrid applications," *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 6–15, Jan. 2010.
- [30]. K. P. Louganski and J.-S. Lai, "Current phase lead compensation in single phase PFC boost converters with a reduced switching frequency to line frequency ratio," *IEEE Trans. Power Electron.*, vol. 22, pp. 113–119, Jan. 2007.
- [31]. S.-Y. Park, C.-L. Chen, J.-S. Lai, and S.-R. Moon, "Admittance compensation in current loop control for a grid-tie LCL fuel cell inverter," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1716–1723, Jul. 2008.
- [32]. H. Qian, J. H. Zhang, J.-S. Lai, and W. S. Yu, "A high-efficiency grid-tie battery energy storage system," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 886–896, May. 2011.
- [33]. S.-Y. Park, P. W. Sun, W. Yu, and J.-S. Lai, "Performance evaluation of high voltage super junction MOSFETs for zero-voltage soft-switching inverter applications," in *Proc. 25th IEEE Appl. Power Electron. Conf. Expo.*, 2010, pp. 387–391.
- [34]. L. Saro, K. Dierberger, and R. Redl, "High-voltage MOSFET behavior in soft-switching converters: Analysis and reliability improvements," in *Proc. 20th IEEE Telecom. Energy Conf.*, 1998, pp. 30–40.
- [35]. X. D. Huang, H. J. Yu, J.-S. Lai, A. R. Hefner, and D. W. Berning, "Characterization of paralleled super junction MOSFET devices under hard and soft-switching conditions," in *Proc. 32nd IEEE Power Electron. Spec. Conf.*, 2001, vol. 4, pp. 2145–2150.
- [36]. C. M. Johnson and V. Pickert, "Three-phase soft-switching voltage source converters for motor drives. II. Fundamental limitations and critical assessment," *IEE Proc. Electr. Power Appl.*, vol. 146, no. 12, pp. 55–162, 1999.
- [37]. V. Pickert and C. M. Johnson, "Three-phase soft-switching voltage source converters for motor drives. I. Overview and analysis," *IEE Proc. Electr. Power Appl.*, vol. 146, no. 2, pp. 147–154, 1999.
- [38]. P. W. Sun, J.-S. Lai, H. Qian, W. S. Yu, C. Smith, and J. Bates, "High efficiency three-phase soft-switching inverter for electric vehicle drives," in *Proc. IEEE Veh. Power Propuls. Conf.*, 2009, pp. 761–766.
- [39]. J. H. Zhang and J.-S. Lai, "A synchronous rectification featured soft switching inverter using CoolMOS," in *Proc. 21st IEEE Appl. Power Electron. Conf. Expo.*, 2006, pp. 810–815.
- [40]. J.-S. Lai, J. H. Zhang, H. J. Yu, and H. Kouns, "Source and load adaptive design for a high-power soft-switching inverter," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1667–1675, Nov. 2006.
- [41]. C.-L. Chen, J.-S. Lai, Y. Wang, S.-Y. Park, and H. Miwa, "Design and control for for LCL-based inverters with both grid-tie and standalone parallel operations," in *Proc. Conf. Rec. IEEE-IAS Annu. Meeting*, Oct. 2008, pp. 1–7.