

Fpga Controlled Cascaded Mli With Advanced Multilevel Strategies For Harmonic Reduction

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Abstract: This paper focused on the implementation of Cascaded H-bridge multilevel inverter fed induction motor by using the modulating technique of OVPWM with U-type carrier to the Five-level inverter. The PWM switching signals based on offset voltage injected in sine reference with U-type carrier been generated. The multilevel inverter fed induction motor drive with SPWM and proposed strategies are performed and results are analyzed. Xilinx FPGA is a programmable logic device developed by Xilinx, which is considered as an efficient hardware for rapid prototyping. In addition to Xilinx FPGA, MATLAB/Simulink software was used for simulation and verification of the proposed circuit before implementation. Hardware is implemented for a single phase cascaded five level inverter with the proposed modulating technique by using FPGA, which drives a single phase induction motor of 0.5 H.P Simulation results and hardware results are compared. It is justified that the proposed modulation technique can be recommended to three phase five level Cascaded H-bridge inverter fed three phase induction motor for better performance with reduced harmonics at output.

Index Terms- Multilevel concept, Cascade Multilevel inverter, FPGA, Multi level carrier signals, Pulse width modulation, Total Harmonic Distortion.

I. INTRODUCTION

Modulation in multilevel inverters has recently been widely investigated, but the overvoltage caused by multilevel modulation has not been discussed thoroughly. Several modulation methods, such as space vector pulse width modulation (SVPWM), space vector control (SVC), duty cycle modulation (DCM) and several sine-triangle comparison modulation variations have been presented, for example, in the literature given by Wei.S et.al.[19] and Naumanen et.al.[24]. All the modulation methods, except for the SVC, are based on pulse width modulation.. The output voltage waveform of the SVC resembles staircase that approximates the shape of the reference wave. An example of a multilevel inverter using SVC is presented by Kouro.S et.al. [22]. Power electronic switches, especially IGBTs have become faster in terms of turn-on and turn-off times, which has led to the high dv/dt of the edges of the PWM voltage. The short rise time compared with the propagation delay causes an oscillating overvoltage at the motor terminals. The propagation delay is caused by the length and insulation of the cable, and with the impedance a mismatch between the cable and the motor an overvoltage occurs. As dv/dt becomes higher, an overvoltage will occur at even shorter cable lengths. This phenomenon has been thoroughly reported by Persson et.al.[6] and Skibinski[9].

The classification of PWM techniques or modulating techniques can be classified as shown in Fig.1.

Wang et.al [15] in his investigation on sine triangle modulation technique stated that SPWM is the most commonly used modulating technique suffers from certain drawbacks like low fundamental output voltage. The Modified Reference Modulation techniques that offer improved performances as discussed by M.H.Rashid [20] and are as Trapezoidal ,Stair case ,Stepped , Harmonic injected, Space Vector PWM (SVPWM) and Offset voltage injected in reference(OVPWM) The above PWM techniques are applicable to three-phase inverters. However the last three techniques are commonly used for three-phase inverters.

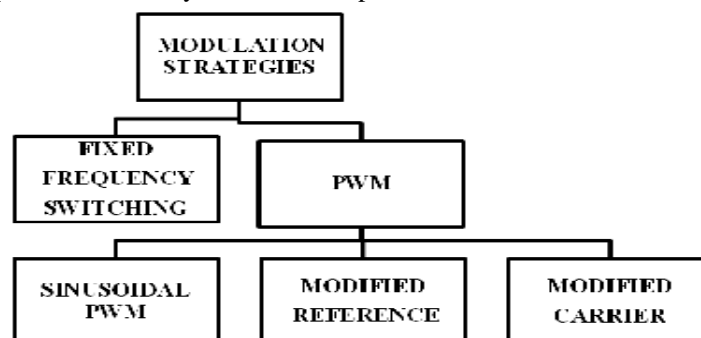


Fig.1 Classification of Modulation strategies

Because of its flexibility of manipulation SVM has increasing applications in power converters and motor control. In the SPWM scheme for two-level inverters, each reference phase voltage is compared with the triangular carrier and the individual pole voltages are generated, independent of each other as mentioned by Holtz.J [2]. As per the literature given by Holmes [3], Kim. J et.al.[7], Carrara et.al.[4] and Baiju et.al.[18], to obtain the maximum possible peak amplitude of the fundamental phase voltage, in linear modulation, a common mode voltage, $V_{offset1}$, is added to the reference phase voltages, where the magnitude of $V_{offset1}$ is given by

$$V_{offset} = \frac{-(V_{max} + V_{min})}{2} \quad (1)$$

In Equ. (1), V_{max} is the maximum magnitude of the three sampled reference phase voltages, while V_{min} is the minimum magnitude of the three sampled reference phase voltages, in a sampling interval. The addition of the common mode voltage, $V_{offset1}$, results in the active inverter switching vectors being centered in a sampling interval, making the SPWM technique equivalent to the SVPWM technique as mentioned in Vander Broeck et.al. [1]. Equation (1) is based on the fact that, in a sampling interval, the reference phase which has lowest magnitude (termed the min-phase) crosses the triangular carrier first, and causes the first transition in the inverter switching state. In a multilevel PWM scheme during a sampling period T_s . R. S. Kanchan et.al.[21], has developed a SVPWM technique presents a simple way to determine the time instants at which the three reference phases cross the triangular carriers. These time instants are sorted to find the offset voltage to be added to the reference phase voltages for SVPWM generation for multilevel inverters for the entire linear modulation range, so that the middle inverter switching vectors are centered (during a sampling interval), as in the case of the conventional two-level SPWM scheme.

In multilevel case, PWM techniques with three different disposed triangular or U-type carriers were proposed as follows:

1. Alternate phase disposition (APOD) – every carrier waveform is in out of phase with its neighbor carrier by 180° .
2. Phase opposition disposition (POD) – All carrier waveforms above zero reference are in phase and are 180° out of phase with those below zero.
3. Phase disposition (PD) - All carrier waveforms are in phase.

As per the modulation methods developed by N.Celanovic et.al [11] and J.Rodriguez et.al.[17] used in multilevel inverters can be classified as shown in fig.1.3 according to switching methods. A very popular method in industrial applications is the classic carrier-based sinusoidal PWM developed by L.Tolbert et.al.[12] and Y.Liang et.al [13], that uses the phase-shifting technique to reduce the harmonics in the load voltage. Another interesting alternative is the SVM strategy, which has been used in three-level inverters as mentioned by V.G.Agelidis et.al [10]. B.N.Mwinyiwiwa et.al.[8], discussed that, several multicarrier techniques have been developed to reduce the distortion in multilevel inverters, based on the classical SPWM with triangular carriers. M.Marchesoni [5], has said that, the studies to improve switch utilization for cascaded inverter have been performed in various methods. Marchesoni presented a PWM method using two clock pointers in single phase three-level cascaded inverter. The method has the feature that all the switch components operate at the same switching frequency with very similar duty cycles in both high and low modulation index. Peng et.al [14] and [16] contributed several papers related to cascaded inverter applied to utility and motor applications. In the methods, the switches are turned on and off once per modulation cycle considering reactive power compensation and switching utilization in three-phase eleven-level cascaded inverter. The method used stair pulses to synthesize eleven-voltage level. Recently, Tolbert et.al [16] has proposed a PWM method at low modulation indices applied to both diode-clamped inverters and cascaded inverters for motor drive application. The method used the redundant output voltage states and level rotation during each cycle to increase device utilization. But these methods have the demerits that the switch utilization is improved only at low modulation indices or it is difficult to be implemented in N-level.

During the survey of modulation techniques for the Multi Level Inverters, various modulation techniques for the cascaded MLIs and the competitive factors that need to be satisfied while feeding to a drive have been thoroughly gone through. Based on the above discussion a Cascaded Multi Level Inverter fed Induction Motor with the implementation of the best in Modified Reference and the best in Modified Carrier is preferable for the quality performance at the output.

Field-Programmable Gate Arrays have become fundamental components in implementing high performance digital signal processing systems, digital input/output (I/O) and different types of communications. FPGAs usually include several on-chip PWM controllers thus making generation of control signals for multilevel inverters an easy task. Chinnaiyan et.al.[25], Lopez O et.al.[23] and Lima EF et.al. have discussed that, cascaded H-bridge based three-phase inverters require a large number of PWM signals and so the FPGA appears as the right choice to implement this stage of the global control system. Consequently, multi-carrier PWM generation and also the control strategies for the chosen inverter were designed using the system generator software of Xilinx.

II. CASCADED MULTILEVEL INVERTER

Principle of operation of Cascaded 5LI:

To produce a staircase output voltage, let us consider only one phase of the five level inverter as shown in the

Fig 2(a). Figure 2 (b) provides a five level output across ‘a’ and ‘0’ i.e., $V_{a0}=0, \frac{V_{dc}}{4}, \frac{2V_{dc}}{4}, -\frac{2V_{dc}}{4}, -\frac{V_{dc}}{4}$. Table. 1 shows the relationship between the allowed switches configurations and the output of a 5-level cascaded inverter.

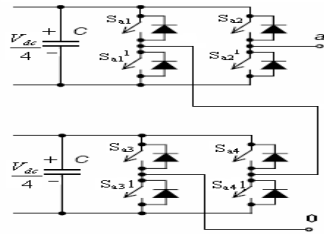


Fig.2 (a) Single phase CC5LI

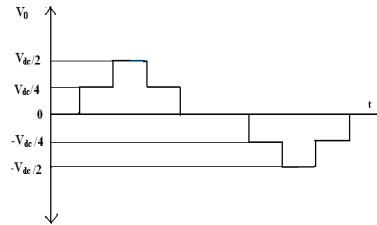


Fig 2 (b) Output waveform

In the case of Five level cascaded the AC output voltage at each level can be obtained in the same manner. The AC terminal voltages of different level inverters are connected in series. By different combinations

of the four switches, S_{a1}, S_{a1}^1, S_{b1} and S_{b1}^1 , each inverter level can generate three different voltage outputs, $+\frac{V_{dc}}{4}, -\frac{V_{dc}}{4}$, and ‘0’ as shown in fig2(b). The AC output of each H-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs.. In this topology, the number of output phase voltage levels is defined by $m = 2s+1$, where ‘s’ is the number of DC sources.

Table.1 Switching states for Cascaded 5LI

Output V_{a0}	Switch States							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S'_{a1}	S'_{a2}	S'_{a3}	S'_{a4}
0	1	1	0	0	0	0	1	1
$\frac{V_{dc}}{4}$	1	0	0	0	0	1	1	1
$\frac{2V_{dc}}{4}$	1	0	1	0	0	1	0	1
$-\frac{V_{dc}}{4}$	0	1	1	1	1	0	0	0
$-\frac{2V_{dc}}{4}$	0	1	0	1	1	0	1	0

Cascaded 3-level and 5-level multilevel inverters are simulated, with the usage of IGBTs as switching devices, which will be closer to the real time implementations. The IGBTs have used constant pulses from repetitive sequence block in Simulink.

Fig 3 (a) and (b) shows the FFT Analysis for the output voltage of 3-level and 5-level Cascaded H-Bridge MLIs and proved that THD is 56.00% and 25.79% with Fundamental magnitudes of 189.2 V and 201.5 V.

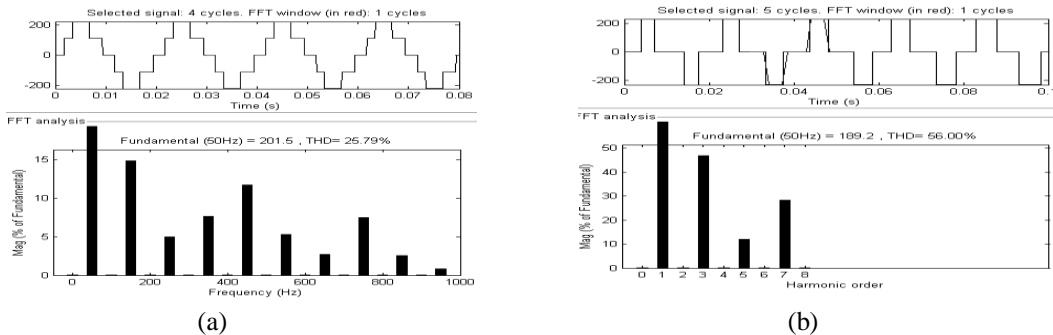


Fig.3 Power GUI FFT Analysis of 3-level and 5-level of CCMLI

Modulating techniques can be divided into two categories based on the reference signal and carrier signal. The conventional Sine wave reference is altered as trapezoidal wave, stepped wave, stair case wave,

harmonic injected in reference sine wave, space vector wave and offset voltage injected in reference called as Trapezoidal PWM, Stepped PWM, Stair case PWM, Harmonic injected PWM, Space Vector PWM (SVPWM) and Offset voltage injected in reference PWM(OVPWM) respectively. The conventional triangular Carrier wave and proposed U-type carrier wave undergone for various shifting methods such as phase disposition (PD), Phase opposition with Disposition (POD), alternatively in opposition disposition(APOD).

III. Offset Voltage Injected In Reference OVPWM (Or) Modified SVPWM With Triangle And U-Type Carrier

The SVPWM for multilevel inverters involves mapping of the outer sectors to an inner sub hexagon sector, to determine the switching time duration, for various inverter vectors. Then the switching inverter vectors corresponding to the actual sector are switched, for the time durations calculated from the mapped inner sectors. It is obvious that such a scheme, in multilevel inverters, will be very complex, as a large number of sectors and inverter vectors are involved. This will also considerably increase the computation time.

A modulation scheme proposed in this work, where a fixed common mode voltage, is added to the reference phase voltage throughout the modulation range. It has been shown that this common mode addition will not result in a SVPWM-like performance, as it will not centre the middle inverter vectors in a sampling interval. The common mode voltage to be added in the reference phase voltages, to achieve SVPWM-like performance, is a function of the modulation index for multilevel inverters. A SVPWM scheme is based on the above principle has been presented, where the switching time for the inverter legs is directly determined from sampled phase voltage amplitudes. This technique reduces the computation time considerably more than the conventional SVPWM techniques do, but it involves region identifications based on modulation indices. While this SVPWM scheme works well for a three-level PWM generation, it cannot be extended to multilevel inverters of levels higher than three, as the region identification becomes more complicated. A carrier-based PWM scheme has been presented, where sinusoidal references are added with a proper offset voltage before being compared with carriers, to achieve the performance of a SVPWM.

The offset voltage computation is based on a modulus function depending on the DC link voltage, number of levels and the phase voltage amplitudes. The PWM switching times for the inverter legs are directly derived from the sampled amplitudes of the reference phase voltages. The SVPWM switching pattern generation is not realized with offset voltage computation from a modulus function. A simple way of adding a time offset to the inverter-gating signal, to generate the SVPWM pattern, from only the sampled amplitudes of the reference phase voltages. The proposed PWM signal generation does not involve checks for region identification, as in the SVPWM scheme.

For this analysis we have developed two types of carrier based techniques:

- OVPWM reference with triangular carriers
- OVPWM reference with U-type carriers

The above said two modulating strategies are under gone for triangular PD, POD and APOD with OVPWM reference and U-type carriers PD, POD and APOD with OVPWM reference. The results are tabulated

Phase Disposition

In this method carriers are the same in frequency, amplitude and phases, but they are just different in DC offset to occupy contiguous bands as shown in Fig 4. The carriers are in phase across all the bands. For this technique, significant harmonic energy is concentrated at the carrier frequency, but since it is co-phasal component, it does not appear in the line-to-line voltage.

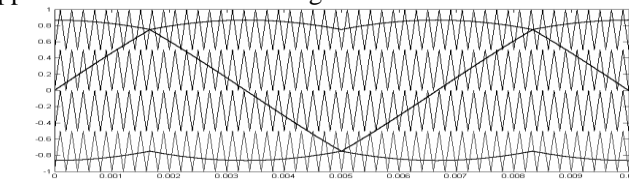


Fig. 4 Generation of PD gate pulses with triangular carriers

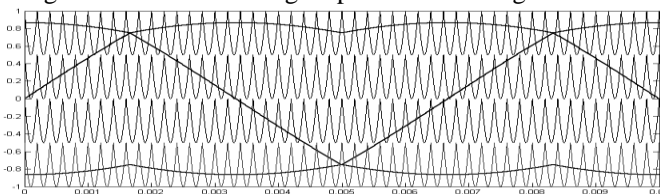


Fig. 5 Generation of gate pulses with U-type carriers

Fig. 4 shows the generation of PD gate pulses with triangular carriers of cascaded five-level inverter. In this OVPWM reference signal compared with four level shifted triangular carriers. Fig. 5 shows the generation of gate pulses with U-type carrier.

Fig. 6 is the line-line output voltage and harmonic spectrum of cascaded five-level inverter with modulating technique represented in Fig 4. For this the triangular carriers are used. The harmonic spectrum of cascaded five-level inverter shows that the total harmonic distortion is 4.68% with fundamental voltage of 339.3V.

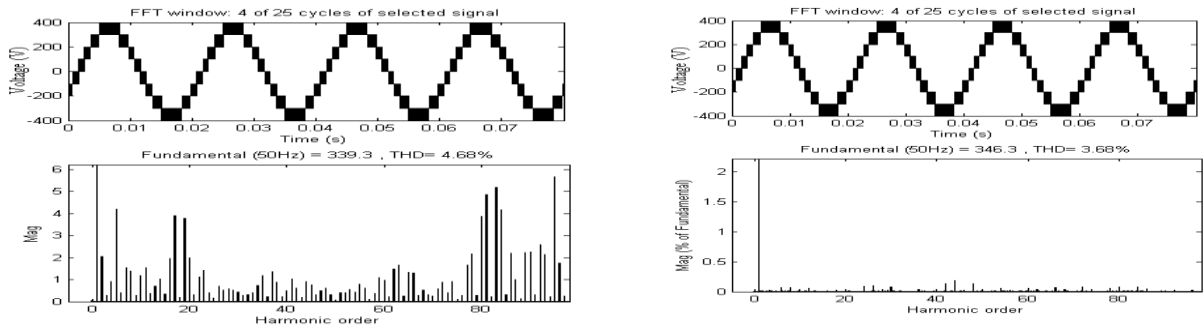


Fig. 6 Output line-line voltages and harmonic spectrum with triangle and u-type carriers

Fig. 6 is the line-line output voltage and harmonic spectrum of cascaded five-level inverter with the modulating technique represented in Fig 5. For this the U-type carriers are used. The harmonic spectrum of cascaded five-level inverter with R-load shows that the total harmonic distortion is 3.68% with 346.3 V

Phase Opposition Disposition (POD)

Carrier signals used in this method are the same in frequency and amplitude but they are different in phase. The carriers above the reference zero point are out of phase with those below that by 180° as shown in Fig.7.

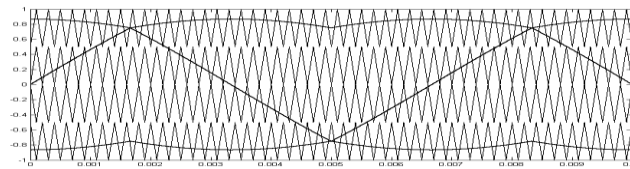


Fig. 7: Generation of gate pulses with triangular carriers

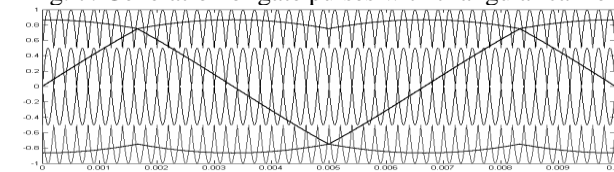


Fig. 8: Generation of gate pulses with U-type carriers

Fig. 7 shows the generation of gate pulses with triangular carriers of cascaded five-level inverter with R-load. In this the reference is OVPWM signal and four triangular carriers are selected. Fig. 8 shows the generation of gate pulses with U-type carriers.

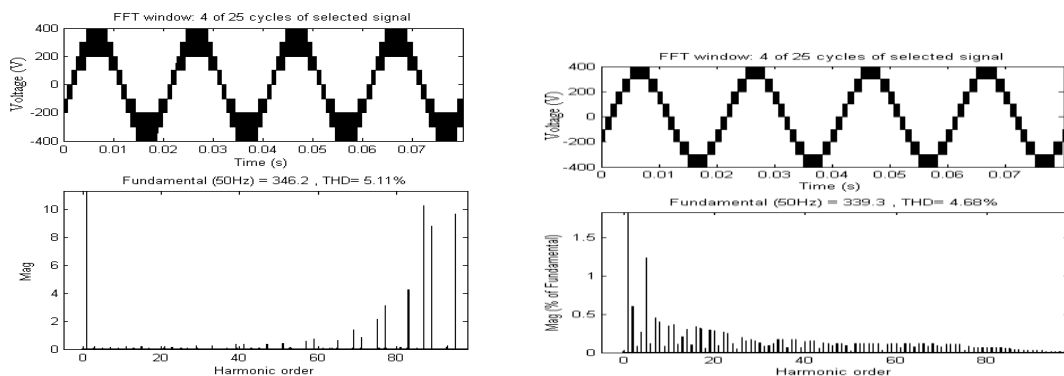


Fig. 9 Output line-line voltages and harmonic spectrum with triangular and U-type carriers

As results obtained in Fig. 9, the harmonic spectrum of cascaded five-level inverter with the modulating technique represented in Fig 7. It shows that the total harmonic distortion is 5.11% with 346.2 V. Fig. 9 also, the line-line output voltage of cascaded five-level inverter with R-load and harmonic spectrum. For this the U-type carriers are used. The harmonic spectrum shows that the total harmonic distortion is 4.68% and fundamental component is 339.3V with the modulating technique represented in Fig 8

Alternative Phase Opposition Disposition (APOD)

In this method carriers have the same frequency and the same amplitude but they are different in their DC offset and phases as shown in Fig. 10. In this method carriers are phase shifted by 180°, so this method uses two degrees of freedom of carriers namely their DC-offset and phases.

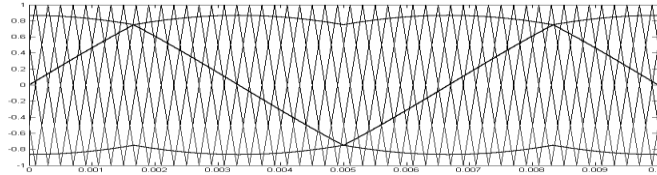


Fig. 10 Generation of gate pulses with triangular carriers

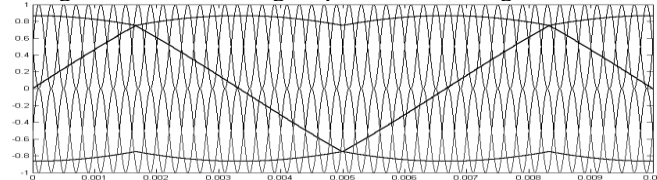


Fig. 11: Generation of gate pulses with U-type carriers

Fig. 10 shows the generation of gate pulses with triangular carriers of cascaded five-level. In this reference is OVPWM compared with four triangular carriers to generate the necessary gate pulses to drive the switches. Fig. 11 shows the generation of gate pulses with U-type carriers.

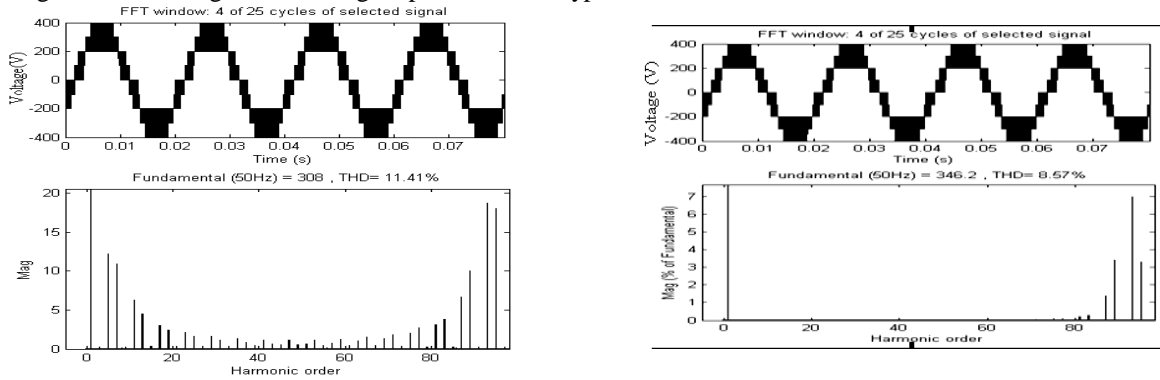


Fig. 12 Output line-line voltages and harmonic spectrum with triangular and U-type carriers

Fig. 12 is the line-line output voltage and harmonic spectrum for the modulating technique represented in Fig 10. For this the triangular carriers are used. It shows that the total harmonic distortion is 11.41% and Fundamental component is 308V.

Fig. 12 also shows the line-line output voltage harmonic spectrum for the modulating technique represented in Fig 11. For this the U-type carriers are used. It shows that the total harmonic distortion is 8.57% and Fundamental component is 346.2V.

Among the discussed techniques, PD technique has less harmonic distortion on line voltages. As it shown PD technique puts the harmonic energy directly into a common mode carrier component so that the harmonics are cancelled in line voltages.

Simulation Results Comparison

In this section the cascaded multilevel inverter simulation results can be shown with R-load by using the modulation techniques of Modified SVPWM. The comparison of simulation results are shown in Table 2 for the following parameters

Input voltage: 400 V

Switching frequency or Carrier Frequency: 5000Hz,

Output Frequency or Reference signal Frequency: 50 Hz

Table 2 The %THD Comparison Of Voltage For Modified SVPWM With Triangular And U-Type Carrier At $F_c = 5\text{kHz}$

f_c of 5KHz	Offset Voltage injected Reference (OVPWM)					
	Triangular Carrier			U-type Carrier		
	PD	POD	APOD	UPD	UPOD	UAPOD
M=1	5.68	5.68	11.41	3.68	5.11	8.57
M=0.86	5.56	6.32	12.56	5.45	5.23	10.38

6						
M=0.8	6.36	7.46	13.01	5.69	6.39	12.25

U-type Position Disposition (PD) is selected as the best among Modified Carrier Modulating Techniques

Table 2 represents the modulation technique of Modified SVPWM. The various Carrier-Based techniques such as PD, POD, and APOD are analyzed and the simulation results are tabulated. In this chapter the Carrier based techniques implemented with triangular carriers and U-type carriers. The results of cascaded multilevel inverter with R-load by using Modified SVPWM are obtained. The conclusion from this table is from all the above techniques the Position Disposition (PD) have the low harmonic distortion. A summary of THD for Cascaded multilevel inverter by using Modified SVPWM modulation techniques is presented. Cascaded five-level inverter is simulated for modified reference with triangular carriers and modified reference with modified carrier (u-type).

The simulation results for output voltage with harmonic spectrum are presented, it is concluded that Cascaded five-level inverter of modified reference with U-type carrier technique has good harmonic spectrum with THD (3.68%) for the switching frequency of 5KHz.

IV. Prototype Model For A Single Phase Induction Motor

Generation of proposed pulses for Cascaded 5-level Inverter Wave forms using Integrated Software Environment (ISE 12.1)

The proposed modulating signals are generated by writing the Verilog code and embedded in Xilinx FPGA Controller board by using ISE 12.1 software. The screen shots are obtained from the simulation of Verilog code using Modelsim 6.0 software.

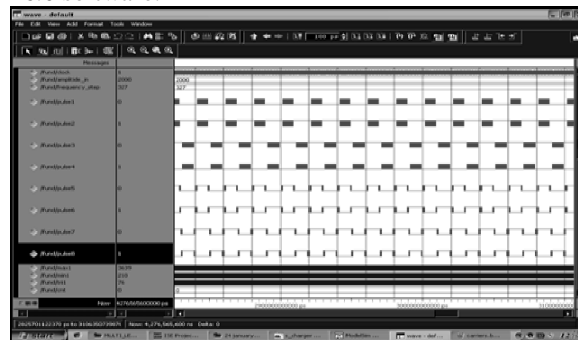


Fig. 13 Triggering pulses for 8 IGBTs using OVPWM

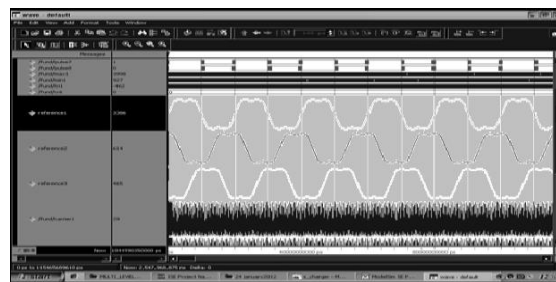


Fig. 14 Modified Reference Signals used in OVPWM

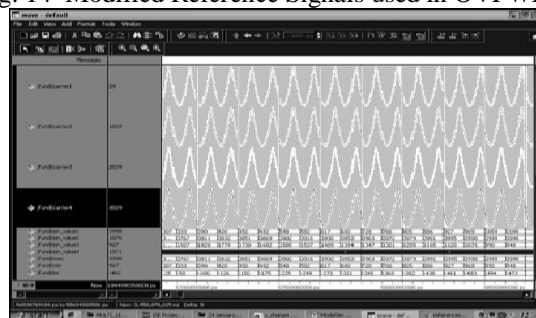


Fig. 15 Level shifted U-type PD carrier signals used in OVPWM

Triggering pulses are represented in Fig 13 for the two H-bridges(i.e. eight IGBTs). The respective pwm pulses are generated with the help of offset voltage injected in sinusoidal reference signals as shown in Fig 14, compared with the level shifted four U-type carrier signals as shown in Fig 15.

Hardware Description

i) INPUT -AC SOURCES

Two Transformers of 230V/110V – 0 - 110V for two individual sources of two H-bridges -Two Transformers of 230V/12V,8V for two H-bridges, to supply V_{CC} for various ICs used as optocouplers , comparators etc.

- Bridge rectifier (MB 356)
- Voltage rating - 600V
- Current rating – 35A

ii) CAPACITORS AS DC SOURCES

Two sets of Capacitors for two H-bridges 2200 μF/450 V parallel with 330 μF / 450 V

iii) FSBB20CH60F (IGBT MODULE)

- UL Certified No. E209204 (SPM27-CA package).
- 600V-20A 3-phase IGBT Inverter Bridge including control ICs for gate driving and Protection

iv) FPGA (XILINX SPARTAN 3E)

To generate the firing pulses of proposed modulating technique in ISE 12.1 with the help of Verilog programming

v) OTHER ICs FOR ISOLATION

To provide isolation from Low voltage side i.e. FPGA side and High voltage side i.e. H-bridge Inverter side

- OPTOCOUPPLERS (4506)
- COMPARATORS (TL084)
- IC 4081

vi) LOAD

- Single Phase Induction Moto
- 0.5 HP, 230V, 4.3 A, 1440 rpm

Block Diagram:

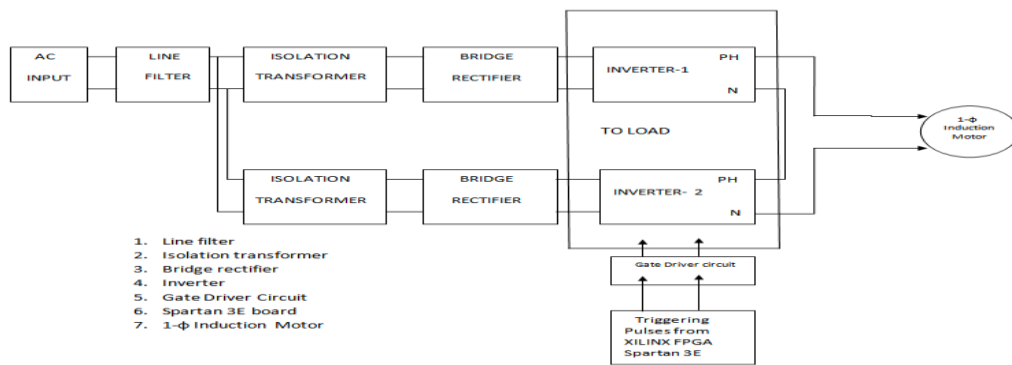


Fig 16 Block Diagram of proposed prototype model

Fig 17 shows the hardware kit implemented for the cascade operation of a 5-level inverter. The circuit consists of rectifier, capacitors, IGBTs, firing circuit, isolation circuit. We can see all the components needed as per block diagram shown in Fig 16, are embedded in the hardware kit..

Explanation of Block Diagram

In the block diagram, it is represented with INVERTER-I and INVERTER-II , are the two H-bridges. The individual DC sources for these two - three level inverters are obtained from the bridge rectifier which feed from a isolation transformer of 230V/110V as shown in Fig 9.4. The switching signals for the two H-bridges are generated using Xilinx-FPGA (Spartan3e)-Verilog code for the proposed modulating technique are programmed in ISE 12.0 environment and embedded in FPGA board to generate triggering pulses. The proposed gate pulses obtained from FPGA board may not sufficient to trigger the IGBTs. So, these pulses are amplified in gate driver circuit and applied to the gate terminals of IGBTs. The gate driver circuit performs three operations, the first one is to boost the FPGA output pulse, second one is the impedance matching for the FPGA and gate & emitter terminal circuit and the third one is to provide is isolation between the pulse generation unit to power circuit

.Single phase five level inverter circuit configuration with five level inverter block consist eight power IGBTs to obtain five level AC output.

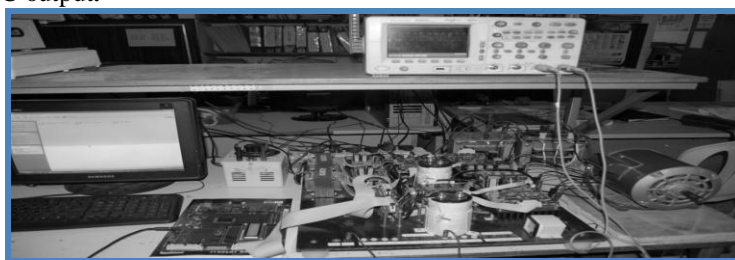


Fig 17 Cascaded 5-level Inverter Hardware Kit

V. ANALYSIS OF RESULTS

Hardware Results

Topology: Single phase Cascaded 5-level H-bridge Inverter

Input Voltage(rms): 230V (two individual dc sources of 162.5 V)

Switching Frequency: 10 KHz

Nature of output: m-levels i.e. 5-levels

Load: Lamp load

Table 3 Hardware results of a prototype model with lamp load

S.No	M	Output voltage		Output current		Remarks Nature of output
		Fundamenta l (rms)	% THD	Fundamental (rms)	% THD	
1.	0.9	200.62	21.99	0.40	22.09	5-levels
2.	0.8	193.15	21.15	0.39	20.93	5-levels
3.	0.7	185.26	21.01	0.38	21.565	5-levels
4.	0.6	160.14	21.59	0.37	21.59	5-levels
5.	0.5	140.02	23.10	0.36	23.10	3-levels
6.	0.4	110.03	24.13	0.35	24.13	3-levels
7.	0.3	70.45	25.12	0.34	25.12	3-levels
8.	0.2	53.82	26.34	0.32	26.34	3-levels
9.	0.1	35.63	28.37	0.30	28.37	3-levels

Load: Single phase induction motor of capacitor start type (0.5 HP, 230 V, 4.5 A, 1425 rpm, 50 Hz) on No-Load

Table. 4 Hardware results of a prototype model with SIM on No-Load

S.No	M	Speed (rad/sec)	Output voltage		Output current		Remarks Nature of output
			Fundamental	% THD	Fundamental	% THD	
1.	0.9	1492	207.31	22.45	3.2	40.01	5-levels
2.	0.8	1486	192.34	21.58	3.23	34.06	5-levels
3.	0.7	1482	158.78	20.67	3.20	27.71	5-level
4.	0.6	1482	135.16	20.84	3.9	35.2	5-levels
5.	0.5	1485	100	25.7	4.3	310.3	3-levels
6.	0.4	1480	85	26.0	5.2	35.0	3-levels

Load : Single phase induction motor of capacitor start type(0.5 HP, 230 V,4.5 A,1425 rpm, 50 Hz) Load

Table .5 Hardware results of a prototype model with SIM on Load

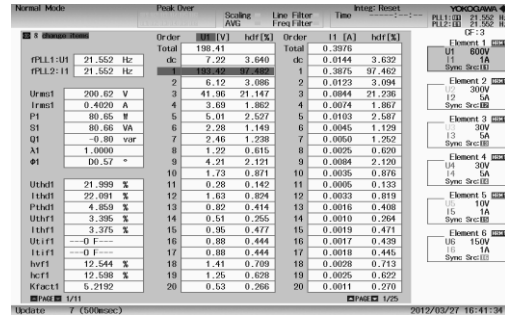
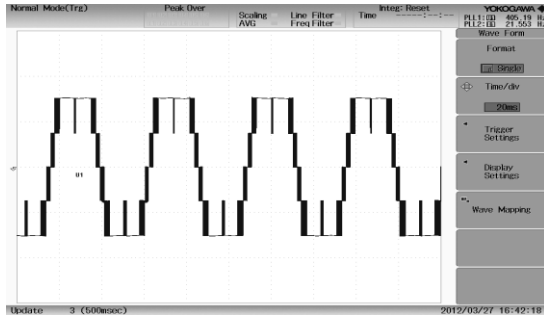
M	Speed	Output voltage		Output current		Remarks Nature of output
		Fundament al	% THD	Fundament al	% THD	
0.9	1430	220.42	21.3	3.19	38.97	5-Level
0.9	1400	211	22	4.01	27	5-Level
0.9	1450	230	21.20	4.25	26	5-Level

Fpga Controlled Cascaded Mli With Advanced Multilevel Strategies For Harmonic Reduction

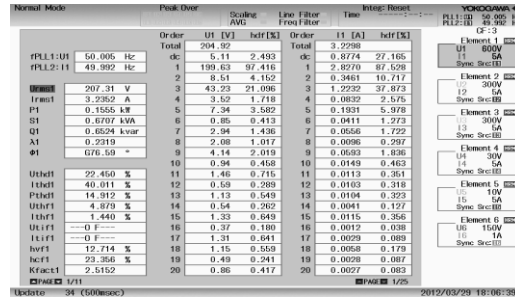
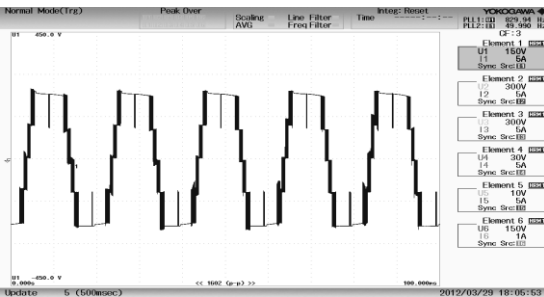
0.9	1438	205	21.43	4.60	25	5-Level
0.8	1490	196.33	22.02	2.64	40.09	5-Level
0.8	1400	177	21	3.6	27	5-Level
0.8	1370	170	22	4.0	23	5-Level
0.8	1422	193	21.54	4.25	22	5-Level
0.8	1416	188.07	22.63	4.60	21	5-Level

Screen shots of Hardware Results

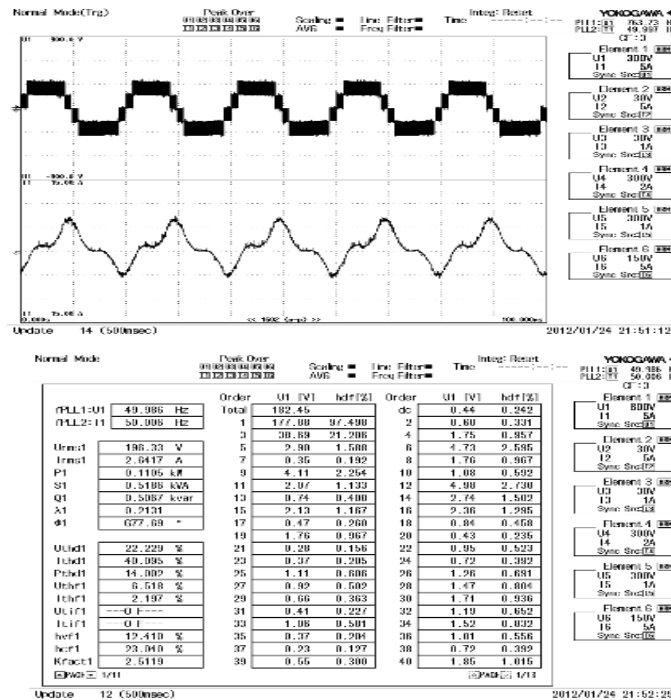
Lamp load



SIM on No-Load



SIM on Load



Order	U1 [V]	U2 [V]	U1 [A]	U2 [A]
dc	0.44	0.242	0.00	0.331
1	177.88	97.498	1.75	98.7
2	0.80	0.331	0.00	0.331
3	38.58	21.208	0.473	2.536
4	1.76	0.967	0.00	0.967
5	2.54	1.295	0.00	1.295
6	1.08	0.592	0.00	0.592
7	0.35	0.192	0.00	0.192
8	4.11	2.254	0.00	2.254
9	0.1105	0.056	0.00	0.056
10	0.1105	0.056	0.00	0.056
11	2.07	1.133	0.00	1.133
12	0.74	0.400	0.00	0.400
13	2.13	1.167	0.00	1.167
14	0.47	0.260	0.00	0.260
15	1.76	0.967	0.00	0.967
16	0.29	0.156	0.00	0.156
17	0.37	0.205	0.00	0.205
18	1.11	0.606	0.00	0.606
19	0.92	0.509	0.00	0.509
20	0.66	0.363	0.00	0.363
21	0.41	0.227	0.00	0.227
22	1.06	0.581	0.00	0.581
23	0.37	0.204	0.00	0.204
24	0.23	0.127	0.00	0.127
25	0.65	0.300	0.00	0.300

VI. CONCLUSIONS

In this chapter, both simulation results and hardware prototype model results are correlated. Harmonic analysis carried out using Simulink FFT in case of simulation and Power analyser WT1800 manufactured by YOKOGOWA. It is proved that Single phase Cascaded MLI output voltage %THD is varied between 21% to 28% as modulation index varied from 0.9 to 0.3. It is also proved that this output voltage THD does not vary for the lamp load or linear load and non linear load or Induction motor. When the analysis comes to output current, it is more sensitive to load variations. The FFT analysis of output voltage and current is similar to the linear loads. For Non linear loads current THD varies depends upon the inductive nature of the load.

In this analysis, Harmonic analysis is obtained for a Single phase Cascaded topology fed single phase induction motor of 0.5 H.P with the proposed modulating technique implemented by FPGA. The output voltage wave form of implemented topology contains only five levels i.e. 'm-levels', because it is a single phase cascaded five level inverter. Single phase induction motor has vast variation in the construction when compared to a three phase induction motor. The known fact is that small rating motors are having low power factors, so that it draws more current. This is the reason, why current wave form reaches nearer to sinusoidal as it is go on increasing. As the load current increases, the corresponding THD decreases. So, that it can be expected that the higher rating motor i.e. > 5 H.P can be given good performance in current THD, when they feed from Cascaded Multilevel inverters of the proposed modulating technique.

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