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# An Area efficient and more accurate DA-based DCT with more compression rate

Ashok Kumar Gulla[1], K.Rajasekhar[2]
[1,2](Electronics and Communication Department, ASR College/ JNTUniversity, India)

***Abstract :*** *In this paper, a scheme for the design of pipeline architecture for a real-time computation of the 2-D DCT has been presented. The objective has been to achieve a low computation time by maximizing the operational frequency and minimizing the number of clock cycles required for the DCT computation, which, in turn, have been realized by developing a scheme for enhanced inter- and intra stage parallelisms for the pipeline architecture. it is most efficient to map the overall task of the DCT computation to only two pipeline stages, i.e., one for performing the task of the level-1DCT computation and the other for performing that of all the remaining decomposition levels. In view of the fact that the amount and nature of the computation performed by the two stages are the same, their internal designs ought to be the same. There are two main ideas that have been employed for the internal design of each stage in order to enhance the intra stage parallelism. The first idea is to decompose the filtering operation into two subtasks that operate independently on the even- and odd-numbered input samples, respectively. This idea stems from the fact that the DCT computation is a two-sub band filtering operation, and for each consecutive decomposition level, the input data are decimated by a factor of two.*

***Keywords –*** *DCT, Pipeline Architecture, 2-D DCT, Intra Stage Parallelisms, Filtering*

## I. INTRODUCTION

The applications of the digital speech and image signals are more and more extensive today than ever before. They usually go through compression before transmission to reduce the bandwidth. The discovery of the discrete cosine transform (DCT) in 1974 [I] provided a significant impact on DSP field. It is believed to be one of the most powerful data compression tools. Consequently, DCT is extensively used in visual communications. In the past decade many papers have been published concerning about reducing the computation complexity, especially the number of multiplications, of DCT. Most of them are efficient with software implementation, but unfortunately due to their irregular structure and complex routing, these algorithms are not suitable for VLSI implementation. Our goal is to design a high speed 4x4 DCT chip suitable for the application in HDTV system. Aimed at this, we derived an algorithm suitable for VLSI implementation. The applications of the digital speech and image signals are more and more extensive today than ever before. They usually go through compression before transmission to reduce the bandwidth. The discovery of the discrete cosine transform (DCT) in 1974 [I] provided a significant impact on DSP field. It is believed to be one of the most powerful data compression tools. Consequently, DCT is extensively used in visual communications. In the past decade many papers have been published concerning about reducing the computation complexity, especially the number of multiplications, of DCT. Most of them are efficient with software implementation, but unfortunately due to their irregular structure and complex routing, these algorithms\ are not suitable for VLSI implementation. Our goal is to design a high speed 8x8 DCT chip suitable for the application in HDTV system. Aimed at this, we derived an algorithm suitable for VLSI implementation. Much architecture has been proposed in order to provide high-speed and area-efficient implementations for the DCT computation [5]–[8]. In [9]–[11], the poly phase matrix of a wavelet filter is decomposed into a sequence of alternating upper and lower triangular matrices and a diagonal matrix to obtain the so-called lifting-based architectures with low hardware complexity. However, such architectures have a long critical path, which results in reducing the processing rate of input samples. On the other hand, the problem of low processing rate is not acute in the architectures that use convolution low- and high-pass filtering operations to compute the DCT [12]–[19]. These convolution-based architectures can be categorized as single- or multistage pipeline architectures. The architectures proposed in [12]–[16] are single-stage architectures in which the DCT computation is performed using a recursive pyramid algorithm (RPA) [20] that results in a reduced memory space requirement for the architectures.

## II. ARCHITECTURES

To perform a 2-D wavelet analysis operation, a chain of processing elements combined with some delay elements, necessary for synchronisation purposes, are assembled together. The architectures used in the proposed framework for both orthonormal and biorthogonal bases are based on a time-interleaved filter's

coefficient allocation approach in combination with two lines of adder [4][5]. In addition to the regularity feature, the architectures are scalable and are able to generate any wavelet filter from both families.

## III. ARCHITECTURES FOR ORTHONORMAL DCT

Figure 2 shows the generic architectures of an area efficient and a high throughput 2-D wavelet filters, respectively. The elements constituting the filters are shown on the right hand side of each structure. The delay elements d1 and d2 are related by d1 X2d2 . X1 isa combination of a de multiplexer and two bit-adders and □2 is a combination of buffer and an bit-adder. The multiplier operators, represented by the asterisk, are similar. An orthonormal DCT is generated easily by adopting the approach proposed in [6].

Due to the fact that the high pass and low pass filters belonging to the orthonormal family are of the same length, the delay elements present a regular structure leading to a simple connection strategy between the low pass and the high pass filter [6].

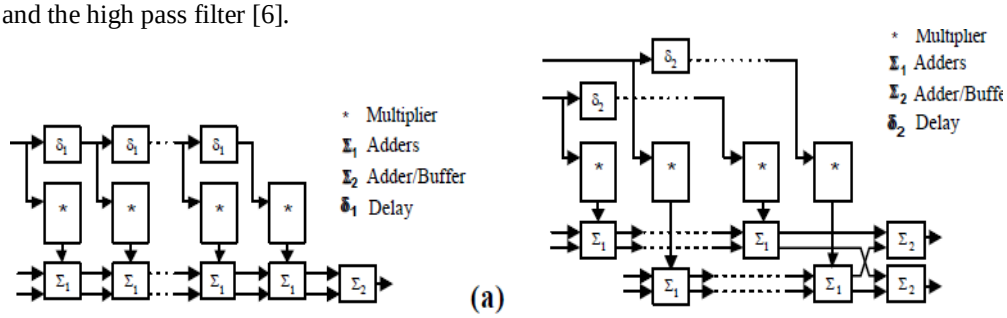



**Fig.2.** Generic Architecture for Orthonormal Filters
(a) Area Efficient (b) High Throughput

## IV. SERIAL-PARALLEL VERSUS DIGIT-PARALLEL

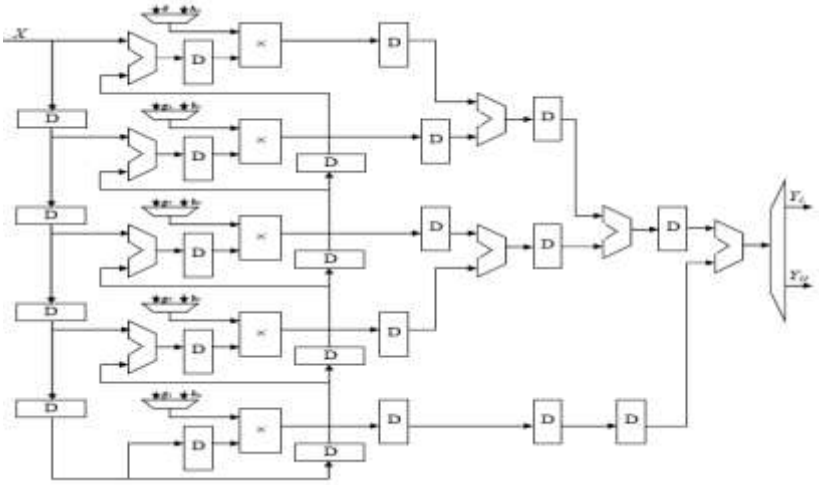
In recent years, the concept of digit-serial arithmetic has been proposed as a compromise between the bit serial and the bit parallel arithmetic [11]. The systems based on this arithmetic give the DSP designers more flexibility in finding the appropriate trade-off between hardware cost and sample rate. However, due to the feedback loop associated, the multiplier obtained using traditional approach can only be pipelined at a digit level. To overcome this problem, a new algorithm that allows different level of pipelining has been developed [9]. To benefit from this approach, the chain of adders of Figure 4 needs to be adjusted to suit the algorithm [9]. In the other hand, since the filtering is based on a multiply and accumulate process, digit adders that can be pipelined at a bit level when extended to a digit size are also required. Details about pipelined digit adders can be found in [12].

## V. PROCESSING ELEMENT

The Processing Element (PE) is invariable through either the wavelet bases or the wavelet supported architectures. It is composed of a bit-multiplier, a de multiplexer and two 1-bit adders (X1 ).

## VI. "TERMINATING" ELEMENT

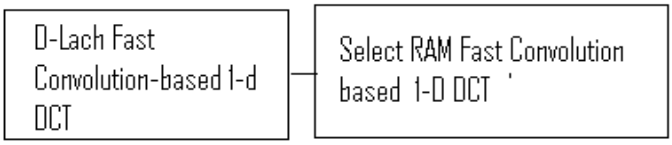
The structure of a Terminating Element (TE) is identical for both bases and both architectures. It is composed of a bit-adder and a buffer ( X2 ).



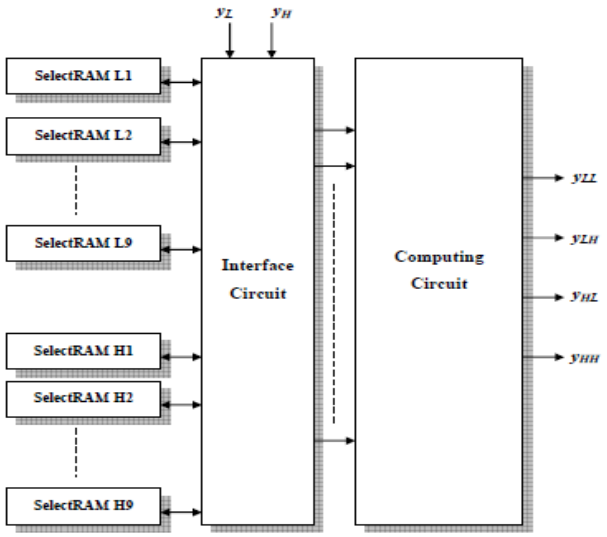
## VII. DELAY ELEMENTS

To handle the peculiarities of the bi orthogonal and the orthonormal basis, it was decided to design two different delay modules. In the case of the ortho normal bases, the generation is easily achieved by connecting side by side either N-1 delay elements 1 *d* or 2(N-1) delay elements 2 *d* . Unfortunately, the generation process in the case of the biorthogonal family is more complicated. More details can be found in [7].

In this approach and to avoid the need of a transpose circuit between the two levels, the system stars the column processing as soon as sufficient numbers of rows have been filtered. Above presents the main 2-D DCT fast convolution based diagram. The proposed FPGA implementation of the 2-D Discrete Wavelet Transform is designed with two fast convolution based blocks. The first one, which is similar to the 2-D block, realizes the row Discrete Wavelet Transform and uses D Latch devices for the X(n) storage. The second achieves the Column Discrete Wavelet Transform using an FPGA block RAM storage of the computed rows.




**YL** and **YH** present the first level outputs. The **YLL**, **YLH**, **YHL** and **YHH** present the second level and the 2-D DCT outputs. **YL0, YL1, YL2, ….**. are obtained at clock cycles 9, 11, 13, … and **YH0, YH1**, **YH2, …** are obtained at clock cycles 8, 10, 12, .. . respectively. The first row of **YLH** and **YHH** can be obtained after the beginning of the third row storage of the first level outputs. After the beginning of the fifth storage of the first level outputs, we can obtain the second row of **YLH** and **YHH** and the first row of **YLL** and **YHL** (Fig. 6).Nine FPGA block RAM in Dual-Port Mode are required to accomplish the second level of the Parallel Distributed 2-D DCT Architecture with the (9,7) wavelet filters. The SelectRAM 2-D DCT fast convolution-based Modules is composed by blocks RAM, interface circuit and a computing circuit (Fig. 7). The computing circuit presents the main architecture of the D-Latch 2-D DCT fast convolution-based.




At each step of computing, only one block RAM is selected in write mode:

- *1st step:*

Block RAM 1 and block RAM 2: read mode
Block RAM 3: write mode

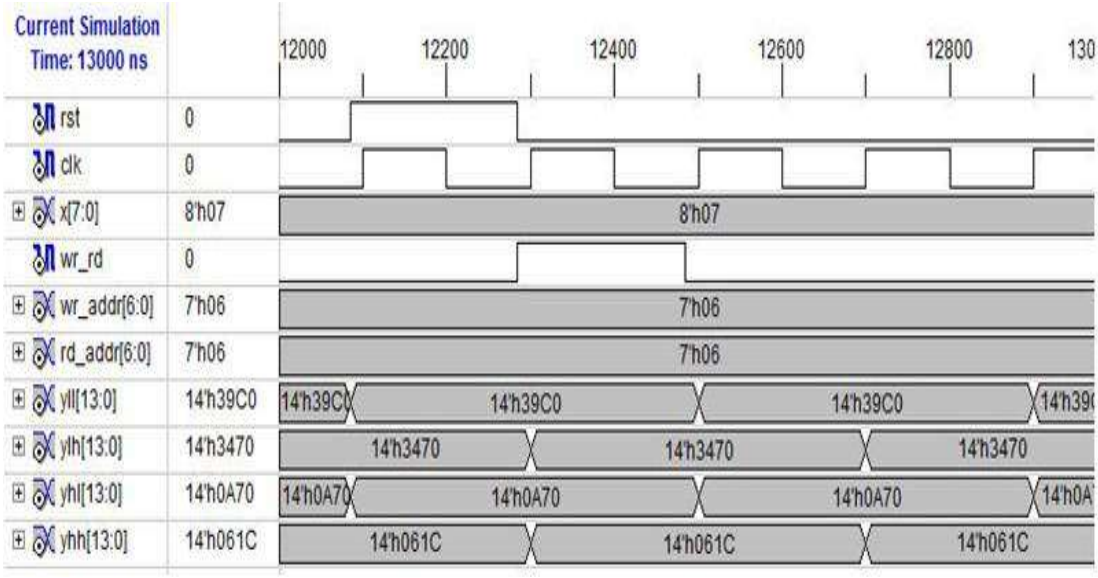
- *2nd step:*

Block RAM 1 to block RAM 4: read mode
Block RAM 5: write mode

- *Advanced step:*

Block RAM 1 to block RAM8: read mode
Block RAM 9: write mode

## VIII. SIMULATION RESULTS




## IX. CONCLUSION

In this paper, we have proposed a parallel architecture for very high-speed computing Discrete Wavelet Transform using SRAM and FIFO memory. To produce one output in every clock cycle in addition to reduce the critical path as well as an efficient memory area, new fast convolution-based architecture approach is performed. In this approach, the system stars the column-processing as soon as sufficient numbers of rows have been filtered. Two fast convolution based blocks, for the one-dimensional (1-D) discrete wavelet transform (DCT), are used to accelerate the computing

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