

## Simulation of Tree Adder Designed With Complementary Energy Path Adiabatic Logic

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**Abstract:** In recent years, a low power design approach has become more appropriate due to the exponentially increasing power dissipation. This has motivated the designers to explore various design approaches to reduce power dissipation in VLSI circuits. Energy recovery circuits based on the adiabatic logic principle have been proved to be a promising approach among various non-conventional low power design methodologies. The CEPAL (Complementary Energy Path Adiabatic Logic) inverter being an adiabatic logic, has proved its advantage through the minimization of the energy dissipation over static CMOS. Its performance is also compared against the CAL (Clocked Adiabatic Logic) inverter, which is a dynamic type of adiabatic logic. This paper presents the implementation of the 2-bit Sklansky tree adder structure, designed with CEPAL logic, which has been chosen due to its increased fan-out that results in reduced latency and improved speed performance. The analyses are carried out using the EDA tool which is the Electric VLSI Design System using 130 nm technology library. Electric is used to draw schematics and to do integrated circuit layouts LT-Spice Tool is used to simulate the SPICE deck which is produced from generated schematics and layouts.

**Keywords-**Adiabatic logic, CAL, CEPAL, PG Logic, Sklansky tree adder.

### I. Introduction

Power minimization is one of the primary concerns in today VLSI design methodologies because of two main reasons one is the long battery operating life requirement of mobile and portable devices and second is due to increasing number of transistors on a single chip leads to high power dissipation and it can lead to reliability and IC packaging problems. The low-power requirements of present electronic systems have challenged the scientific research towards the study of technological, architectural and circuitual solutions that allow a reduction of the energy dissipated by an electronic circuit.

Adiabatic logic presents a promising alternative to conventional CMOS for the realization of low power electronics. The basic difference between two logics is shown in below Fig.1. Energy recovery techniques and adiabatic logic topologies minimizes energy dissipation by maintaining low voltage drop across conducting devices at all times. The undissipated energies related to the charges stored in the circuit capacitors are recycled. Thus the energy is not dissipated as heat. This method can usually be applied in addition to other approaches like power supply voltage reduction and algorithmic techniques for reduced logic transitions. In conventional CMOS logic we use constant voltage source to charge the load capacitance whereas all adiabatic logic families are based on the time varying ramp voltage supply.

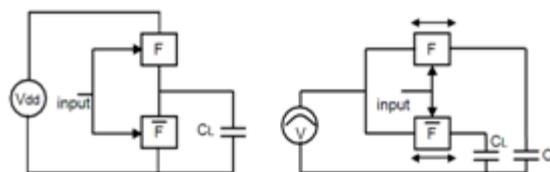


Figure1 conventional CMOS logic equivalent adiabatic logic

The following mathematical analysis, based on time period (T), stored charge (CLV), load capacitance CL and channel resistance R is sufficient to understand adiabatic logic principle.

$$P_{diss} = 2\left(\frac{RC_L}{T}\right)C_L V_{DD}^2.$$

Hence as given by above equation, keeping the clock transient time T much larger than intrinsic time constant RC of a device; we can reduce power dissipation in a switching transition.

In literature, various kinds of adiabatic circuits proposed all of them can be grouped into two fundamental classes: fully adiabatic circuits and quasi-adiabatic or partial energy recovery circuits. In the first class, in

particular working conditions can consume asymptotically zero energy for operation, the large area occupation and the design complexity make these circuits not competitive with traditional CMOS where as in second class circuits designed to recover large portion of the energy stored in the circuit node capacitances. This energy loss drawback however allows a good trade-off between circuit complexity and then area occupation.

The literature has brought out several types of adiabatic logic circuits namely, PAL (Pass transistor adiabatic logic), PFAL (Positive feedback adiabatic logic), 2N2P/2N-2N2P. The static adiabatic logic circuits are CEPAL, QSERL (Quasi static energy recovery logic), QSSERL (Quasi static single phase energy recovery logic) and CAL is the dynamic adiabatic style.

Addition is one of the most commonly used arithmetic operations. The parallel-prefix tree adders are identified to be the best performing adders. The reduced logic depth of the adders, reduced area and synchronization overhead, and the resultant lesser power consumption are the major factors. Hence, present work aims at the energy recovery type of logic that employs the parallel prefix tree adder to validate the logic.

## II. Static Vs Dynamic Adiabatic Logic

The schematic structure of the static energy recovery logic CEPAL is employed using Electric tool in the design, is shown in Fig.2. The basic structure of a CEPAL circuit and simulated waveforms of CEPAL inverter are shown in below figures. CEPAL is composed of two charging pMOS diodes (P1 and P2), a pull-up (P) network, two discharging nMOS diodes (N1 and N2) and a pull down (N) network. Two sinusoidal supply clocks in complementary phases (i.e. PC and PCbar) are used. Assume that initially output (Vout) is LOW, and the P-network is on while the N-network is off then the output either follows PC or its complement as it swings HIGH. Once Vout becomes HIGH the followed power clock then swings down and output node of CEPAL becomes floating but this situation is soon removed because at the same time the complement of the followed power clock swings up, thereby eliminating the weak HIGH at the output node. Similarly the weak LOW at the output can be eliminated by the complementary energy paths.

The elimination of redundant switching of the output nodes and the consequent reduction in adiabatic power dissipation are the major advantages of the CEPAL circuit. This beneficial characteristic of CEPAL identifies the circuit as the static type.

The schematic and layout of CEPAL inverter are drawn using the ELECTRIC VLSI Design Tool and are shown in below Fig.2&Fig.3. The simulated output of CEPAL Inverter is shown in Fig.4 using LT SPICE tool.

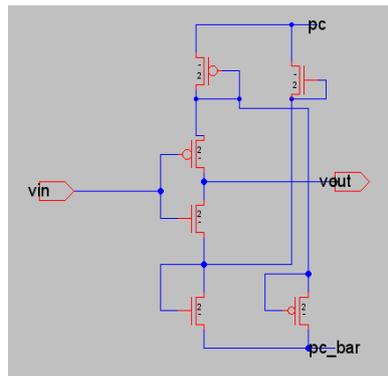


Figure2: CEPAL inverter schematic

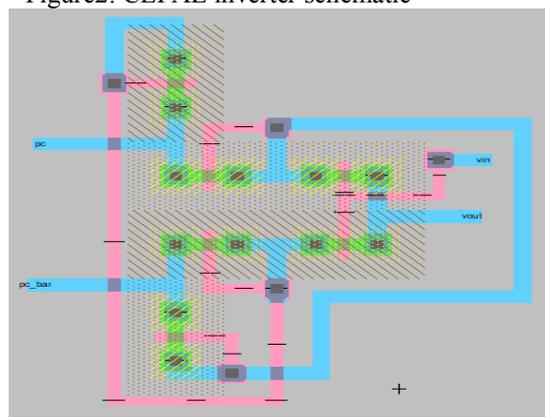


Figure3 CEPAL inverter layout

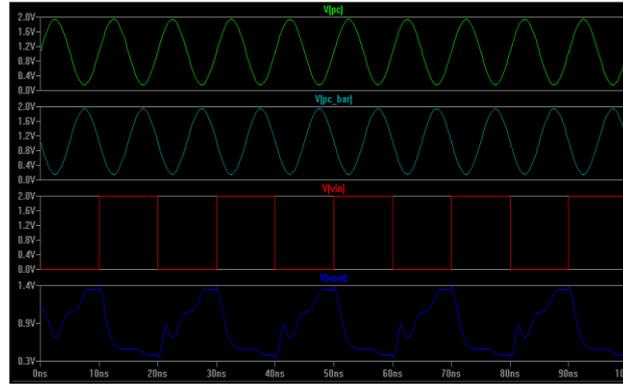


Figure4 waveform of CEPAL inverter

The structure of the Clocked Adiabatic Logic CAL inverter is shown in Fig.5. It consists of cross coupled transistors to offer the memory function. The structure uses auxiliary clock timing signal to enable the logic function in one power clock. To understand the operation of the circuit, let us assume that initially the auxiliary clock CX is high during the first clock period. This enables the logic evaluation. When the input signal in is high, the right side of the logic tree is switched on and the output signal out is low and its compliment Outbar closely follows the power clock. In other words, the output node switches for every power clock. During the subsequent clock period, the auxiliary clock signal CX is low which disables the logic evaluation. The previously stored logic state remains at the outputs due to its memory irrespective of the input signal applied to the system. Therefore the CAL takes the new input in every other power cycle. Due to this single phase operation of the dynamic adiabatic logic, CAL is used to study the performance advantages of static logic CEPAL against dynamic logic.

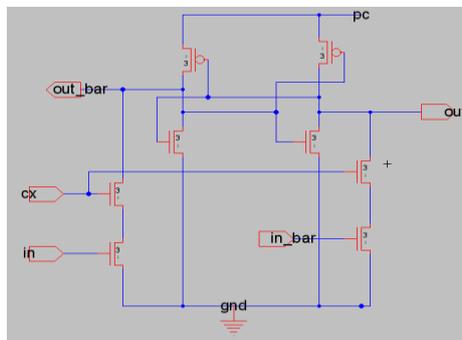


Figure5 CAL inverter schematic

The layout and simulated waveform of CAL Inverter are shown in Fig.6 and Fig.7.

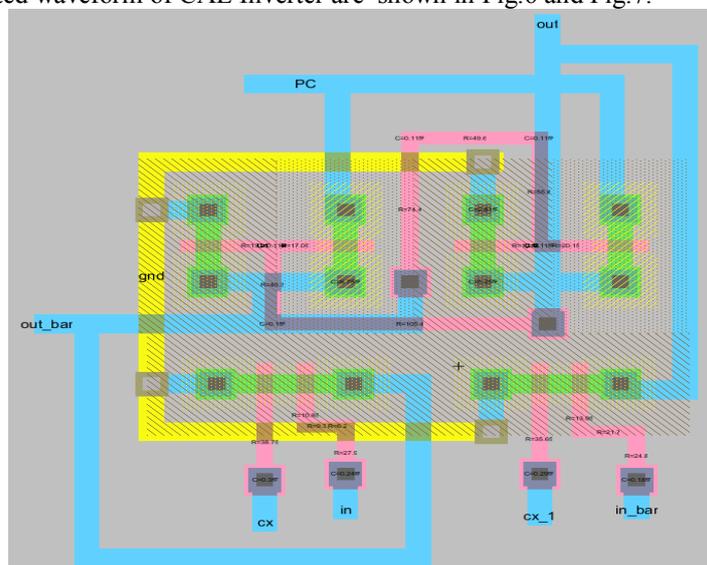


Figure6 CAL inverter layout

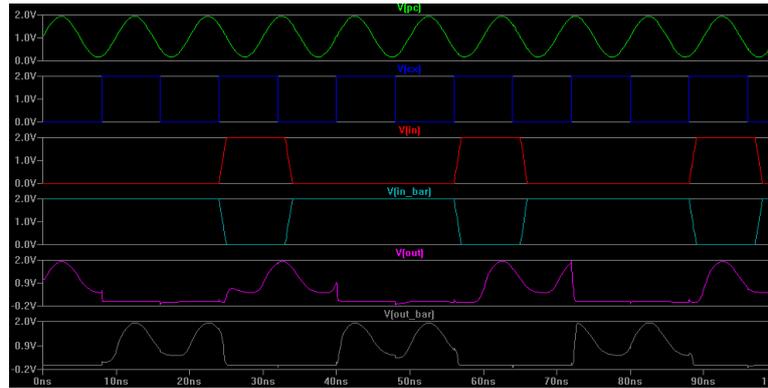


Figure7 waveform of CAL inverter

The operational differences between the static and dynamic inverters are shown in Fig.4 and Fig.7, with the help of the simulated input and output transients of CEPAL and CAL inverters. Waveform 3 depicts the response of CEPAL inverter with the output changing only with respect to the change in the input conditions. This is nearly like a static CMOS inverter. The output does not switch for all the power clock cycles. This feature makes it identifiable as a static inverter. On the other hand, waveform 6 depicts the output node switching for every power clock cycle. That is, the output follows the power-clock for the same input. This is the property that makes the CAL type of adiabatic logic a dynamic inverter.

The experimental work consists of simulating the CMOS, CEPAL and CAL circuits using LT SPICE simulator with all the transistors of equal sizes. The supply voltage, power clock frequency (fPC), input frequency (fin) and load capacitance are 2.0V, 100MHz, 50MHz and 10fF respectively. The power dissipation among three inverters is shown in the below table 1.

Table1: The power dissipation among three inverters

NAME OF THE CIRCUIT	POWER DISSIPATION (μW)
CMOS	40
CEPAL	4E-20
CAL(Clock Transient time=16ns)	2.5E-20

### III. Structure And Design Of Adiabatic Tree Adder

Binary addition is one of the most primitive and most commonly used applications in computer arithmetic. The requirements of the adder are that it should be primarily fast and secondarily efficient in terms of power consumption and chip area. Parallel-prefix adders are suitable for VLSI implementation since they rely on the use of simple cells and maintain regular connections between them. Here, the Sklansky type of tree adder is preferred due to its lower power consumption than that incurred by other tree adder structures.

Parallel Prefix adders (PPA) are family of adders derived from the commonly known carry look ahead adders. These adders are best suited for adders with wider word lengths. PPA circuits use a tree network to reduce the latency to  $O(\log_2 n)$  where ‘n’ represents the number of bits. A three step process is generally involved in the construction of a PPA.

The static adiabatic logic, CEPAL is validated for its functioning through simulation of the tree adder structure. Several tree structures have been proposed to carry out parallel carry computation for wide word length adders. The tree structures proposed by Kogge and Stone and Sklansky adder are the fastest among the already proposed structures. It can be noted that this structure realizes the advantage in terms of reduction of delay to  $(\log_2 N)$  and reduced latency of computation. Hence, this paper uses the Sklansky tree adder to validate the logic due to its high speed of operation.

Fig.8 shows the three step addition process used in computing the *Propagate* and *generate* signals of 2-bit adder. These signals are used to calculate the carryout signal for the generation of SUM. The first and third steps are common for any tree adder structures. Fig.9 and Fig.10 show the PG (Propagate - Generate) logic for the Sklansky tree adder and the basic modules used in the PG block.

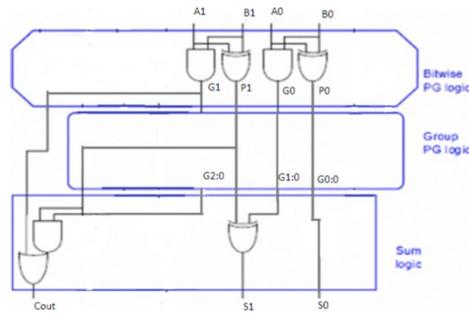


Figure 8 propagate generate circuit

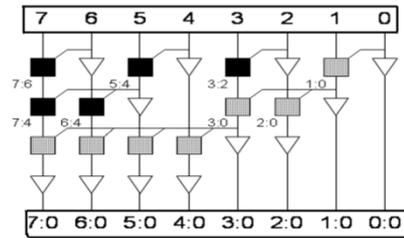


Figure 9 8-bit Sklansky tree adder

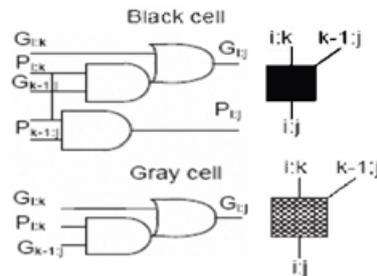


Figure 10 AND OR AND, AND OR

### 3.1 2-Bit Sklansky Tree Adder

The schematic design of the circuit using CEPAL is made for the tree adder. The circuit design is done hierarchically, through the instantiation of the individual modules, such as AND, XOR, OR, AND-OR, AND-OR- AND & PG (Propagate-generate) cells. The individual modules are constructed using pre-layout simulation through the Schematic Electric tool and the designs are exported to the LT Spice circuit Simulator.

The following figures show the 2-bit Sklansky Tree Adder and its gate level circuit.

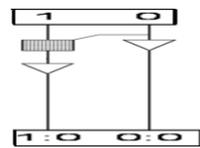


Figure 11 2-bit Sklansky tree adder

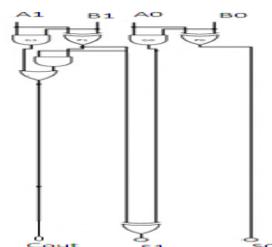


Figure 12 gate level circuit

#### IV. Results And Discussion

In this section, the functionality of proposed CEPAL adder is examined and compared the results with the CMOS adder. The simulations were performed using LT SPICE simulator USING 130nm technology. The supply voltage, power clock frequency (f<sub>PC</sub>), input frequency (f<sub>in</sub>) and load capacitance used are 2V, 100MHz, 50MHz and 10fF respectively. Fig.15 shows the simulation waveform of a CEPAL adder. The power comparison of CMOS and SKLANSKY CEPAL adders is shown in the table2.

Table2: Power dissipation of Adders

NAME OF THE ADDER	TRANSISTOR COUNT	POWER DISSIPATION (μW)
CMOS ADDER	60	18.668
CEPAL ADDER	128	0.00049

In this paper, the implementation of 2-bit Sklansky tree adder circuit using CEPAL is presented. The CEPAL structure, being a static type of logic, incurs the reduced switching activity than the dynamic adiabatic logic CAL. Simulations indicate that the CEPAL realizes energy advantage against the static CMOS.

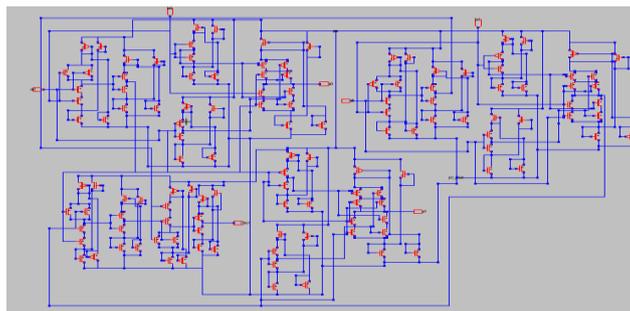


Figure13 schematic of 2-bit Sklansky adder

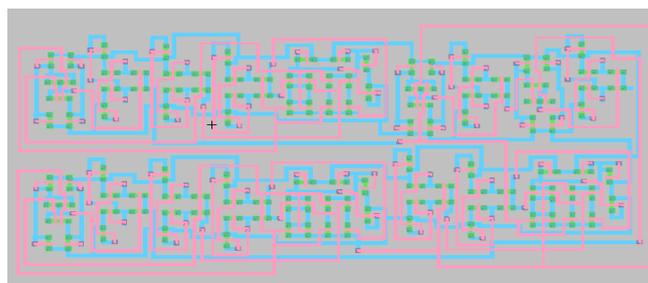


Figure 14 layout of 2-bit Sklansky adder

The results proved that the power comparisons for the Sklansky adder are best with CEPAL logic style over static CMOS using 130nm technology file. The Schematic and Layout of CEPAL 2-bit adder are shown in Fig.13 & Fig.14 using Electric tool. The simulation results of CEPAL tree adder are shown in below Fig.15.

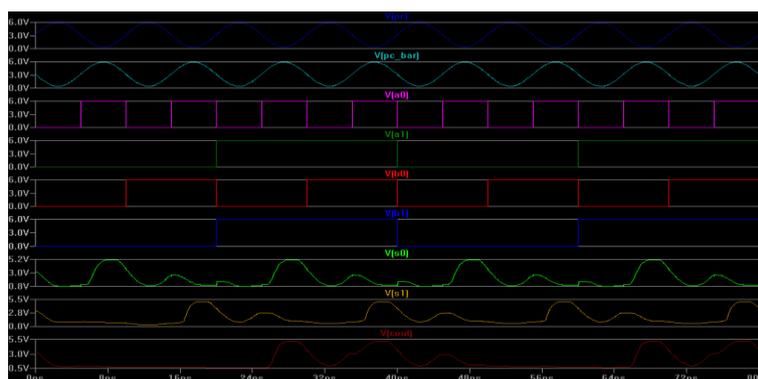


Figure15 simulation results of 2-bit Sklansky adder

## V. Conclusion

The CEPAL uses increased number of transistors than the CMOS and CAL logic styles due to the necessity of using the MOS diodes, in the charging/discharging process paths. These MOS diodes used in the CEPAL structure makes it identified as a static logic and the use of diodes helps in reducing the switching activity. The main advantage of CEPAL over CAL is the simpler clock generator circuitry. This is due to the reason that the CAL employs the square wave auxiliary clock signal along with the sinusoidal power clock. The results also prove that the CEPAL is suitable for optimal speed performance applications.

As a future scope the CAL circuit equivalent realizes more energy efficiency against the static CMOS. However, the CAL realizes this advantage at the cost of additional square wave clock signal and increased number of devices in the pull-down structure of the adiabatic latch.

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