

Domino Logic Topologies of OR Gate with Variable Threshold Voltage Keeper

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Abstract: In this paper, we tend to take four domino circuit topologies to boost the strength and lower the consumption of power. A high speed and noise immune domino logic circuit is given that uses the property of the footer semiconductor to raise the sensitivity of the dynamic node to noise and eventually in improved performance. Dynamic logic circuits are used for prime performance and high speed applications. We tend to analyze and compare completely different domino logic style topologies for lowering the sub-threshold outpouring current in standby mode NMOS block, increasing the speed and increasing the noise immunity. We tend to compare power, delay, and Power Delay Product (PDP) of various topologies. Simulation is finished employing a 45nm cadence tool for eight input OR circuit. Our projected circuits scale back power consumption by 100 percent to 35 the troubles, improvement of unity noise gain of 39% to 85% and have a higher figure of advantage as compared to conditional keeper domino. The simulation results unconcealed that prime Speed Conditional keeper Domino (CKD) circuit offers the most effective ends up in terms of reduction in delay and power consumption as compared to different circuits.

Key words: CMOS, domino logic, keeper ratio, Standby power, Noise immunity, Lower power design.

I. Introduction

Domino logic is incredibly quick and needs less space as compared to static CMOS logic. It's utilized in a high performance essential system like microchip, multiplexor etc. because the technology is scaled down, over voltage is reduced. This reduces the ability consumption. The brink voltage is additionally scaled to take care of the desired performance. Low threshold voltage of the electronic transistor, increase the sub threshold AND circuit chemical compound outpouring current [1, 2]. However, low threshold voltage makes the domino circuit a lot of at risk of input noises. The most supply of noise signal in deep-submicron circuits are XT, outpouring current, charge sharing and provide noise. These noise signals scale back the lustiness of the domino circuit. High outpours current discharges the dynamic node and build the logic failure of the domino circuit. The keeper is sized weaker than the pull-down network, so as to permit quick analysis, whereas maintaining Associate in Nursing equal precharge-evaluation delay. The keeper quantitative relation K is outlined as

$$K = \frac{\mu_p \left(\frac{w}{L}\right) \text{ keeper transistor}}{\mu_n \left(\frac{w}{L}\right) \text{ evaluation transistor}} \quad (1)$$

Where W and L denote the dimensions of an electronic transistor, μ_p and μ_n are the mobilities of hole and electron, severally. The dimensions of the pull down network is mounted and therefore the size of the keeper is variable. Increasing the worth of K improves the lustiness, however, has two negative effects on power consumption. Initial dynamic and output node capacitance will increase, that increase change power consumption. Second, it will increase the rivalry, current between the keeper and therefore the pull down network. That will increase the short power consumption. Up to a size of the keeper conjointly increase the delay of the domino circuit [3-7]. This technique isn't a reliable answer as a result of it will increase the speed and power consumption of the domino circuit. Associate in nursing different standard technique to boost circuit, lustiness are victimization high threshold voltage electronic transistor at the expense of speed [8-11]. Totally different techniques are planned within the literature to deal this issue. High speed domino logic and conditional keeper domino are the effective technique as compared to standard apodous domino logic circuit. During this paper, we tend to propose 3 lustiness footed domino logic circuits and one apodous domino logic circuit. These circuits use atiny, low voltage at the supply of the pull down network within the standby mode. The rest of the paper is organized as follows.

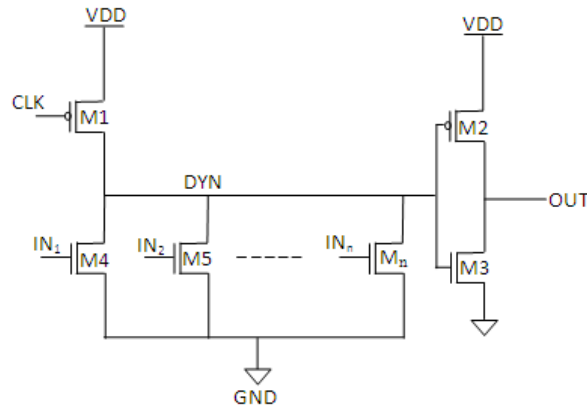


Fig. 1: standard footless Domino high fan in OR Gate without keeper

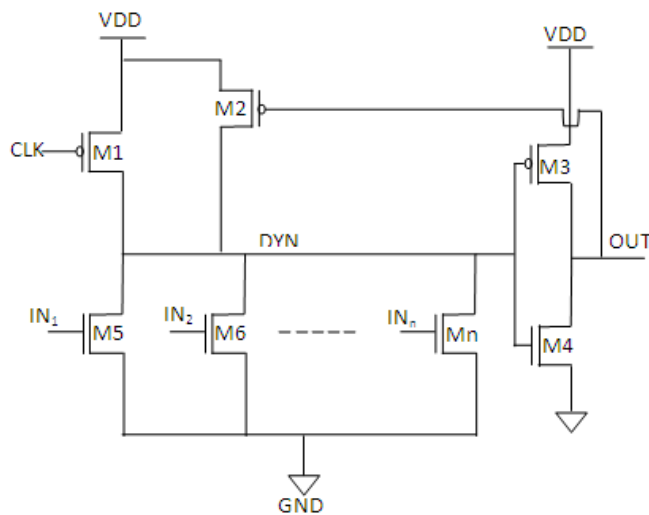


Fig. 2: Standard footless domino high fan-in OR gate with keeper

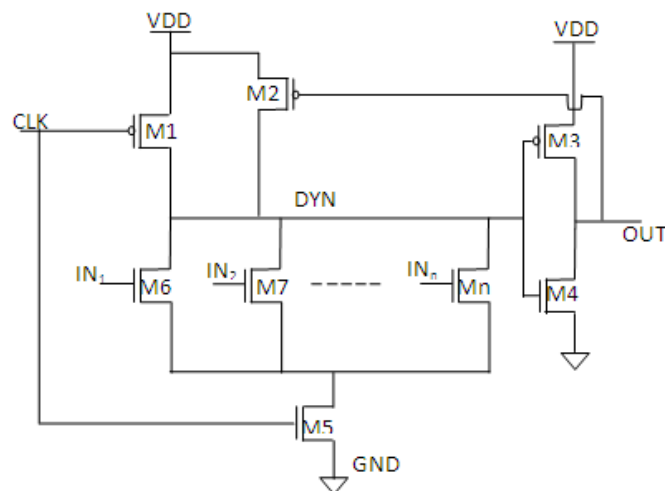


Fig 3: Standard footed domino high fan-in OR gate.

Dynamic node of the apodous domino circuit is quickly sensitive to noise is shown in Fig 1. Once the dynamic node is discharged owing to noise signal, its knowledge can't be recovered. Throughout analysis part dynamic node should be stable. Fig. 2 shows the quality Apodous domino logic with keeper. By adding an associate in Nursing NMOS footer electronic transistor at the supply of the pull down network it becomes footed domino logic circuit (FDL) is shown in Fig 3. FDL minimizes the outpouring current owing to stacking result at the price of speed. For wide fan-in FDL circuit doesn't show a lot of lustiness. Many circuit techniques are

planned within the literature like HS Domino [12], conditional keeper domino circuit [13-15] etc. Main plan relating to these circuit styles to boost circuit performance and noise lustiness.

II. High Speed Domino Logic (Hs Domino)

The schematic of n- input, HS Domino gate is shown in Fig 4. At the beginning of the analysis half, once the clock is switched to high, PMOS monetary resource is ON, thus it turns off the keeper semiconductor device provide. Once the delays for the inverters, the PMOS semiconductor device MP2 is turned off. If the dynamic node is discharged to the ground and collectively the output is high, the NMOS transistor M4 remains off. But if the dynamic node remains high throughout the analysis , then M4 is turned on and pulls down the gate of the keeper semiconductor [transistor |electronic transistor| semiconductor device |semiconductor unit| semiconductor} to low and activates the keeper transistor. However, since the keeper transistor is disabled, the dynamic node is floating at the beginning of the analysis half. If there is noise at the inputs, the analysis node may even be discharged whereas not the keeper. The node is about to be $V_{dd} - V_{t_M4}$, where V_{t_M4} is that the sting voltage of the NMOS electronic transistorM4. So, it finally ends up in associate degree, passing DC current through the PMOS keeper transistor and collectively the NMOS logic tree.

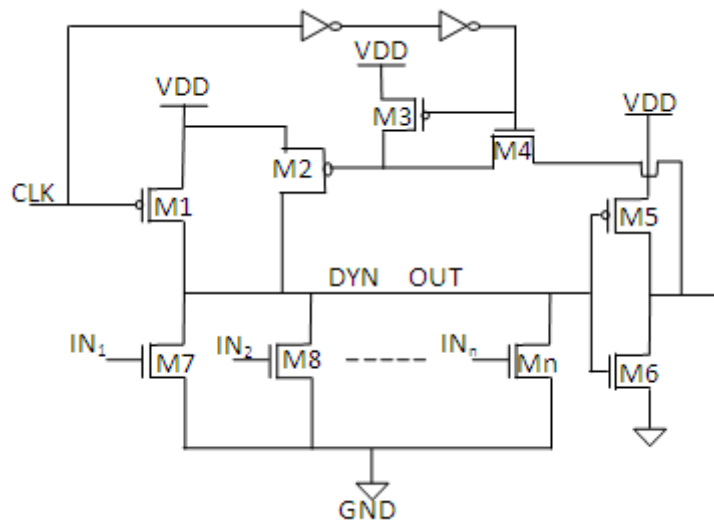


Fig. 4: Wide domino OR gate using HS domino keeper technique.

III. Conditional Keeper Domino Logic (Ckd)

The n-input conditional keeper domino (CKD) logic gate is shown in Fig 5. Wherever we tend to use two keepers, one keeper is weak keeper supply (fixed keeper) and another keeper is powerful keeper supply(conditional keeper). Once the clock is Low then dyamic node charge to VDD. Weak keeper supply isactivate and robust keeper supply is put off. At the beginning of the analysis section (clock low to high) weak keeper activated when a delay of $T_{keeper} = T_{delay\ part} + T_{NAND}$, keeper supply gets activated.Junction transistor supply is conditional keeper, it activates provided that the dynamic node is high. Thus, conditional keeper improves noise immunity of the circuit. Week keeper provides tiny rivalry, current to the pull down network, this improves the speed of the circuit and it's additionally decent to take care of the noise immunity throughout TKeeper. Keeper sizes area unit chosen to specify $W(M0)=W(M2)+W(M3)$. Where $W(M0)$ is that the customary keeper size, $W(M2)$ is that the weak keeper size and $W(M3)$ is that the sturdy keeper size. For prime performance and higher noise immunity, $W(M0)$ is 100 percent of the dimensions of pull down network.

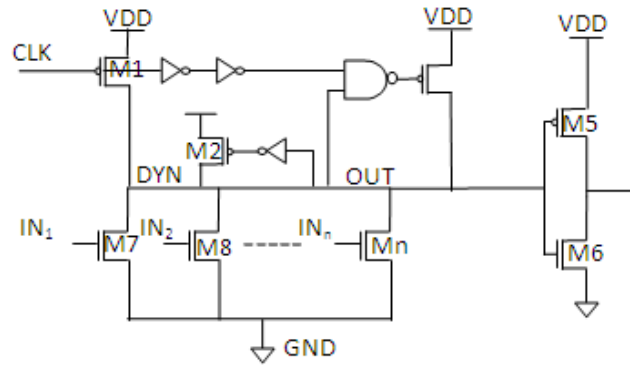
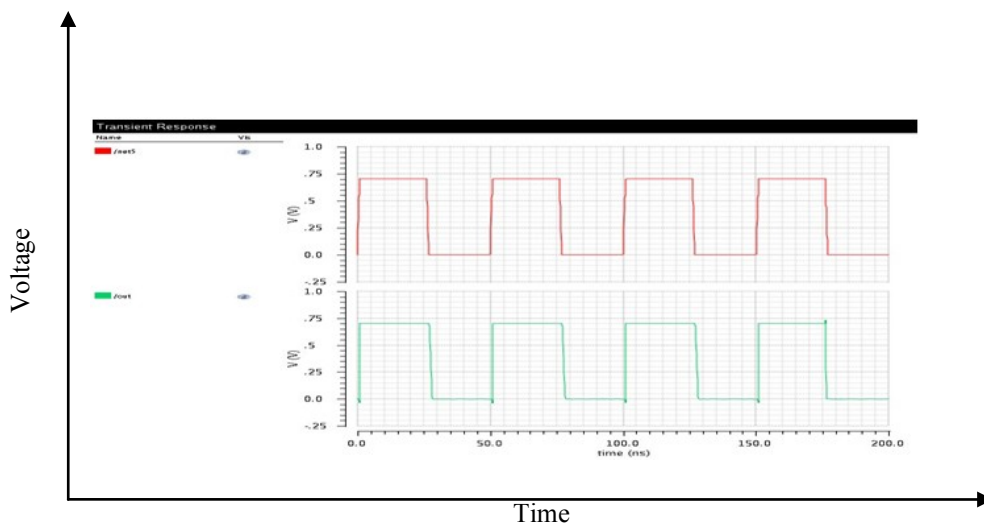


Fig. 5: Wide domino OR gate using conditional keeper technique

IV. Result And Simulation

Transition Response: Domino logic circuit is simulated at operating voltage 0.7 volts (45nm technology).



Power: The Total power consumption value of Fig 6. is observed during simulation of domino logic circuits at 45 nm CMOS technology. The proposed circuit's garbage input/output is accomplished using the virtuoso tool of the cadence IC 6.1 version. Specter simulator of cadence is used for simulation of the output. And the simulations performed victimisation the cadence tool at 45 nm technology. There are 2 main parts that comprise the ability employed by a CMOS integrated circuit. Static power, includes of the ability used once the semiconductor unit isn't within the method of change and it's determined by an easy formula. Power consumption depends on the facility consumed by the semiconductor unit victimisation the operation.

$$P_{\text{static}} = I_{\text{static}} \cdot V_{\text{dd}} \quad (2)$$

Where V_{dd} is termed as supply voltage and I_{static} is identified as the total current flowing through this device.

$$\text{Average Power} \quad P_{\text{avg}} = C \cdot V_{\text{DD}}^2 \cdot f_{\text{CLK}} \quad (3)$$

Where, P_{avg} = Average Power, C = Load Capacitance and F_{clk} = Clock Frequency

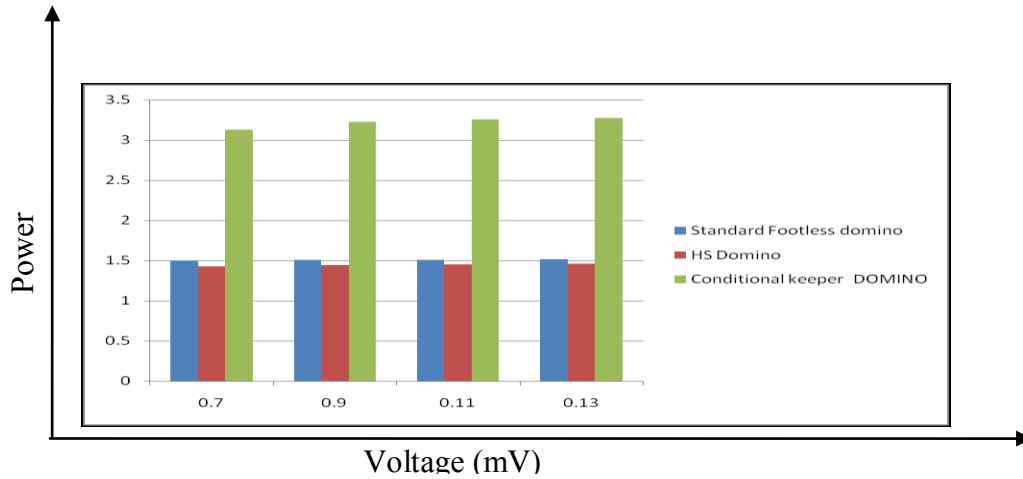


Fig 6 – Simulated result by varies voltage to Active Power

Delay: After the design of logic signal the delay is found to necessary in the every circuit. We need for this design, find out the values of resistor that can introduce that the delay on the signal lines. Delay of the circuit has depended on the value of the resistor itself and as well as the capacitive Load of the circuit. The propagation delay of the RC circuit can be calculated by the Elmore model delay formula as follows.

$$t_p = 0.69 R_{eq} \times C_L \quad (4)$$

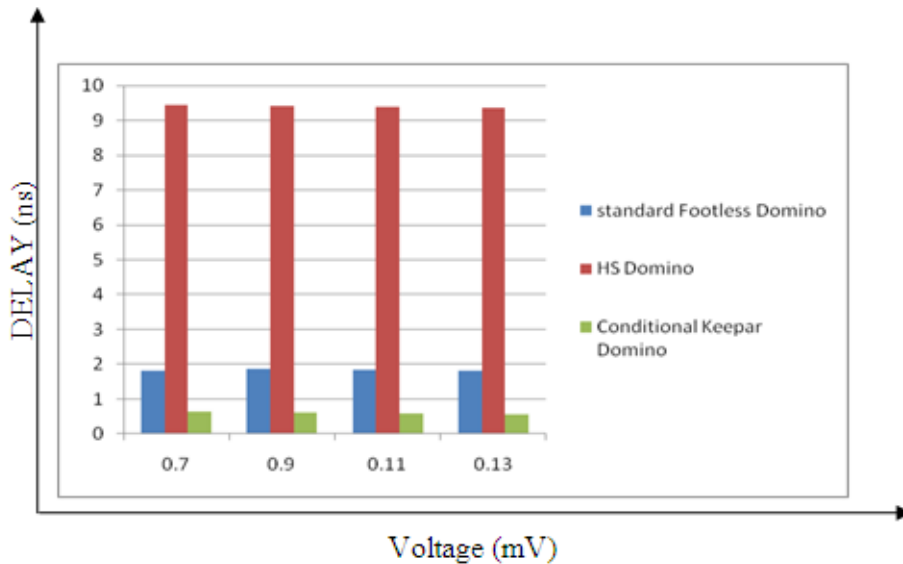


Fig7. Delay Vs Voltage

Power Delay Product:-

Power delay Product is independent of switching frequency and can be calculated

$$PDP = P \times t_d = 0.69 V_{DD} \times \Delta V \times C \quad (5)$$

Where, PDP = Power delay product. P = power, t_d = Delay time

Whereas power delay product is the product of leakage power and delay.

$$PDP = \text{Power} \times \text{Delay} \quad (6)$$

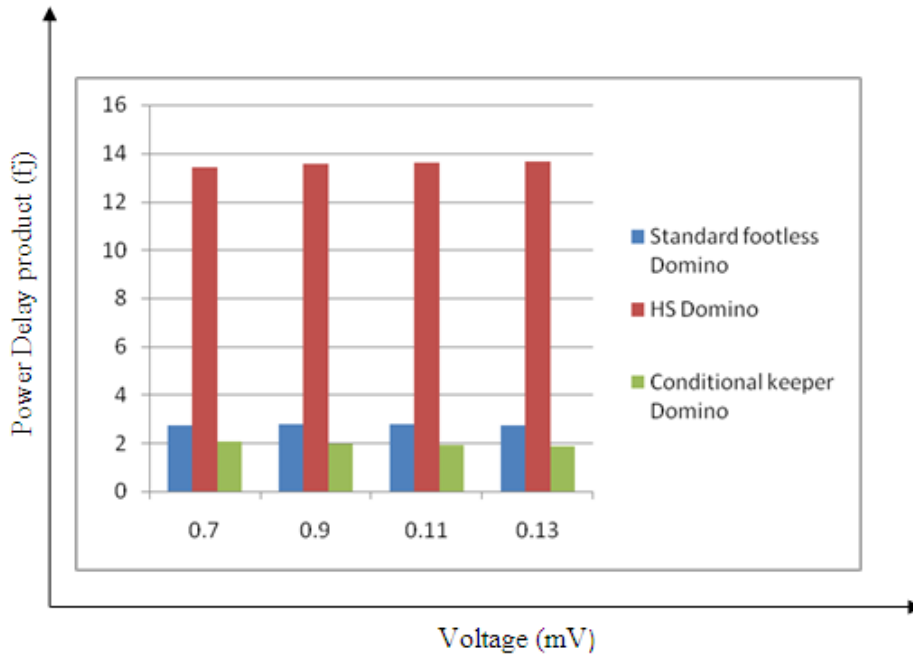


Fig 8. Power Delay Product Vs Voltage

Table 1: Delay, power, and PDP Of the various existing circuits based on 8 input OR Gate

Domino circuits	45 nm technology		
	Power(μ w)	Delay(ns)	PDP(fJ)
Standard footless	1.496	1.816	2.716
HS Domino	1.424	9.434	13.434
Conditional keeper	3.125	0.652	2.037

V. Conclusion

In this paper, totally different topology of four new circuits is planned. Three circuits are predated and one circuit is footless. The most plan by victimisation these techniques to supply little potential at the supply of pull down network, this offer negative gate to supply voltage and increase the hardness of the circuits. Existing and planned circuits is simulated in 45nm victimisation cadence tool for wide fan-in eight input gate circuit. The Planned circuit has higher delay, PDP and standby power as compared to alternative topologies. Therefore, planned circuit is superior vogue, notably for wide fan-in gates high speed domino logic circuit is presented throughout this paper. Simulated results show necessary improvement in leak tolerance and acceptable speed for prime speed applications. Mean whereas we've got a bent to used minimum size for keeper transistor and in addition smaller size for the analysis network. Therefore, the power consumption and house were weakened at a similar time in our planned circuit. During this paper, many domino logic circuit topologies were planned for high-speed style. Conditional keeper domino (CKD) methodology has the most effective performance among others. CKD has a speed improvement of 9% as compared to HS Domino and noise immunity also increases. CKD method can be used for very high speed circuit.

References

- [1]. Roy, K., S. Mukhopadhyay and H. Mahmoodi, 2002. Leakage current in deep-submicron CMOS circuits, Journal of Circuits, Syst. Comput, 11(6): 575-600.
- [2]. De, V. and S. Borkar, 1999. Technology and design challenges for low power and high performance, in Proc. Int. Symp. Low Power Electronics and Design, pp: 163-168.
- [3]. Anders, M., R. Krishnamurthy, R. Spotten and K. Soumyanath, 2001. Robustness of sub-70nm dynamic circuits: Analytical techniques and scaling trends, in Proc. Symp. VLSI Circuit, pp: 23-24.
- [4]. Wairya, S., R.K. Nagaria and S. Tiwari, 2012. Performance analysis of high speed hybrid CMOS full adder circuits for low voltage VLSI design, full adder circuits for low voltage VLSI design.
- [5]. Kao, J.T. and A.P. Chandrakasan, 2000. Dual-threshold voltage techniques for low power digital circuits, IEEE Journal of Solid-State Circuits, 35(7): 1009-1018.
- [6]. Kursun, V. and E.G. Friedman, 2004. Sleep switch dual threshold voltage domino logic with reduced standby leakage current, IEEE Transaction on Very Large Scale Integr. (VLSI) Syst. 12(12): 1311-1319.
- [7]. Liu, Z. and V. Kursun, 2007. PMOS-only sleep switch dual-threshold voltage domino logic in sub-65-nm CMOS technologies, IEEE Transaction on Very Large Scale Integr. (VLSI) Syst. 15(12): 1311-1319.
- [8]. Liu, Z. and V. Kursun, 2006. Leakage power characteristics of dynamic circuits in nanometer CMOS technologies, IEEE Transaction on Circuits CMOS technologies, IEEE Transaction on Circuits.

- [9]. Anis, M.H., M.W. Allam and M.I. Elmasry, 2002. Energy-efficient noise-tolerant dynamic styles for scaled-down CMOS and MTCMOS technologies, *IEEE Transaction on Very Large Scale Integration (VLSI) Systems*, 10: 71-78.
- [10]. Alvandpour, A., K. Krishnamurthy and Sourrty S.Y. Borkar, 2002. A sub-130nm conditional-keeper technique, *IEEE Transaction on Journal of Solid State Circuits*, 37: 633-638.
- [11]. M. Alioto, G. Palumbo, and M. Pennisi, "Understanding the effect of process variations on the delay of static and domino logic," *IEEE Trans. Very Large Scale (VLSI) Syst.*, vol. 18, no. 5, pp. 697-710, May 2010.
- [12]. R. G. David Jeyasingh, N. Bhat, and B. Amrutur, "Adaptive keeper design for dynamic logic circuits using rate sensing technique," *IEEE Trans. Very Large Scale (VLSI) Syst.*, vol. 19, no. 2, pp. 295-304, Feb. 2011.
- [13]. H. Mostafa, M. Anis, and M. Elmasry, "Novel timing yield improvement circuits for high-performance low-power wide fan-in dynamic OR gates," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 10, pp. 1785-1797, Aug. 2011
- [14]. V. Kursun and E. G. Friedman, "Domino logic with variable threshold voltage keeper," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 11, no. 6, pp. 1080-1093, Dec. 2003
- [15]. A. Alvandpour, R. K. Krishnamurthy, K. Soumayanath, and S. Y. Borkar, "A sub-130-nm conditional keeper technique," in *Proc IEEE Int. Conf. Electron. Circuit Syst.*, 1999, pp. 209-212.