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Modelling and Simulation of a SAR ADC with Internally Generated Conversion Signal

T. Vimal Prakash Singh
Department of Electrical Engineering,NERIST,Nirjuli,Arunachal Pradesh,India

Abstract: *This paper presents the modeling and simulation of a 833.33 kS/s, 51.279µW successive approximation register(SAR) Analog to Digital Converter(ADC) using 0.18µm CMOS technology that uses internally generated signal for approximation for low power applications. The ADC is powered by single supply voltage of 1V. In our scheme, comparator output time and bit settling time of the Digital to Analog Converter(DAC) are utilized to generate a signal level such that the next step of the conversion can take place. This model is significant for Globally Asynchronous Locally Synchronous(GALS) system integration.*
Keywords: *Globally Asynchronous Locally Synchronous (GALS), Asynchronous ADC.*

I. Introduction

Analog to Digital Converters (ADC) are used to interface the analog domain with digital domain in order to take the advantage of the high-speed digital Signal Processing (DSP) algorithms in variety of applications. In Systems on Chip(SOC), large number of ADCs are used for interfacing purpose. And in such systems, power consumption is one of the prime concern in order to increase the battery life [1],[2],[3],[4]. And perhaps for reduced power density in the chip. ADCs are the prime component in these system. SAR ADC is widely used for medium resolution because of its low power consumption and high speed [5],[6],[7].

However capacitive Digital to Analog Converter (DAC) used in a SAR ADC increases exponentially as the number of bit increases. And it affects the speed of conversion. The choice of the unit capacitance also depends on the thermal noise and capacitor mismatch.

In a conventional synchronous SAR ADC, for a 8 bit SAR ADC 8 clock cycles are required to complete the conversion. Clock cycle time is determined by considering charge distribution time of the DAC and comparator response time. And clock cycle period is uniformly kept looking at the worst case time of all the blocks of a SAR ADC. Due to requirement of such a high speed clock, power consumption is high and conversion time is also fixed.

This paper proposes a technique to implement a SAR ADC that does not use a global clock for the conversion steps. A self timing like strategy using DAC settling time and comparison settling time of the comparator is used to implement the asynchronous ADC. In our model, settling times of DAC and Comparator are determined and a signal level is generated for the conversion steps.

II. Architecture Design

The architecture of the proposed ADC is shown in Figure 1. It consists of a comparator, and Sample and Hold (S/H), binary weighted switched capacitor DAC , SAR logic and conversion signal generator.

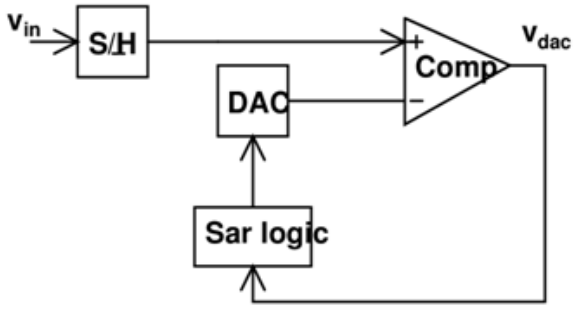

Figure 1: ADC Block Diagram

(A) Sampled and Hold Circuit: In order to reduce the non-linearity introduced due to the V_{GS} of the sample switch NMOS M_S, we use a bootstrapped sample and hold circuit as shown in the Figure 2. Initially the capacitor C_G is charged to Vdd and in the track phase a constant voltage of V_{DD} is applied across V_{GS} of the

sample NMOS M_S. Charge in C_G is also replenished in every phase of sample/track and hold with appropriate signals. Sample/track and Hold transient simulation is shown in Figure 3.

(B) Design of Comparator: Comparator is a main module in a SAR ADC design. Comparator circuit which is used in our implementation is shown in Figure 4. It should be able to detect the difference of two LSBs and it is also to be noted here that in our architecture sampled input is compared with the DAC output voltage. Therefore the sampled input noise is also considered in our design and implementation. In order to verify the working of the comparator, we applied an input reference voltage of 500mV at one of the comparator input and a square wave input voltage from 499.97mV to 500.03mV was swept at the other input and transient analysis was performed. Transient response was plotted in the Figure 5. In the plot, $V_{convsig}$ is the signal to enable comparator and V_{outnr} and V_{outmr} are the comparator outputs.

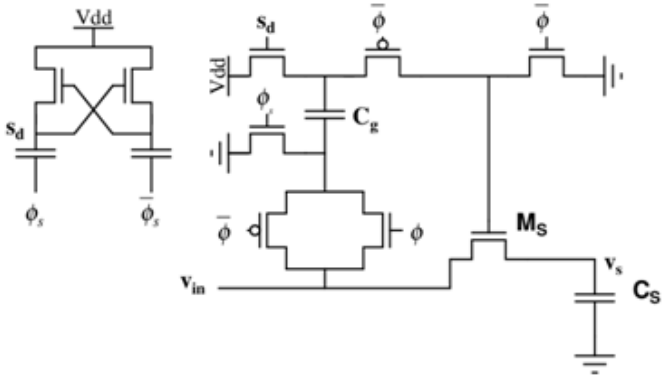

Figure 2: Sample/Track and Hold Circuit

(C) Design of DAC: In our designed DAC, we use a simple binary weighted capacitor array shown in the Figure 4. instead of split capacitor array. The split capacitor array DAC is prone to capacitor mismatch and parasitic capacitance. The unit capacitor should be as small as possible to reduce the power consumption although it is decided by the thermal noise and capacitor mismatch[7]. The conversion starts with closing the MSB switch initially. When the MSB switch is closed and connected to Vref and remaining capacitors are connected to Gnd, the circuit acts like a voltage divider. The voltage at the DAC output is $V_{dac} = \frac{V_{ref} * C(n-1)}{\sum_{i=0}^{6} C(n-2-i)} + C(0)$. The DAC output

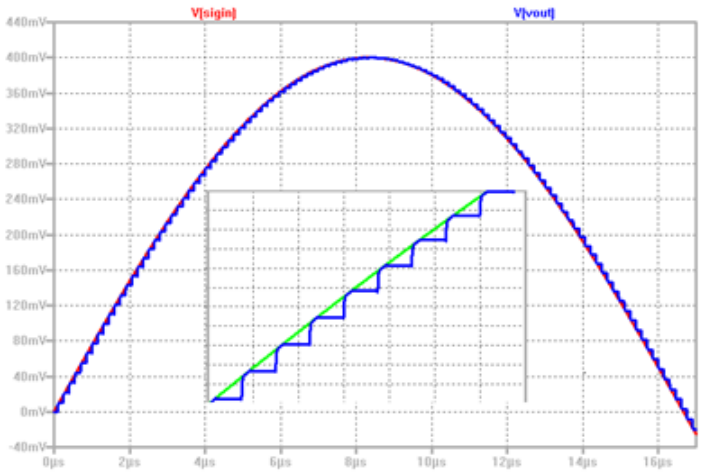

Figure 3: Sample/Hold and Hold Transient Simulation

voltage is compared with the sampled voltage. If the DAC output is less than the sampled input voltage, MSB is set to 1 otherwise the MSB is set to 0. This process of conversion is carried out till LSB bit is determined.

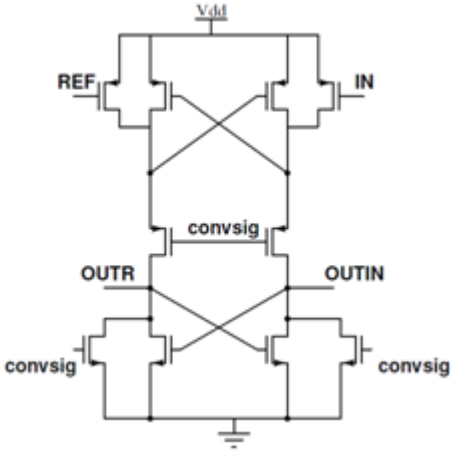

Figure 4: Comparator Circuit

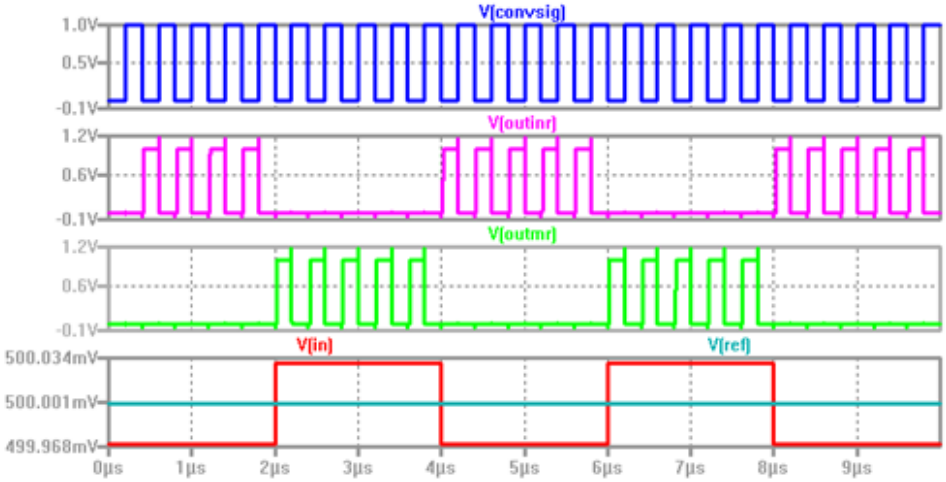

Figure 5: Comparator Transient Simulation

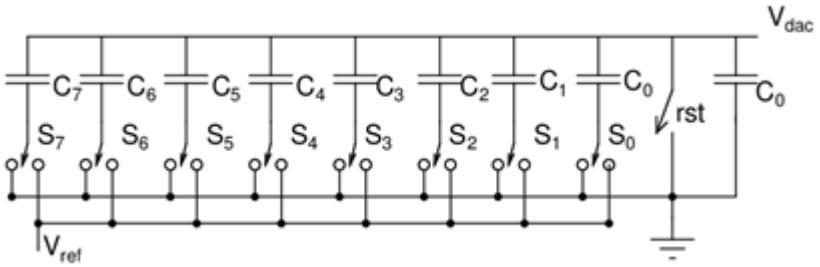

Figure 6: DAC Circuit

Fig. 7 shows simulation results of few comparisons. From bottom to the top, analog input, DAC output voltage which is one of the comparator input, internally generated conversion step signal, comparator output and start of conversion are plotted.

(D) Design of SAR Controller: In a synchronous 8-bit SAR ADC, 8 clock cycles are required for the whole conversion cycle. Clock cycle period is designed considering charge redistribution time, settling time of the DAC and comparator response time. As such clock cycle period is kept uniform considering the worst time of all the three blocks of a SAR ADC.

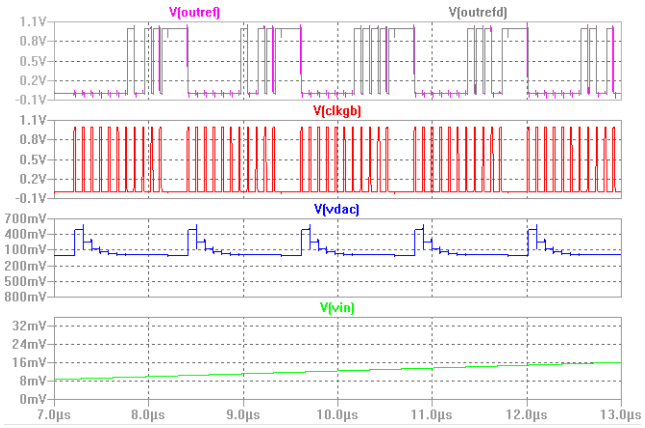

Figure 7: Transient Simulation of DAC

In our designed self timed like SAR ADC, control signal for Successive Approximation is generated internally without global synchronization by considering the variation in the comparator settling time and comparator response time. In a binary weighted capacitor array DAC, settling time for MSB capacitor is longer than that of LSB capacitor. Therefore in order to take advantage of these variation in the settling time of each bit , we propose a completion detection scheme and it is shown in Figure 8. Similarly settling time of the comparator also depends on the comparator input voltage. Comparator settling time completion detection scheme is shown in Figure 9. The process of successive approximation is started with by determining the DAC completion time and comparator completion time. After determining the completion time of both the comparator and DAC, a signal is generated to start the binary approximation. Control signal generation scheme for our proposed SAR ADC implementation is shown in Figure 10 and control signal generation is plotted in Figure 11. In the plot, clkgb is the control signal and V_{aa} is DAC completion signal and V_{bb} is the comparator completion signal.

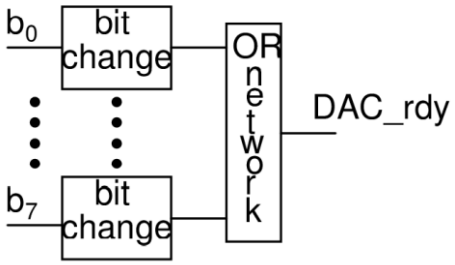

Figure. 8: DAC completion detection scheme

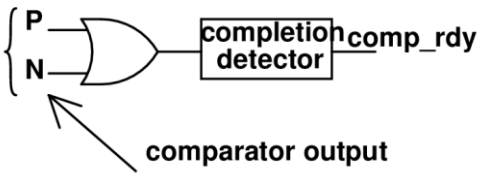

Figure 9. Comparator completion detection scheme

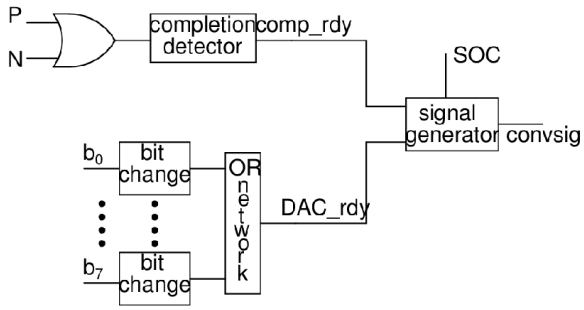

Figure 10: SAR Controller signal generation scheme

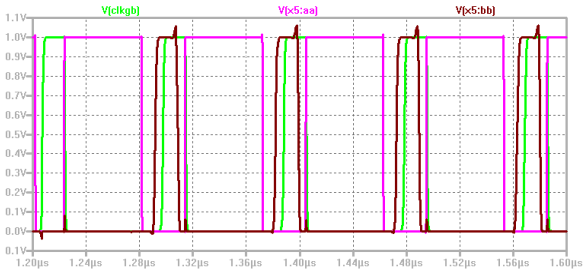

Figure 11: SAR Controller signal generation

III. Simulation Result

Transient simulation of the designed SAR ASC was done with LTSPICE using 180nm CMOS process library and is plotted in the Fig. 12. We apply an input ramp signal having a slope of 0.00125 V/µs and simulation was run for a period of 400µs to cover all the codes.

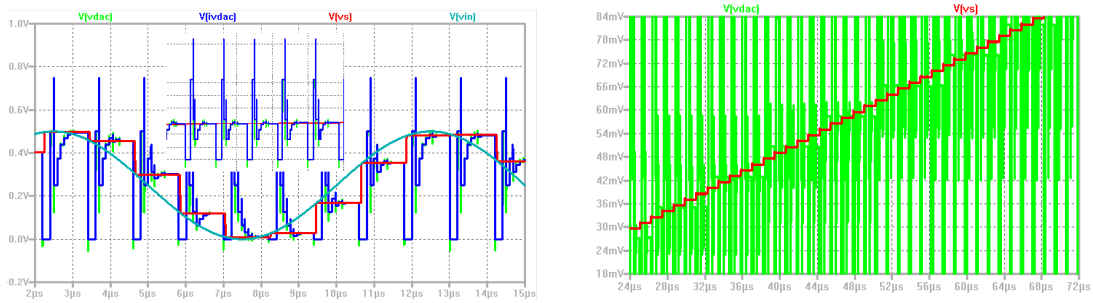

Figure 12: Transient Simulation of ADC

Table 1 summarizes the performance comparison of the proposed work with state of the art ADC available in the literature. Power consumption of the proposed ADC with V_{DD} was simulated and the result is plotted in the Figure 13. The proposed self timed like SAS ADC was able to give correct code at V_{DD} of 0.8V also.

IV. Conclusion

A successive approximation SAR ADC using self timed like strategy without requiring a global clock is modeled and simulated using 180nm standard CMOS Process. Conversion signal was generated internally after completion of the comparator activity and DAC activity. Our self timed like SAR ADC consumes 51.279µW at 833.33 kS/s and V_{DD} of 1 V. Our self - timed like SAR ADC is suitable for low power applications and asynchronous SOC implémentations

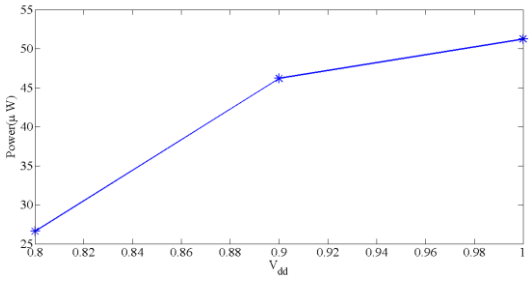

Figure13. Power with V_{dd}

Table 1: Performance comparison

	This work	[3]	[7]	[4]	[1]
Technology(µm)	0.18	0.18	0.13	0.065	0.13
Resolution	8	4	-	10	8
Global Clock	no	yes	yes	no	no
Supply voltage	1V	1V	1V	1V	1V
Sampling rate	833(kS/s)	25(kS/s)	1	25(kS/s)	10.24(MS/s)

Power(µW)	51.34	0.160	0.053	0.281	26.3

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