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Online and Offline Testing Of C-Bist Using Sram

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Abstract: *Built-in self test techniques constitute a class of schemes that provide the capability of performing at-speed testing with high fault coverage hence; they constitute an attractive solution to the problem of testing VLSI devices. Concurrent BIST schemes perform testing during the circuit normal operation without imposing a need to set the circuit offline to perform the test; therefore they can circumvent problems appearing in offline BIST techniques. In this brief, a novel input vector monitoring concurrent BIST architecture has been presented, based on the use of a SRAM-cell like register for storing the information of whether an input vector has appeared or not during normal operation. The evaluation criteria for this class of schemes are the hardware overhead and the CTL, i.e., the time required for the test to complete, while the circuit operates normally. The simulation results shown to be more efficient than previously proposed Concurrent BIST techniques in terms of hardware overhead and CTL.*

I. Existing System

The system has been developed with a c-bist architecture which comprises of a modified decoder, in order to generate and compare the input vectors. These schemes are evaluated based on the hardware overhead and the concurrent test latency i.e., the time required for the test to complete, whereas the circuit operates normally. In this brief, we present a novel input vector monitoring concurrent BIST scheme, which is based on the idea of monitoring a set of vectors reaching the circuit inputs during normal operation, and the use of a static-RAM like structure to store the relative locations of the vectors that reach the circuit inputs in the examined window; the proposed scheme is shown to perform significantly better than previously proposed schemes with respect to the hardware overhead and CTL tradeoff.

II. Simultaneous Testing

The system is first set into testing mode. The possible test vectors are applied to the CUT and the response is captured in SRAM. During this process the errors are detected. Now the circuit is driven into online mode. When the error is detected based on the hit of vector from the values stored in the SRAM the original output is produced as the output of the circuit. Permanent faults can also be identified by using the memory testing algorithms. Here the CUT is the booth radix4 multiplier. Desired circuits can also be used instead of multiplier.

III. Methodology

This figure 1[4] shows the control unit of the BIST unit. The block is being implemented where there is separate logic for each block.

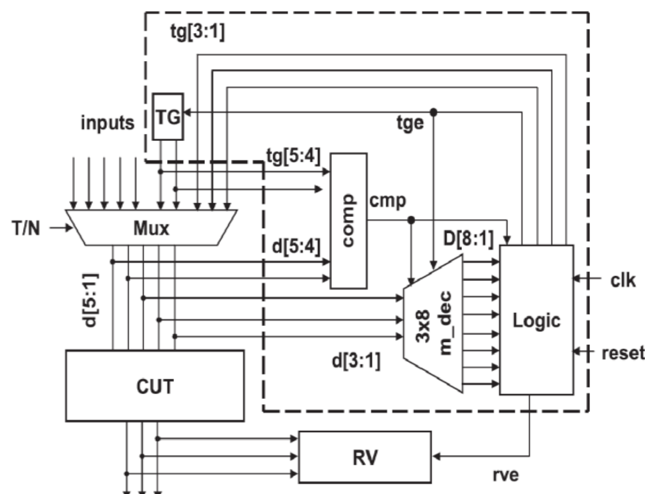


Figure 1 block diagram of BIST

The pattern generator used here is LFSR. The inputs given to the decoder are 2^n in order to produce n outputs. Here the design involves modified decoder structure with the outputs of the comparator and test pattern generator. The modified decoder figure- 2[4] is shown below. When the tge input is given as high then all the outputs of the decoder is high. When the cmp signal is high all the outputs of the decoder are low.

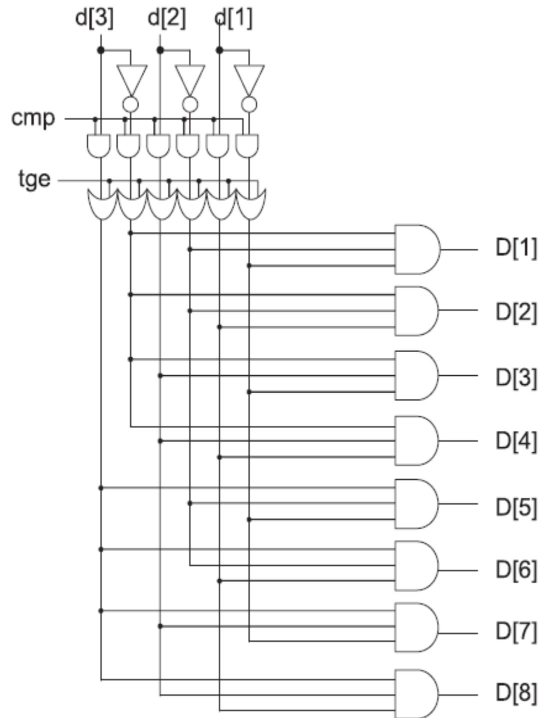


Figure 2 modified decoder

IV. Circuit Under Test Mode

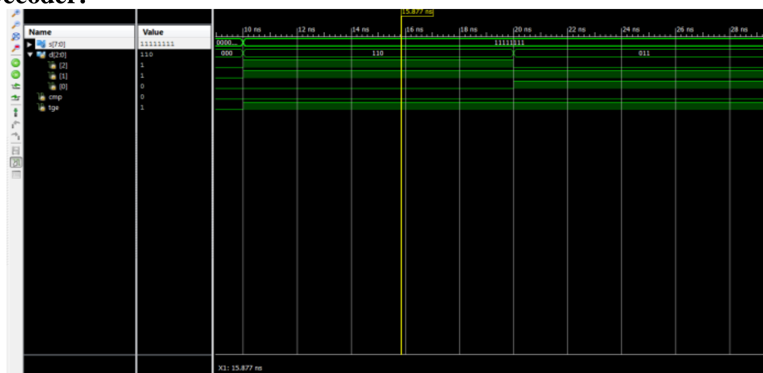
The mode is set to high such that the circuit is under test mode. The possible test patterns are applied to the circuit. For each respective input the response is captured. The errors are detected during this mode. Thus the hit of vector is identified.

V. Circuit Online

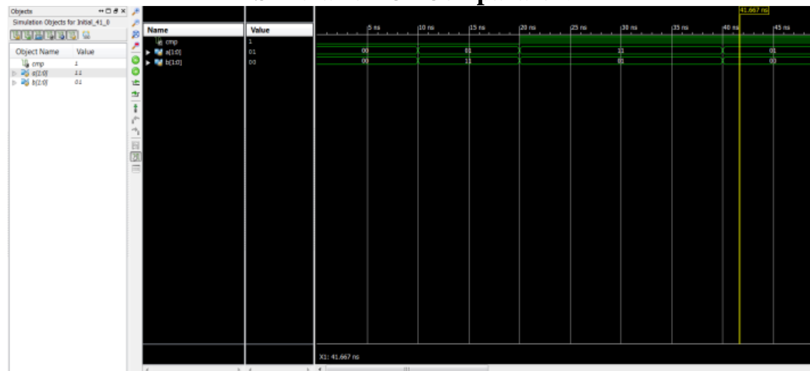
The circuit is now driven into online mode. The normal function of the circuit is carried out without imposing the circuit to be in offline mode again. If the error occurs at the circuit for the given input then the expected output is produced as the output of the circuit instead of the error by retrieving the value from the SRAM register. Comparison has been made on the basis of hardware overhead and CTL. XLINX 13.1 can be used to estimate the no. of LUT of the SPARTAN family FPGA, QUARTUS can be used to estimate the no. of logical elements and timing analysis of ALTERA family FPGA.

VI. Result And Analysis

Simulation Of Decoder:

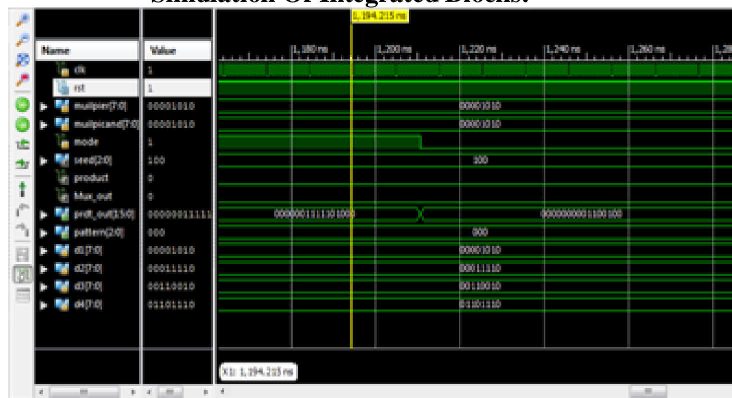


Simulation Of Comparator:



Simulation Of Multiplexer:

Simulation Of Integrated Blocks:



Multiplicand=00001010; Multiplier=00001010;
If mode=1 then circuit is under test (error detected)
If mode=0 then circuit is online (value is loaded from SRAM)

Comparison:

	With SRAM	Without SRAM
hardware overhead	43	94
CTL	0.9ns	4.7ns

VII. Conclusion

Thus an attractive solution to the problem of testing VLSI devices as been modelled. Input vector monitoring concurrent BIST schemes perform testing during the circuit normal operation without imposing a need to set the circuit offline to perform the test. The hardware overhead of the proposed scheme is calculated using the logical elements as a metric. C-BIST was the first input vector monitoring concurrent BIST technique proposed, and suffers from long CTL; therefore modifications have been proposed, Multiple Hardware Sig-

nature Analysis Technique (MHSAT) , Order Independent Signature Analysis Technique (OISAT) , RAM-based Concurrent BIST (R-CBIST) , Window-Monitoring Concurrent BIST (w-MCBIST) , and Square Windows Monitoring Concurrent BIST (SWIM).This architecture has been presented, based on the use of a SRAM-cell like structure for storing the information of whether an input vector has appeared or not during normal operation. The proposed scheme is shown to be more efficient than previously proposed input vector monitoring concurrent BIST techniques in terms of hardware overhead and CTL.

Similarly this technique can be compared with the other techniques mentioned above and spectral analysis using FFT can be carried by giving the spectrum as the input to the circuit.

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