IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 5, Issue 2, Ver. I (Mar. - Apr. 2015), PP 10-19
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

HDL Implementation and Performance Comparison of an Optimized High Speed Multiplier

Arati Sahu[1,] Siba Kumar Panda[2,] SwarnaPrabha Jena[3,]
M. *Tech Scholar, Dept. of ECE*
Centurion University of Technology and Management, Bhubaneswar, Odisha,India Assistant Professor, Dept. of ECE
[2,3,] *Centurion University of Technology and Management, Bhubaneswar, Odisha,IndiaAssistant Professor, Dept. of ECE*

***Abstract**: This paper is devoted for the design of an optimized high speed Vedic multiplier using Udhava-Tiryakbhyam sutra. High speed multiplier is required to perform critical multiplication operation of Digital Signal processing applications like DFT,FFT, convolution , Arithmetic and logic unit(ALU) and Multiply and Accumulate(MAC). This paper shows the Multiplier architecture for 2×2, 4×4,8×8 and 16×16 .The performance has been evaluated in XILINX ISE 9.2.Synthesis and simulation have been performed for various architectures considering delay, number of slices, power and area.*
***Keywords:** Vedic Mathematics, Vedic multiplier, Udhava- Tiryakbhyam, Array multiplier, Booth Algorithm, Digital Signal Processing, VLSI Signal processing, Verilog*.

I. Introduction

Multiplication plays a vital role in arithmetic operation. Multiplication-based operations such as Multiply and Accumulate(MAC) and inner product are among some of the frequently used Computation-Intensive Arithmetic Functions(CIAF) currently implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform(FFT), filtering and in microprocessors in its arithmetic and logic unit. High speed multiplier is required to perform multiplication in Digital signal processing and its application like convolution, DFT, FFT etc. The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. In many DSP algorithms, the multiplier lies in the critical delay path and ultimately determines the performance of algorithm. The speed of multiplication operation is of great importance in DSP as well as in general processor. Multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the time delay and power consumption are very essential requirements for many applications. Multiplier based on Vedic Mathematics is one of the fast and low power multiplier**.**

Vedic mathematics is a part of four Vedas which covers description of several modern mathematical terms including arithmetic, geometry, trigonometry, quadratic equations, factorization and also calculus. Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja(1884-1960),[12] reintroduced after research in Artharva Veda. The word 'Vedic' comes from the word 'Veda' which means the book of wisdom. Vedic mathematics consists 16 sutras and 13 Upa sutras dealing with various branches of mathematics.

II. Background And Related Work

Manoranjan Pradhan, Rutuparna Panda and Sushanta Ku Sahu [1], proposed Vedic multiplier architecture shows speed improvements over a multiplier architecture presented in [2]. The 16×16 Vedic multiplier using 'Nikhilam' sutra found to be better than 16×16 Vedic multiplier using 'Urdhva Tiryakbhyam' sutra in terms of speed when magnitude of both operands are more than half of their maximum values. Amrita Nanda and Shreetam Behera [4], proposed a highly efficient method of multiplication, "Urdhav- Tiryakbhyam sutra" based on Vedic mathematics. Urdhva-Tiryakbhyam sutra is being implemented because this sutra is applicable to all cases of algorithm for N×N bit numbers and the minimum delay is obtained.

Poornima M, et al. [5], proposes the design of high speed Vedic Multiplier using the techniques of Vedic Mathematics that have been modified to improve performance. A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. This paper presents study on high speed 8x8 bit Vedic multiplier architecture which is quite different from the Conventional method of multiplication like add and shift.

Premananda et al. [6], designed the speed of the multipliers is limited by the speed of the adders used for partial product addition. In this paper, they proposed an 8-bit multiplier using a Vedic Mathematics (Urdhva Tiryagbhyam sutra) for generating the partial products. The partial product addition in Vedic multiplier is realized using carry-skip technique. An 8-bit multiplier is realized using a 4-bit multiplier and modified ripple carry adders. In the proposed design we have reduced the number of logic levels, thus reducing the logic delay.

G.Ganesh Kumar et al [7], have been implemented 32x32 bits Vedic multiplier on Spartan XC3S500-5-FG320. The design is based on Vedic method of multiplication. The worst case propagation delay in the Optimized Vedic multiplier case is 31.526ns. It is therefore seen that the Vedic multipliers are much morefaster than the conventional multipliers. This gives us method for hierarchical multiplier design. So the design complexity gets reduced for inputs of large no of bits and modularity gets increased.

B.Ratna Raju, D.V. Satish [8], proposed a high speed 16×16 multiplier based on Urdhva Tiryakbhyam sutra. A novel complex number multiplier design based on Vedic mathematics, highly suitable for high speed complex arithmetic circuits which are having wide application in VLSI and signal processing. The delay of the proposed multiplier is 6.21ns and the power consumption is 0.027mW. The advantages of this model are efficient in speed and area.

'Urdhva Tiryagbhyam' is a broad-spectrum multiplication method of vedic mathematics applicable to all suitcases of multiplications. Siba Kumar Panda, R.Das et.al [10] used this algorithm to design vedic multipliers in VHDL environment. The advantage of this algorithm [2]is that partial products and their sums are calculated in parallel.

III. Proposed Scheme Of Design

(i) Urdhva Tiryakbhyam Method:

The "Urdhva- Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. „Urdhva and „Tiryagbhyam words are deived from Sanskrit literature. "Urdhva means "Vertically" and "Tiryakbhyam means "crosswise". The multiplier is based on an algorithm Urdhva-Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication.

To explain the multiplication process, let us consider the multiplication of two decimal numbers (325* 738). The multiplication is shows in the figure-1 .

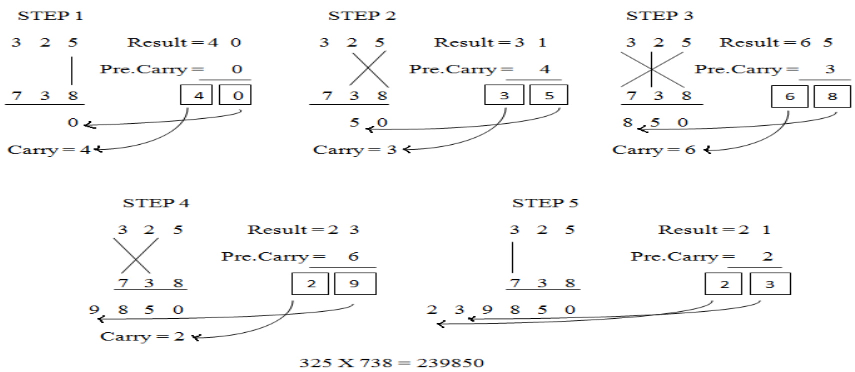

Figure -1: Multiplication of two decimal numbers by Urdhva Tiryakbhyam

The digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and hence the process goes on. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit acts as the result bit and all other bits act as carry for the next step. At the initial stage carry is taken to be zero.

(ii) Multiplication of Two Binary Number:

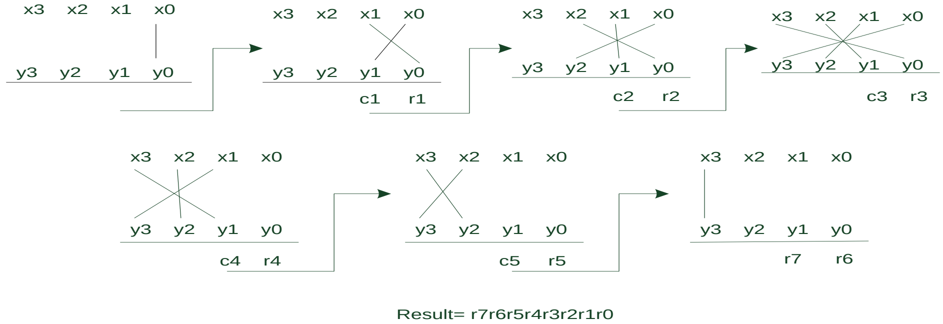

Figure- 2: Multiplication of two binary number using UT Method

To explain the multiplication process, let us consider the multiplication of two binary numbers x3x2x1x0 and y3y2y1y0. The result of this multiplication stored in r7r6r5r4r3r2r1r0. Firstly, the Least significant bits are multiplied and the result is stored in r0. Then in the next step LSB of multiplicand is multiplied with the next higher bit of the multiplier and added with previous carry. The result is stored in r1 and carry is transfer to the next step. Likewise the process goes on till we get the result.

Thus we get the following expression:
r0= x0y0;
c1r1= x1y0+ x0y1;
c2r2= c1+ x2y0+ x1y1+ x0y2;
c3r3= c2+ x3y0+ x2y1+ x1y2+ x0y3;
c4r4= c3+ x3y1+ x2y2+ x1y3;
c5r5= c4+ x3y2+ x2y3;
c6r6=c5+ x3y3;

(iii) 2×2 Vedic Multiplier Using UT Method:

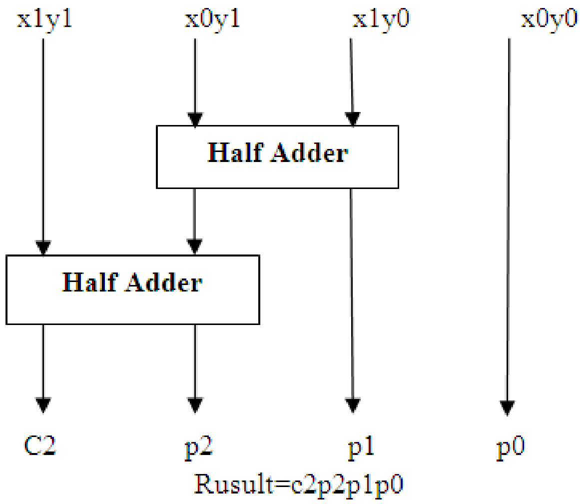

Figure-3: Block diagram of 2×2 Vedic multiplier

The 2×2 bit multiplier is shown in figure-3. The fundamental blocks of this multiplier is one bit multiplier and adders. Let us consider two inputs, each of 2 bits i.e. x1x0 and y1y0. The result is 4 bits i.e. c2p2p1p0. According to basic method of multiplication, result is obtained after getting partial product and doing addition.

```
         x1   x0
       × y1   y0
      --------
        x1y0  x0y0
 x1y1  x0y1
----------------
 c2  p2   p1    p0
```

In Vedic multiplication method, p0 is vertical product of bit x0 and y0, p1 is addition of crosswise bit multiplication i.e. x1 & y0 and x0 and y1, and p2 is again vertical product of bits x1 and y1 with the carry generated, if any, from the previous addition during p1. c2 output is nothing but carry generated during p2 calculation. This module is known as 2x2multiplier.

(iv) 4×4 Vedic multiplier using UT method:

The 4× 4 Vedic multiplier architecture [9] is implemented using four 2×2 Vedic multiplier module and three 4 bit carry save adder stages. The 4×4 Vedic multiplier is structured using 2×2 Vedic multiplier blocks shown in the figure. Let's analyze 4x4 multiplications, say a3a2a1a0 and b3b2b1b0. Following are the output line for the multiplication result, P7P6P5P4P3P2P1P0. The least significant two bits of the first 2×2 Vedic

Multiplier (VM) are directly given the output i.e. P (1-0). The second and third 2×2 VM blocks output is added directly using the first 4 bit carry save (CS) adder. The second 4 bit CS adder is used to add two 4 bit operands i.e. concatenated 4 bit ("00" & most significant two output bits of first 2x2 VM block) & one 4 bit operand we get as the result of first CS adder & the carry 'c' is transferred to third CS adder. Finally, we get a 4 bit result i.e. P (7-4) from the fourth 2×2 VM block and the carry is discarded.

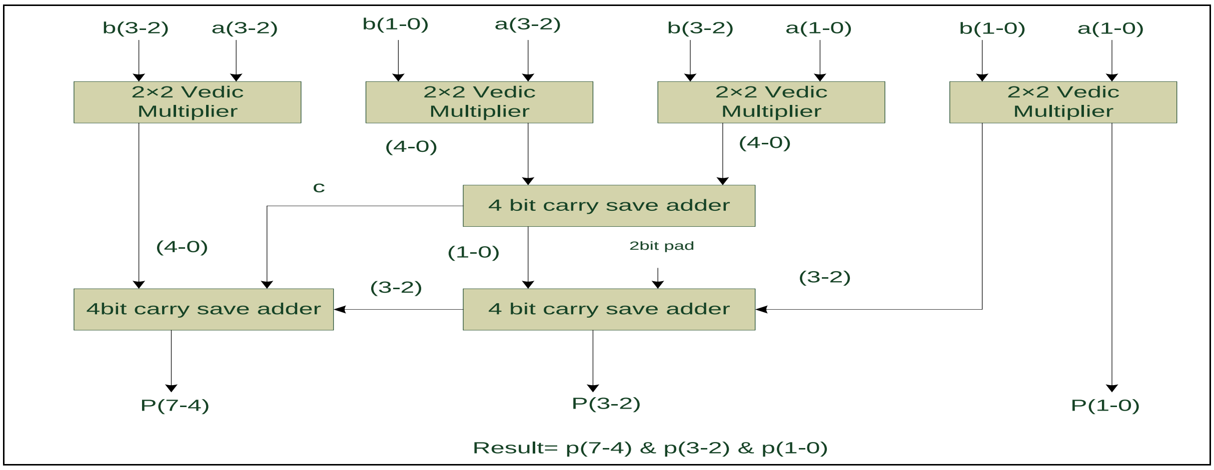

Figure-4: Architecture of 4×4 Vedic Multiplier

(v) 8×8 Vedic Multiplier using UT Method:

The 8× 8 Vedic multiplier architecture is implemented using four 4×4 Vedic multiplier module and three 8 bit carry save adder stages. The 8×8 Vedic multiplier is structured using 4×4 Vedic multiplier blocks shown in the figure.

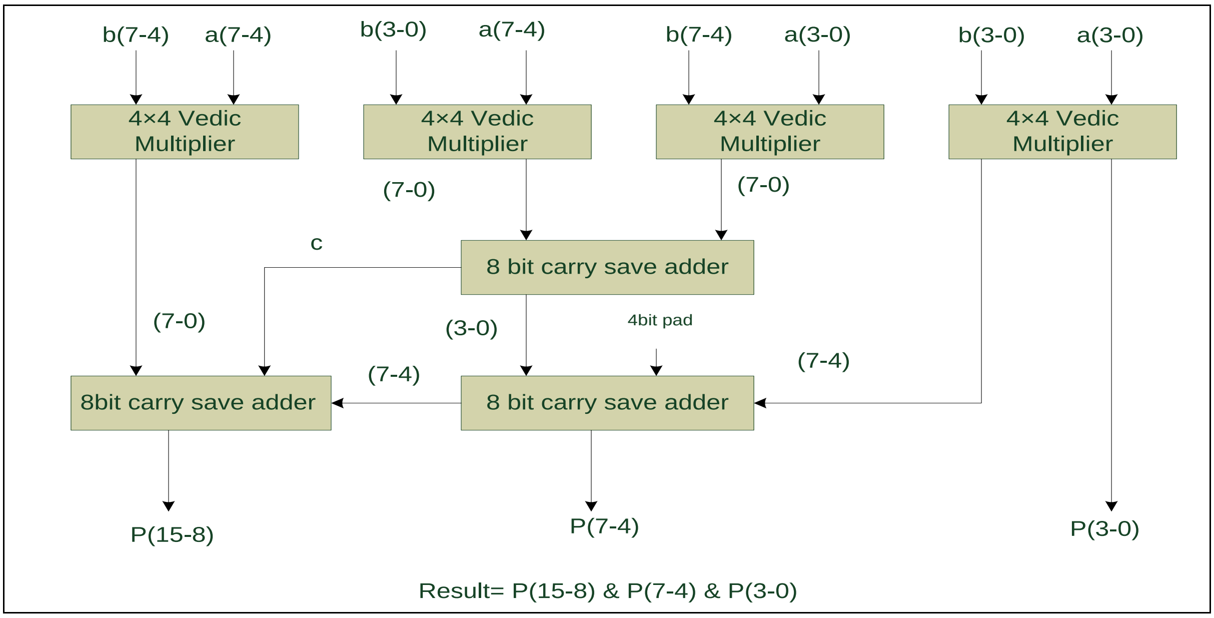

Figure-5: Architecture of 8×8Vedic Multiplier.

Let's analyze 8x8 multiplications, say a (7-0) and b (7-0). Following are the output line for the multiplication result, P (15-0). The least significant two bits of the first 4×4 Vedic Multiplier (VM) are directly given the output i.e. P (3-0). The second and third 4×4 VM blocks output is added directly using the first 8 bit carry save (CS) adder. The second 8 bit CS adder is used to add two 8 bit operands i.e. concatenated 8 bit ("0000" & most significant four output bits of first 4x4VM block) & one 8 bit operand we get as the result of first CS adder & the carry 'c' is transferred to third CS adder. Finally, we get a 8 bit result i.e. P (15-8) from the fourth 4×4 VM block and the carry is discarded.

(vi) 16×16 Vedic Multiplier using UT Method:

The 16×16 Vedic multiplier architecture is implemented using four 8×8 Vedic multiplier module and three 16 bit carry save adder stages. The 16×16 Vedic multiplier is structured using 8×8 Vedic multiplier blocks shown in the figure.

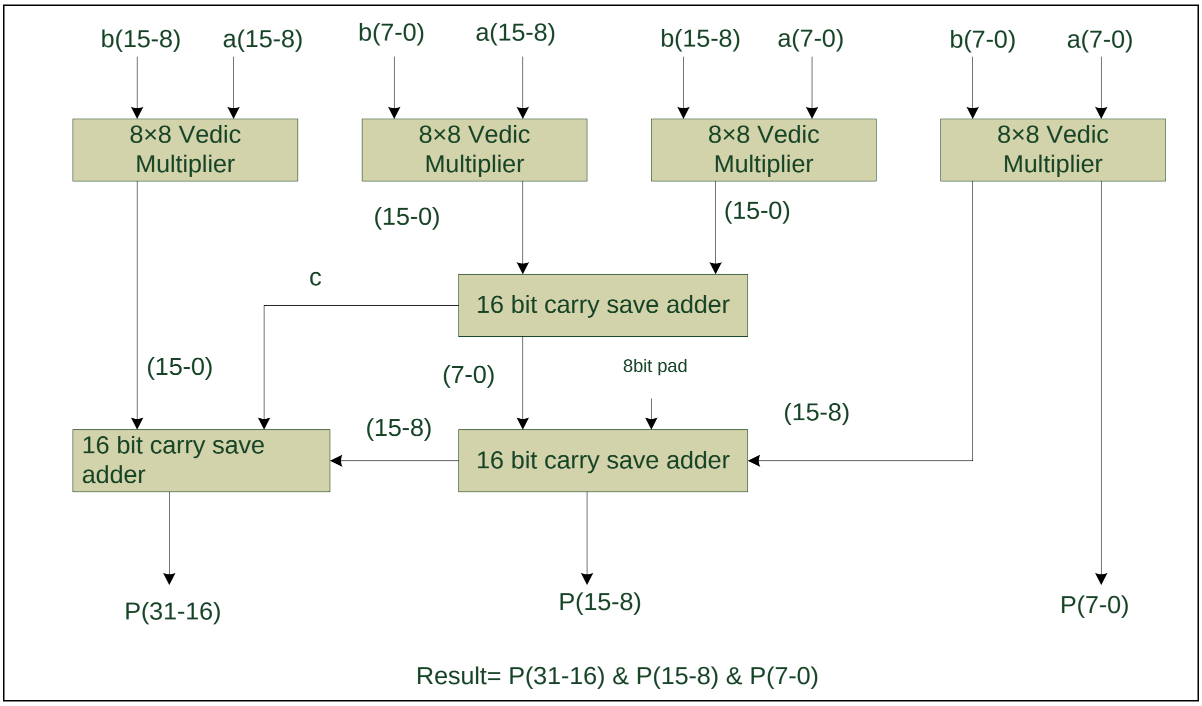

Figure-6: Architecture of 16×16Vedic Multiplier

Let's analyze 16x16 multiplications, say a (15-0) and b (15-0). Following are the output line for the multiplication result, P (31-0). The least significant two bits of the first 8×8 Vedic Multiplier (VM) are directly given the output i.e. P (7-0). The second and third 8×8 VM blocks output is added directly using the first 16 bit carry save (CS) adder. The second 16 bit CS adder is used to add two 16 bit operands i.e. concatenated 16 bit ("00000000" & most significant eight output bits of first 8x8VM block) & one 16 bit operand we get as the result of first CS adder & the carry 'c' is transferred to third CS adder. Finally, we get a 16 bit result i.e. P (31-16) from the fourth 8×8 VM block and the carry is discarded.

IV. Result Analysis

The implementation of Vedic Multiplier is based on a novel technique of digital multiplication which is quite different from the conventional method of multiplication like add and shift. Where smaller blocks are used to design the bigger one. The Vedic Multiplier is designed in Verilog HDL, as its give effective utilization of structural method of modelling. The individual block is implemented using Verilog hardware description language. The functionality of each block is verified using simulation software and Xilinx ISE 9.2i.The simulated result and waveform of 4×4, 8×8 and 16×16 is given below.

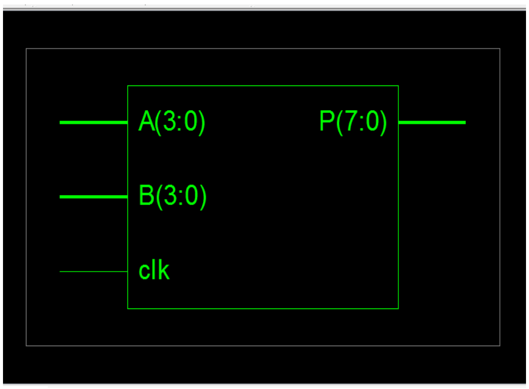

Figure-7: Block view of 4×4 Vedic multiplier

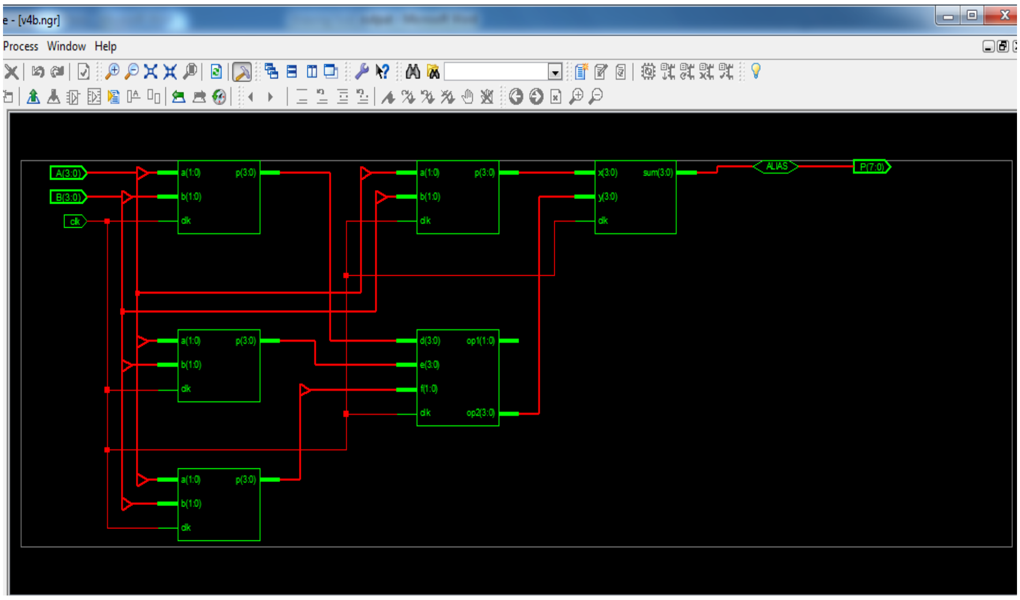

Figure-8: RTL Schematic of 4×4 Vedic multiplier

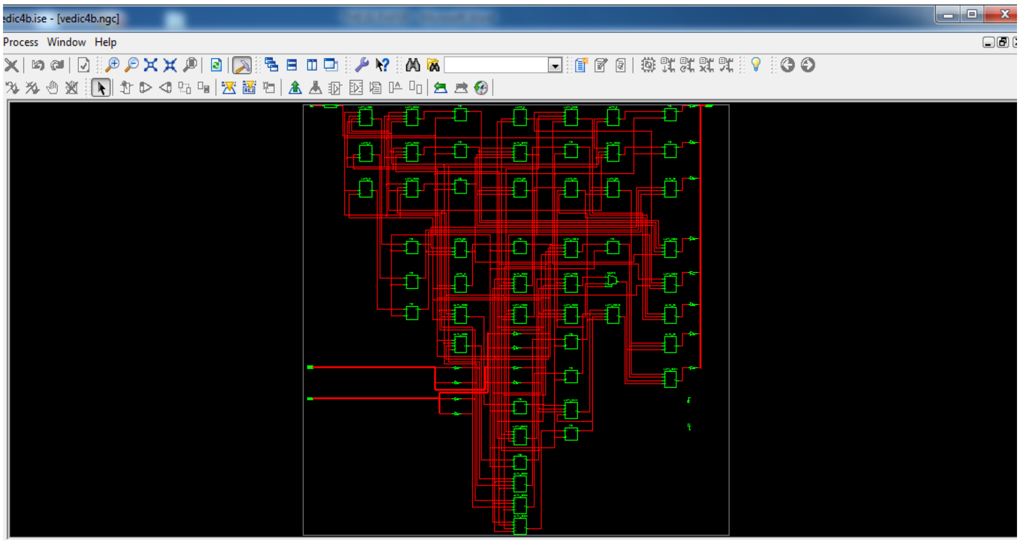

Figure-9: Technology Schematic of 4×4 Vedic Multiplier

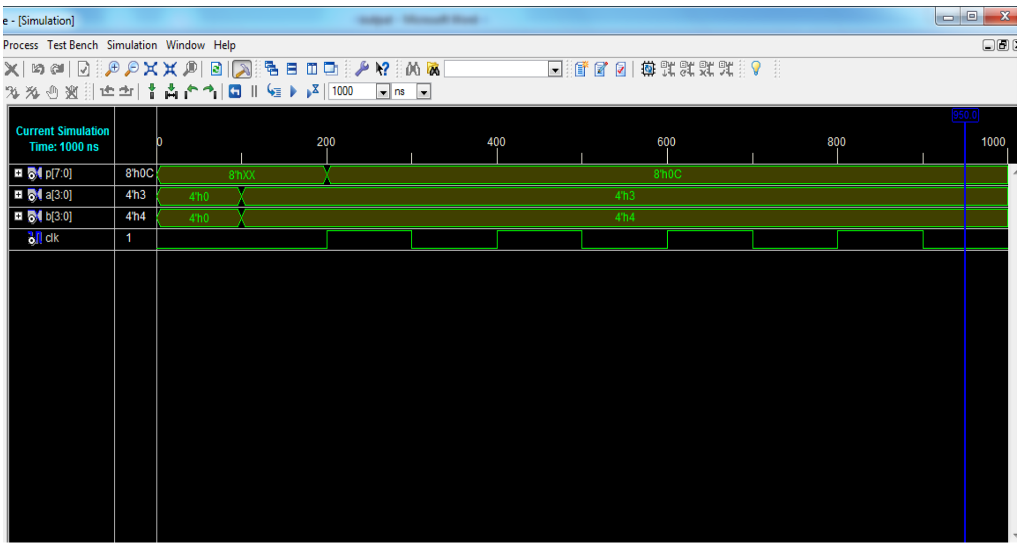

Figure-10: Test Bench Waveform of 4×4 Vedic multiplier

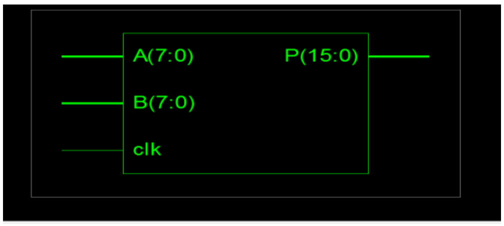

Figure-11: Block view of 8×8 Vedic multiplier

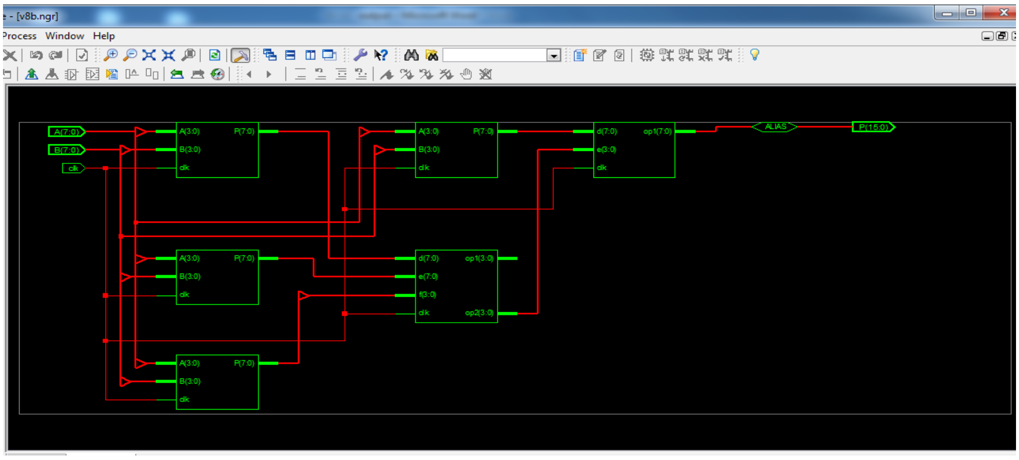

Figure-12: RTL Schematic of 8×8 Vedic multiplier

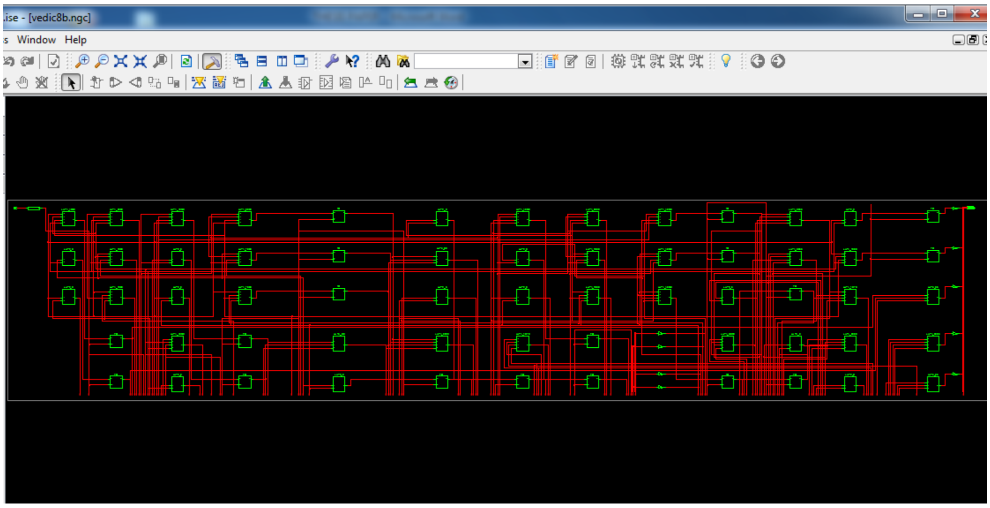

Figure13: Technology Schematic of 8×8 Vedic Multiplier

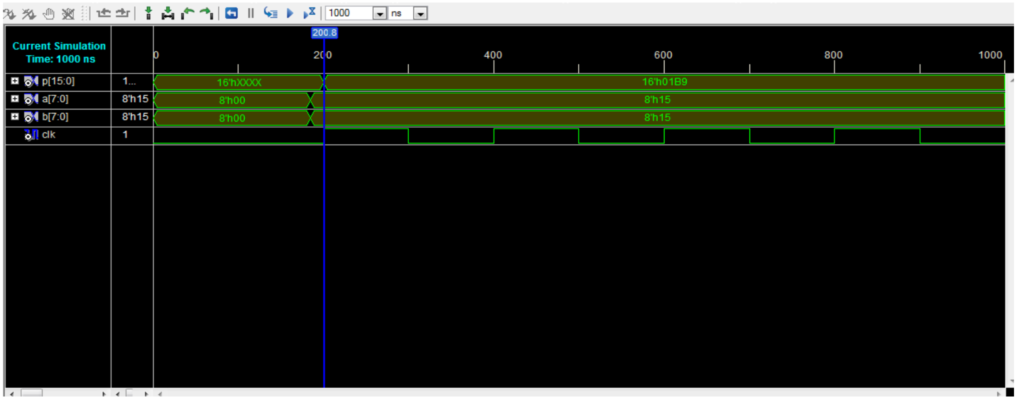

Figure-14: Test Bench Waveform of 8×8 Vedic multiplier

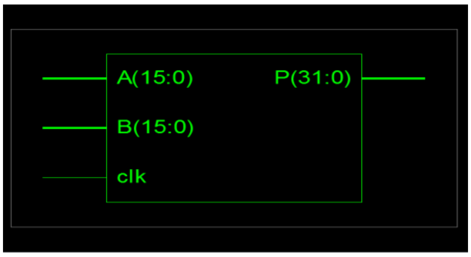

Figure-15: Block View of 16×16 Vedic multiplier

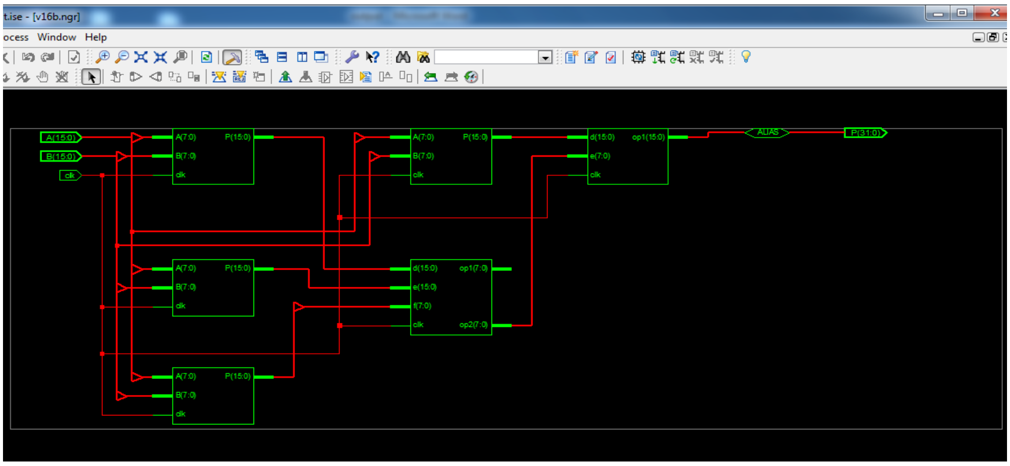

Figure-16: RTL Schematic of 16×16 Vedic multiplier

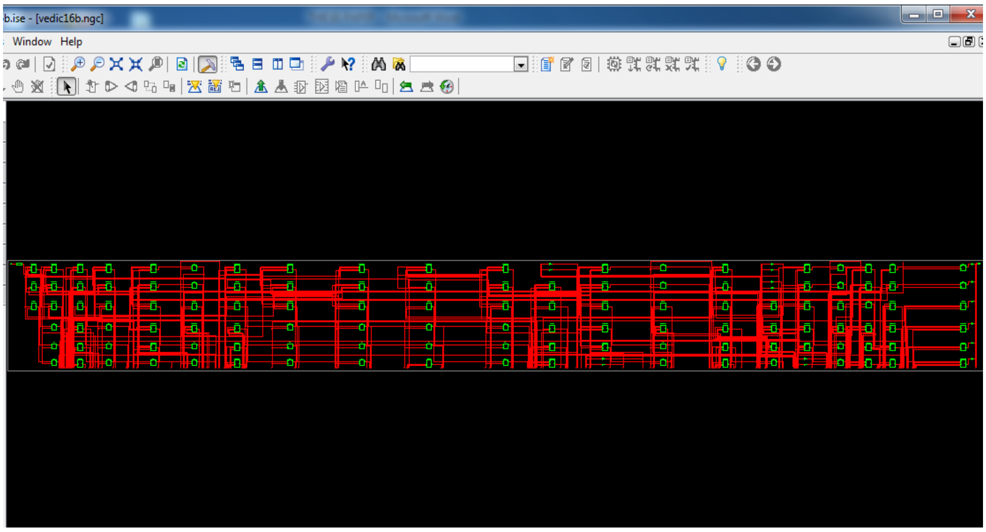

Figure-17: Technology Schematic of 16×16 Vedic Multiplier

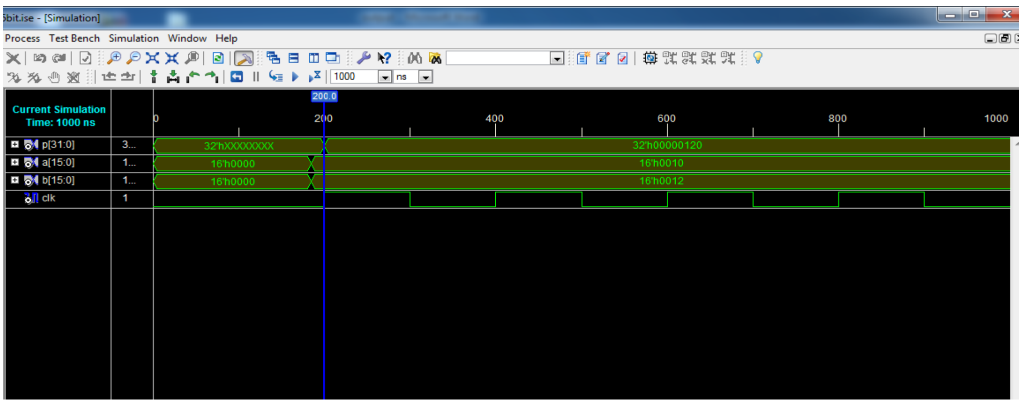

Figure-18: Test Bench Waveform of 16×16 Vedic multiplier

The below Table-1 shows the performance comparison of the proposed scheme of design with the array multiplier and booth multiplier in terms of No of slices, No of 4 input LUT, No of IOs,No of bounded IOBs, Delay and memory. From this performance analysis it reveals that, it is optimized in terms of all the parameters with greater speed.

Multiplier → Parameters ↓	Array Multiplier[13]			Booth Multiplier[12]			UT Proposed Work		
	4×4	8×8	16×16	4×4	8×8	16×16	4×4	8×8	16×16
No of Slices	35 out of 786	71 out of 786	290 out of 786	50 out of 786	96 out of 786	499 out of 786	19 out of 786	62 out of 786	217 out of 786
No of 4 input LUT	64 out of 1536	123 out of 1536	505 out of 1536	90 out of 1536	178 out of 1536	923 out of 1536	35 out of 1536	97 out of 1536	194 out of 1536
No of IOs	17	33	65	17	33	65	17	33	65
No of bounded IOBS	17 out of 124	32 out of 124	64 out of 124	17 out of 124	32 out of124	65 out of 124	17 out of 124	32 out of 124	65 out of124
Delay	15.23ns	32.01 ns	60.92 ns	14.33ns	29.45ns	70.86ns	7.63ns	13.94ns	22.45n
Memory	192684	195752	197544	191464	193354	196849	190144	192244	196848

Table.1- Performance Comparison

V. Conclusion

Our proposed UT based Vedic multiplier architecture shows speed improvements along with less memory size and delay over existing multiplier architecture methodologies like array multiplier and booth Algorithm based multiplier .The 32x32 bit Vedic multiplier along with other lower bit multipliers using Urdhva Tiryakbhyam Sutra found to be the best approach in terms of speed and complexity in the gate level design architecture All the work has been carried out under Xilinx ISE 9.2 i environment showing satisfactory results. In the future works, our proposed scheme can be further implemented for 32bit, 64 bit and 128 bit multipliers and the same can be used in any Digital filter design for echo cancellation, noise cancellation, adaptive equalization processes.

References

[1]. Rutuparna panda,M.pradhan," Speed comparision of 16*16 vedic multipliers" IJCA,vol-21,may-2011

[2]. M.Pradhan, R.Panda, S K Sahu, " MAC Implementation using Vedic Multiplication Algorithm," IJCA (0975-8887), Vol-21, No.7, may 2011.

[3]. M.Pradhan, R.Panda, "Design and Implementation of Vedic Multiplier," A.M.S.E. Journal, vol.15, Issue 2,pp.1-19, July 2010.

[4]. A Nanda, S Behera, "Design and Implementation of Urdhva-Tiryakbhyam Based 8×8 Vedic Binary Multiplier", IJERT, Vol.3,Issue 3, March 2014.

[5]. Poornima M, Shivaraj Kumar Patil, Shivukumar , Shridhar K P , Sanjay H, "Implementation of Multiplier using Vedic Algorithm", International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-2, Issue-6, May 2013.

[6]. Premananda B.S., Samarth S. Pai, Shashank B., Shashank S. Bhat "Design and Implementation of 8-Bit Vedic Multiplier " International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering (An ISO 3297: 2007 Certified Organization) Vol. 2, Issue 12, December 2013.

[7]. G.Ganesh Kumar, V.Charishma "Design of High Speed Vedic Multiplier using Vedic Mathematics techniques ", International Journal of Scientific and Research Publications, Volume 2, Issue 3, March 2012.

[8]. B.Ratan Raju, D.V. Satish, "A High Speed 16×16 Multiplier Based On Udhva Tiryakbhyam Sutra", IJSEAT, Vol.1, Issue 5, October 2013.

[9]. Pushpalata Verma, "Design of 4×4 bit Vedic Multiplier using EDA Tool", International Journal of Computer Applications, Volume 48, June 2012.

[10]. Siba Ku Panda, Ritisnigdha Das et al. "VLSI Implementation of Vedic Multiplier Using Urdhva- Tiryakbhyam Sutra in VHDL Environment: A Novelty", IOSR, Vol.5, February 2015.

[11]. S. Kokila, Ramadhurai. R, L. Sarah, " VHDL Implementation of Fast 32×32 Multiplier based on Vedic Mathematics", International Journal of Engineering Technology and Computer Application, Vol.2, April 2012.

[12]. S. Koushighan, K. Hariharan et al." Design of an Optimized High Speed MultiplierUsing Vedic Mathematics", Contemporary Engineering Sciences, Vol. 7, 2014.

[13]. S. S. Kerur, Prakash Narchi et al." Implementation of Vedic Multiplier for Digital SignalProcessing", IJCA 2011.

[14]. Swami Bharati Tirtha, Vedic Mathematics. Delhi: Motial Banarsidass Publishers, 1965.
[15]. D L Perry, "VHDL: Programming by Example", McGraw-Hill Publications, New Delhi, 2002.

Author Profile

Mrs Arati Sahu was born in Rourkela , Odisha , India, in 1991. She has completed B.Tech in Electronics and Communication Engineering,from Sundargarh Engineering Collage,Sundargarh.Currently pursuing her M.tech degree in VLSI from ECE , Centurion University of Technology and Management, Bhubaneswar, Odisha 751020 ,India, in the academic period of 2013-2015.

Mr. Siba Kumar Panda was born on November 09,1989.He received the B.Tech degree in Electronics & Communication Engineering from Biju Patnaik University of **Technology,odisha in 2012 and M.Tech degree in VLSI Signal Processing Specialization** from Veer Surendra Sai University Of Technology,odisha in 2014. Currently he is working as an Assistant Professor at Centurion University of Technology and Management, Bhubaneswar; Odisha.He also awarded the University Silver medal for best Electronics & Telecommunication Engineering Post Graduate for the academic year 2012-2014 at VSSUT, Odisha. His research area of interest includes Ultra-wideband (UWB) device design, RF circuit design using CMOS Technique,VLSI implementation of Vedic mathematics,VLSI Signal Processing.

Mrs. Swarnaprabha Jena currently working as Assistant Professor in ECE Department, CUTM, Jatani, Odisha.She completed her M.Tech degree in VLSI Design in 2012.Her Research area of interest is VLSI design and Embedded System.