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Power Reduction in CMOS Sub-threshold Dual Mode logic circuits by Power Gating

Celine Elsa Jose[1], B Kousalya[2]
[1](ME VLSI Design, Department of ECE, HIT, Anna University, India)
[2](Department of ECE, HIT, Anna University, India)

Abstract: *Power dissipation has always been a major concern in integrated circuit design. Even during static state, there is a small amount of leakage power. In this project we have implemented various Power gating techniques like Sleep, Dual Sleep and Sleepy Stack in Sub threshold Dual mode logic circuits. This logic can bring down the total power. Hence a comparative analysis of power consumption is performed. The Dual mode logic has two modes of operation namely Static and Dynamic. In Static mode, there is a considerable decrease in the power consumed along with a moderate performance. Dynamic mode renders high performance compromising on an increase in power consumption. Power gating employs sleep transistors to isolate the circuit thereby reducing leakage power. The power is evaluated using Tanner Simulation tool under 180nm technology.*

Keywords: *Complementary MOS, Dual Mode Logic (DML), static power*

I. Introduction

Digital circuit design is one of the main focus areas for low power applications. The supply voltage applied to the circuits operating in the sub-threshold region is equal to or less than the threshold voltages of the transistors, allowing a significant reduction of both dynamic and static power. The most common logic family used for sub-threshold operation is the Complementary Metal Oxide Semiconductor (CMOS).The dual mode logic based NAND, NOR and NOT gates are designed to operate in the sub threshold region. The logic gates can be operated in two modes: static CMOS-like mode and dynamic CMOS-like mode. In the static mode of operation, the DML gates have very low power dissipation with moderate performance. When the DML gate is in the dynamic functional mode, they have much higher performance, at the cost of increased power dissipation. This particular feature of the Dual Mode Logic provides the option to control system performance on-the-fly and hence support applications in which a flexible workload is required. Section II provides an overview of the basic Dual Mode architecture and its method of operation. Section III describes the design of the basic logic gates NAND, NOR & NOT with DML mode. Section IV describes the power gating techniques implemented in the DML circuits.

II. Dual Mode Architecture

The basic DML gate architecture is composed of a standard CMOS gate and an additional transistor M1, whose gate is connected to a global clock signal. At first glance, this architecture is very similar to the noise tolerant precharge (NTP) structure. However, in contrast to the NTP, which was developed as a high-speed, high-noise-tolerance dynamic logic, the DML aims to allow operation in two functional modes: static mode and dynamic mode. To operate the gate in the dynamic mode, the Clk is assigned an asymmetric clock, allowing two distinct phases: precharge and evaluation. During the precharge phase, the output is charged to high/low, depending on the topology of the DML gate.

The basic DML logic gate designed to operate in either static mode of operation or dynamic mode of operation consists: A static gate having one or more logic inputs, a single logic output and a switching element that is associated with the static gate. The switching element comprises of an input that is connected to a constant voltage, and another input for providing a signal used for mode selection, an output that is connected to a logic output of the static gate. Switching the Dual mode logic gates between the two functional modes, static and dynamic, is performed by applying either a constant voltage or a dynamic clock signal at the mode selection input of the switching element.

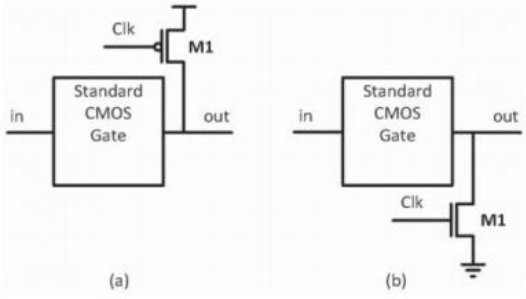

Figure 1: DML Gates

The switching element can be operated in any of the two modes by: i) disconnecting the static gate output from both the input that is connected to a constant voltage, and the other input for providing a signal used for mode selection, when the mode selection signal applies a constant voltage to the input used for providing mode selection signal, thereby selecting static mode of operation ii) Connecting the static gate output to both the input that is connected to a constant voltage, and the other input for providing a signal used for mode selection, when the mode selection signal applies a dynamic clock signal to the input used for providing mode selection signal, thereby to select dynamic mode operation. The design methodology that should be used when designing a DML gate is to place the precharge transistor in parallel to the stacked transistors. Thus, the evaluation is performed with the parallel transistors and, therefore, it is faster.

III. Design Of Dml Nand, Nor & Not Gates

The basic logic gates NAND, NOR & NOT are implemented using Dual Mode Logic using Tanner EDA tool. The schematic is simulated for Type A and B in static & dynamic modes and power is analyzed. In the DML Type-A Static NAND topology, the switching element is a PMOS transistor connected parallel to the Pull-up network. The input to the switching element is a constant high voltage to make it OFF. The only difference when designing DML Type-A Dynamic NAND topology, is that the input to the switching element is a clock signal having pre-charge and evaluate phase for dynamic mode of operation. Conventional NOR logic gate design is done using Tanner S-Edit EDA tool and its power and performance are found. Also Dual Mode Logic NAND gate Type A and Type B topologies designed and their power consumption and performance were analyzed for static and dynamic mode of operations.

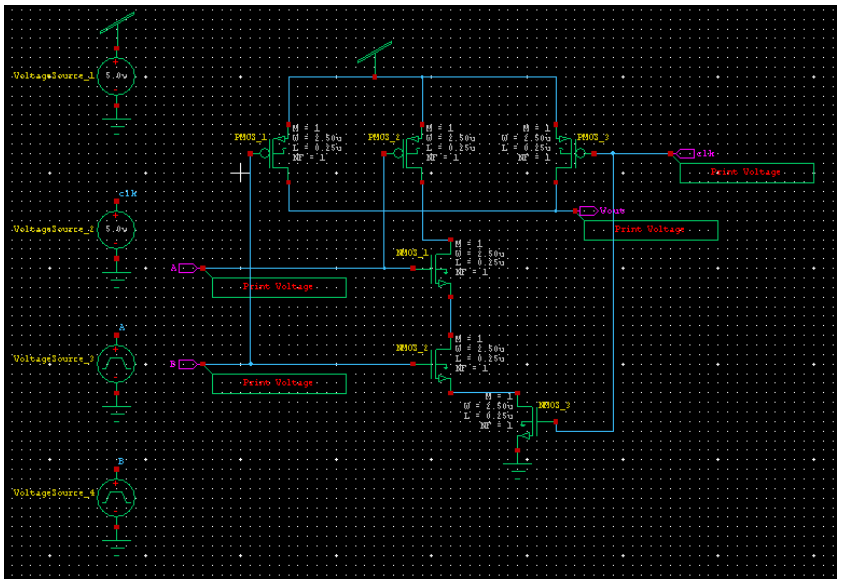

Figure 2: Schematic of Type A Static NAND gate

.In the DML Type-A Static NOR topology, the switching element is a PMOS transistor connected parallel to the Pull-up network which is a series connection of 2 PMOS transistors. The input to the switching element is a constant high voltage to make it OFF. The only difference when designing DML Type-A Dynamic NOR topology, is that the input to the switching element is a clock signal having pre-charge and evaluate phase for dynamic mode of operation. In the DML Type-B Static NOR topology, the switching element is an NMOS

transistor connected parallel to the Pull-down network which is a parallel connection of 2 NMOS transistors. The input to the switching element is a constant low voltage to make it OFF. The only difference when designing DML Type-B Dynamic NOR topology is that the input to the switching element is a clock signal having pre-charge and evaluate phase for dynamic mode of operation. Also Dual Mode Logic NOT gate Type A and Type B topologies designed and their power consumption and performance were analyzed for static and dynamic mode of operations. In the DML Type-A Static NOT topology, the switching element is a PMOS transistor connected parallel to the Pull-up network. The input to the switching element is a constant high voltage to make it OFF.

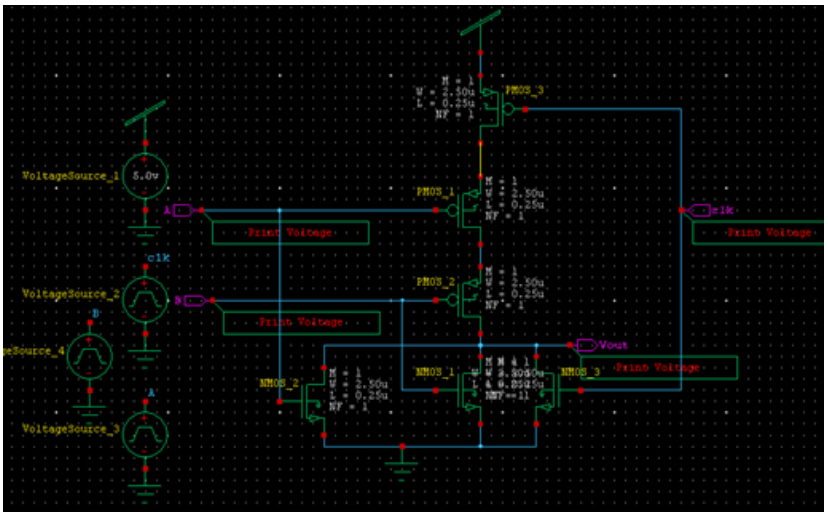

Figure 3: Schematic of Type B Dynamic NOR gate

The only difference when designing DML Type-A and B Dynamic NOT topology is that the input to the switching element is a clock signal having pre-charge and evaluate phase for dynamic mode of operation. In the DML Type-B Static NOT topology, the switching element is an NMOS transistor connected parallel to the Pull-down network. The input to the switching element is a constant low voltage to make it OFF.

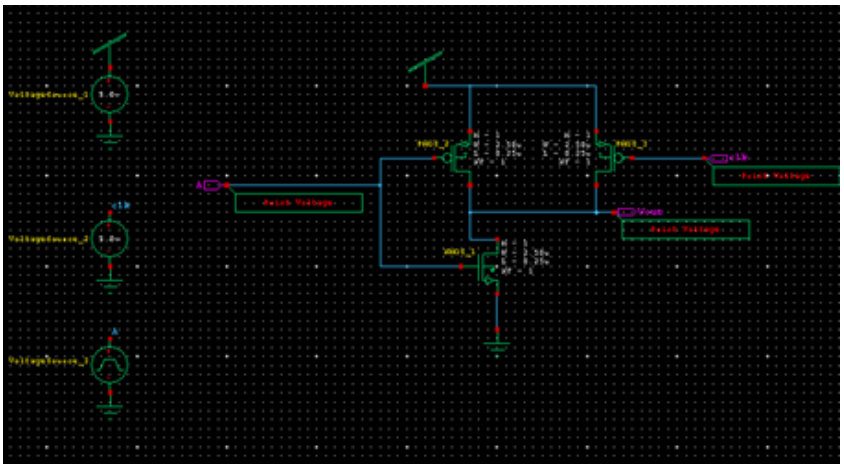

Figure 4: Schematic of Type A Static NOT gate

IV. Power Gating In Dml Circuits

Power gating affects design architecture more than clock gating. It increases time delays, as power gated modes have to be safely entered and exited. Architectural trade-offs exist between designing for the amount of leakage power saving in low power modes and the energy dissipation to enter and exit the low power modes. An externally switched power supply is a very basic form of power gating to achieve long term leakage power reduction. To shut off the block for small intervals of time, internal power gating is more suitable. CMOS switches that provide power to the circuitry are controlled by power gating controllers. Outputs of the power gated block discharge slowly. Hence output voltage levels spend more time in threshold voltage level. This can lead to larger short circuit current. Power gating uses low-leakage PMOS transistors as header switches to shut off power supplies to parts of a design in standby or sleep mode. NMOS footer switches can also be used as

sleep transistors. Inserting the sleep transistors splits the chip's power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off. Typically, high-Vt sleep transistors are used for power gating, in a technique also known as multi-threshold CMOS (MTCMOS). The sleep transistor sizing is an important design parameter. The quality of this complex power network is critical to the success of a power-gating design. Two of the most critical parameters are the IR-drop and the penalties in silicon area and routing resources. Power gating can be implemented using cell- or cluster-based (or fine grain) approaches or a distributed coarse-grained approach.

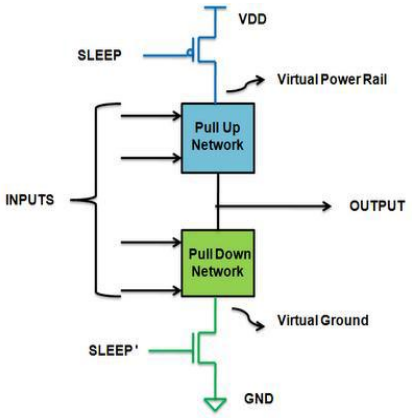

Figure 5: Power Gating implementation

In active mode, SLEEP signal is set to logic 0 and SLEEP` signal is set to logic 1. Hence T1 & T2 transistors are ON. In this case both the transistors offer very low resistance. Virtual ground (VGND) node potential is pulled down to the ground potential. This makes the logic difference between the logic circuitry approximately equal to the supply voltage. Whereas in sleep mode, SLEEP signal is set to logic 1 and SLEEP` signal is set to logic 0. Hence T1 & T2 transistors are OFF. Logic part is disconnected from the supply and ground leading to very less power consumption during the sleep mode.

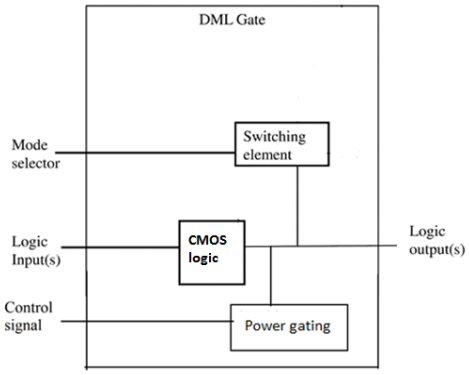

Figure 6: Proposed Block Diagram

Different methods of power gating like the sleep method, sleepy stack and dual sleep approaches added to the existing Dual mode logic NAND, NOR, NOT gates. The Sleep method is the basic power gating method. The sleep transistors isolate the logic networks and the sleep transistor technique or the sleep method dramatically reduces leakage power during sleep mode.

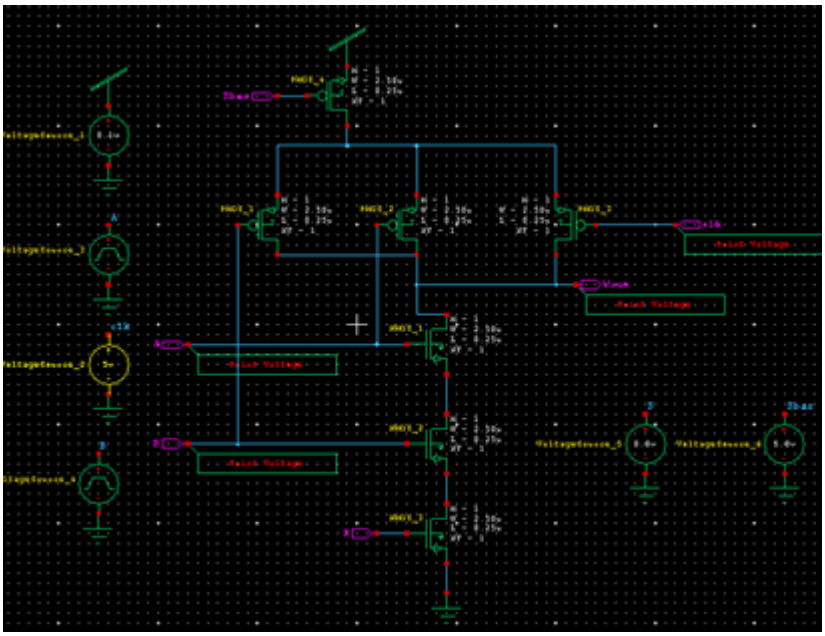

Figure 7: Schematic of Type A Static NAND gate with Sleep Power Gating

The sleepy stack approach merges the sleep and stack approaches. The sleepy stack technique splits the existing transistors into two half Size transistors like the stack approach. The activity of the sleep transistors in the sleepy stack method is same as the activity of the sleep transistors in the sleep method. The sleep transistors are turned on during the active mode and they are turned off during the sleep mode. Figure below shows Type B Dynamic NOT gate with Sleepy Stack Power Gating Technique.

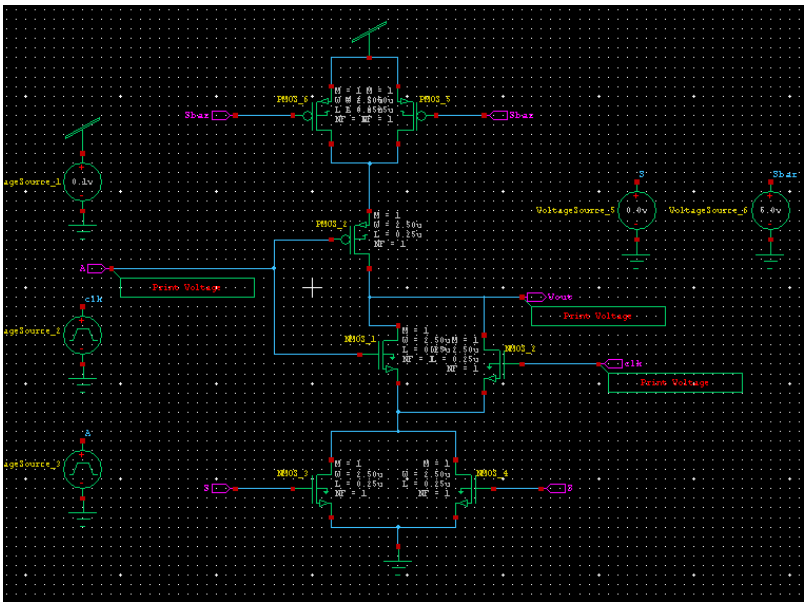

Figure 8: Schematic of Type B Dynamic NOT gate with Sleepy Stack Power Gating

The Dual sleep approach has the advantage of using the two extra pull- up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. In normal mode when S=1 the pull down NMOS transistor is in ON state and in the pull-up network the PMOS sleep transistor is in ON state since S‟=0.

During sleep mode state S is forced to 0 and hence the pull-down NMOS transistor is in OFF state and PMOS transistor is in ON state and in the pull-up network, PMOS sleep transistor is OFF while NMOS sleep transistor is ON. So in sleep mode state a PMOS is in series with an NMOS both in pull-up network and pull-down network which reduces the power dissipation. Figure below shows Type A Static NAND with Dual Sleep Power Gating Technique.

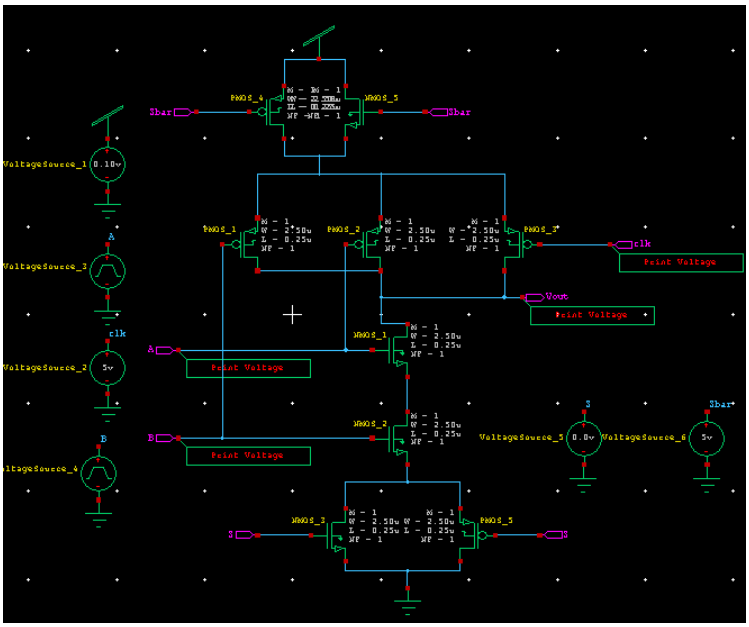

Figure 9: Schematic of Type A Static NAND gate with Dual Sleep Power Gating

The total power consumption in watts for NAND, NOR and NOT logic gates and Full Adder in Type A and B is tabulated below.

TYPE	NAND	NOR	NOT
CONVENTIONAL	6.24E-09W	5.11E-09W	3.35E-09W
TYPE A STATIC	5.32E-09W	4.91E-09W	2.37E-09W
TYPE A DYNAMIC	9.44E-09W	5.54E-09W	1.15E-09W
TYPE B STATIC	6.07E-09W	5.08E-09W	3.27E-09W
TYPE B DYNAMIC	7.02E-09W	5.15E-09W	3.26E-09W

Table 1: Power Comparison of NAND, NOR and NOT gates

The NAND, NOR and NOT Dual mode logic gate is compared in terms of power consumption for different power gating techniques like sleep method, sleepy stack method and dual sleep method in tables given below.

TYPE	NAND SLEEP	NAND SLEEPY STACK GATING	NAND DUAL SLEEP GATING
CONVENTIONAL	1.71E-09W	2.06E-09W	1.01E-08W
TYPE A STATIC	1.36E-09W	7.42E-10W	7.39E-09W
TYPE A	2.73E-09W	3.29E-09W	1.34E-08W
TYPE B STATIC	1.55E-09W	8.32E-10W	9.87E-09W
TYPE B	2.13E-09W	8.09E-09W	1.14E-08W

Table 2: Comparison between NAND DML gates with different power gating techniques

	NOR SLEEP	**NOR SLEEPY STACK**	**NOR DUAL SLEEP**
CONVENTIONAL	2.88E-09W	2.34E-09W	2.79E-09W
TYPE A STATIC	2.29E-09W	2.19E-09W	1.90E-09W
TYPE A	7.74E-09W	2.44E-09W	5.55E-09W
TYPE B STATIC	2.87E-09W	1.88E-09W	1.37E-09W
TYPE B	3.12E-09W	3.15E-09W	2.90E-09W

Table 3: Comparison between NOR DML gates with different power gating techniques

TYPE	**NOT SLEEP**	**NOT SLEEPY STACK**	**NOT DUAL SLEEP**
CONVENTIONAL	1.68E-09W	2.54E-09W	1.79E-09W
TYPE A STATIC	5.09E-09W	3.49E-09W	1.95E-09W
TYPE A	5.34E-09W	1.94E-09W	1.75E-09W
TYPE B STATIC	1.45E-09W	2.20E-09W	1.57E-09W
TYPE B	1.60E-09W	2.75E-09W	2.12E-09W

Table 4: Comparison between NOT DML gates with different power gating techniques

V. Conclusion

From the results, we can observe that in Static mode there is a power reduction as compared to conventional mode. The DML sizing strategy results in reduced energy dissipation, as compared to conventional static CMOS gates. DML has immunity to process variations, temperature fluctuations, and solving some of the domino's well known drawbacks such as charge sharing, crosstalk noise, and susceptibility to glitches, which intensify with process and voltage scaling. The implementation of Power gating techniques has further reduced the total power consumption.

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