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Quadrature Delta Sigma Modulator Design and Overview

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Abstract: *Quadrature Band pass ADC is well known to be adopted in order to reduce the system complexity, increase integration and improve performance by digitizing the bandpass signal directly without prior conversion to baseband. The Quadrature sigma delta modulator is analyzed for different quantization level for the different parameters like Signal to noise distortion ratio, quantization noise rejection capability for various devices. The result highlights the analysis of different quadrature bandpass modulators which provides a good order modulator and help to enhance device efficiency.*
Keywords: *Analog-to-digital conversion, bandpass delta-sigma modulator, Signal to Noise Ratio, Quantization Noise*

I. Introduction

Considerable research effort pushes toward the realization of fully monolithic, chiefly digital, RF transceivers with the ultimate objective being the implementation of small, inexpensive, low-power communication devices that are robust, testable, and capable of handling multiple communications standards. Quadrature band-pass sigma-delta modulators are important building blocks for communication systems. Superheterodyne receivers often use quadrature mixers with complex signals that must be transformed into digital form.

Often use quadrature mixers with complex signals that must be transformed into digital form sigma-delta converters are used with an aim of high level of reliability and functionality with reduced chip cost. Often zero IF solutions are unattractive because of the demanding image rejection requirements. Even low-IF for which the DC offset and the 1/f noise fall outside the signal band can be problematic for low power applications: the architecture must use wide-band A/D converters that are power hungry.[1] The solution is using quadrature or complex modulators that suppress the quantization noise only in the signal band and not the image band.

This paper proposes a new design approach that locks the IF frequency to the clock frequency of the complex modulator. The accuracy of coefficients possibly influences the relative position of the zeros of the NTF but the notch is firmly defined. The proposed methodology is applied to different cases scheme and Simulation results indications on the possible circuit implementation are given.

They can use in several applications like wireless, communication, medical .In these application multiple devices face the hurdle of SNR, NTF e.g. Digital Radio therefore the paper focuses on these wireless devices that require various parameters to improve its performance. This paper describes such an IC, which is a quadrature variant of a bandpass delta– sigma ∑Δ modulator.

II. Theory

General aspect:

A conventional quadrature ∑Δ converter consists of an input branch, a loop filter and feedback branch.The main difference between the real and quadrature modulator is that the quadrature modulator operates on complex input samples and similarly the output is given in complex form. [2]

A complex loop filter,employed in the quadrature modulator, can be realized as a complex integrator when considering the first order modulator .Higher order systems usually have multiple integrator includes . The main principle is similar as in a real integrator used in low pass ∑Δ modulators input sample are integrated over a unit delay the difference to a real system being that the samples are complex valued, as is the loop gain.

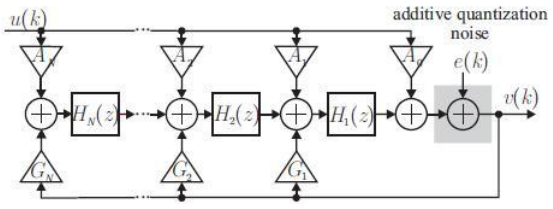

Figure 1: Gernal quadrature delta sigma modulator

The basic structure of quadrature delta sigma modulatore present in figure 1, where u(k),v(k) and e(k) are the complex inputs the linearized complex quantization error and the complex output signal respectively the multipliers A and G are complex valued and affect the input signal fed straight to quantizer, the input fed signal to the loop filter H[z] and the feedback signal from the output of the modulator .[3]

Based on this kind of structure, the Z- domain transfer function of the modulator can be derived. Thus the output v[z] of the modulator can be expressed with the input u[z] and quantization error E[z] as

V[z] □ (A □ BH[z])U[z] □ E[z] □ GH[z]V[z] ……. (1)

Where A, B, G and H [z] are mentioned before in figure 1. More details of the overall transfer function will be given in following sections where STF and NTF are treated separately.

Conventional methodologies:

Low-IF has been used in many receiver architectures in which different A/D conversion approaches. One uses two separate ADC's for I and Q channels or sharing one ADC for both channels. These ADC's are often pipelined-type but also they may be ∑ΔADC's. However, both approaches consume significant power and area. Reducing the number of NTF zeros with a complex or quadrature type A/D converter diminishes the power while keeping the benefit of the band-pass noise shaping. The mismatch in quadrature A/D converters can be source of tones in the image position; problem overcame by placing a zero on the image or by taking advantage of system specifications such as GSM.[4] The IF frequency of quadrature A/D converters is independent clock frequency, but in case of a mismatch, the independency becomes source of error requiring the possible use of complex calibration or trimming methods. Although it is possible to select IF frequency and clock frequency such that the performance degradation in case of a mismatch error is limited. Hence, in reality these frequency are not independent but for effective design they should be related in the design phase for robust performance.

NTF of quadrature delta sigma modulator:

In quadrature ∑Δ converters, the first design step is the placements of zeros since the shaping of the noise transfer function (NTF) determines bandwidth and resolution. The second step is the definition of the block diagram in the z-domain and then it is necessary to find the circuit implementation. Many architectures use the integrators as basic blocks that are actually delays in loop configuration. This work foresees a generalization with multiple feedbacks and delay elements.[5] Before studying possible block diagrams let us consider the noise transfer function of a system with a set of zeros on the unity circle at the positions $e^{j\phi}$, i=1,n. The NTF is

Therefore, depending on the zero position the last term which has module one and phase that is the addition of the phase of all the zeros.

Design Methodology:

Summing up the above study we can summarize the proposed design method for a band-pass quadrature modulator with the following steps.

1) Calculate the required SNR and bandwidth for achieving The desired specifications.[6]
2) Calculate the order of the system regarding the SNR value calculated.
3) Decide where to place zeros of the system. If for image rejection another zero is required, and then increases the order of the system.
4) After the calculation of number of zeros and their placement, select which NTF (with 1, j, −1 or −j) is suitable for covering these zeros.
5) Set the coefficients in the intermediate injection points for achieving the desired zero locations.
6) Perform behavioral simulation for verification.

III. Design Examples

The proposed method has been verified in the design of modulators with 2, 3 or four zeros without complex conjugate counterparts. Figure 2 shows the location of the complex zeros that have phase $3\pi/4 \pm \pi/20$. This design requires using K=1.4 in the extra injection point. The obtained noise shaping with 4-bit quantizer is shown in Figure 3. The SNR with OSR=8 is as good as 74.5 dB.

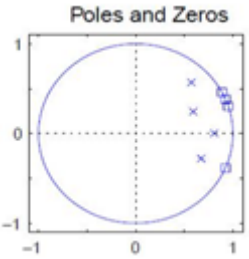

Figure 2: Location of complex zeros and poles in phase

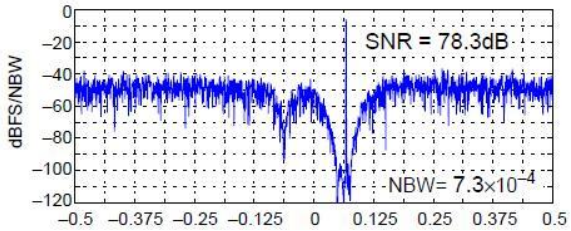

Figure 3: Noise shaping with 4 bit quantizer

The circuit uses four delay blocks compared to four integrators required by a conventional counterpart Moreover, the scheme can be realized with a sampled-data or continuous time approach. However, for continuous-time, the request of calibration is not as critical as for the conventional solutions. Figure 4 shows the quantized output signal for input sine wave. In the figure, it is shown that the signal has no slope overload and following input signal.

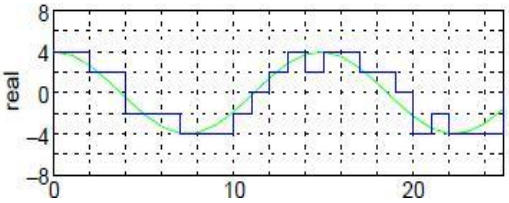

Figure 4: Output quantized signal

The design example with three zeros uses $\varphi 1 + \varphi 2 + \varphi 3 = \pi/2+4\pi$ that gives $jz-3$ as the higher order term of the NTF. The zeros with $\varphi 1 = 17\pi/2$, $\varphi 2 = 18\pi/2$ and $\varphi 2 = 19\pi/2$ are shown in Figure 5 shows the noise shaping along with the signal tone. The chosen value of coefficients grants a wide signal band (fN/4) with a significant SNR. The position of thefour zeros can be used to equalize the peaks of the noise in the signal band or, as done in the example, for rounding value of coefficients as required by an effective design[7]-[9].

The result is that the value of unity capacitance used in an SC implementation is acceptable while obtaining a good matching.

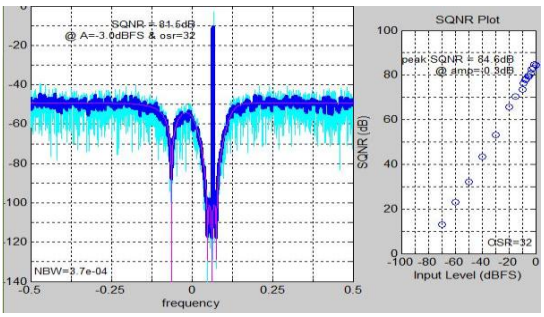

Figure5: PSD for fourth order system

Figure 6 shows the comparison of noise transfer function and signal transfer function in the quadrature modulator.It shows the effect of mismatch in the NTF and STF.

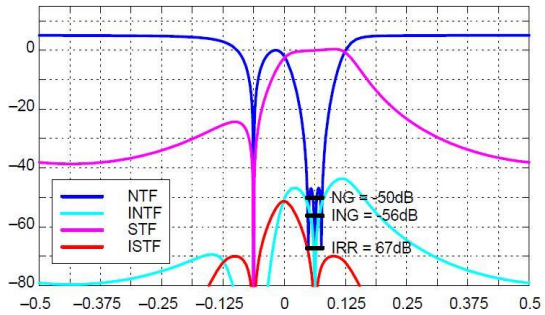

Figure 6: Effect of mismatch in NTF and STF

IV. Conclusion

This work proposes a new methodology which is suitable for quadrature ADC's to be use in Low-IF communication Architectures. The novel method of locking frequencies limits the possible transfer functions to a sub-set of possibilities. However, the resulting architectures that use unity delays and adders obtain a limited sensitivity to errors. The NTF zero placements is straightforward with the possibility to avoid using zeros in the conjugate position. This option for high order architectures optimizes the power consumption. Provided examples prove that the methodology can be implemented to different orders to achieve different NTF responses.

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