

Design and Implementation of combinational circuits in different low power logic styles

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Abstract: Low power consuming devices are playing a dominant role in the present day VLSI design technology. If the power consumption is less, then the amount of power dissipation is also less. The power dissipation of a device can be reduced by using different low power techniques. In the present paper the performance of binary to gray code converter in different low power techniques was analyzed and its power dissipation in those techniques is compared with the conventional CMOS design. Each of these techniques has different advantages depending on their logical operation.

Keywords- Low power, Power dissipation, Multiplexer, DPTL, Adiabatic, Charge recovery

I. Introduction

The need for low power devices has been increasing rapidly. As many of the present day electronic devices are portable, they need more battery backup which can be achieved only with the low power consumption circuits that are internally designed in them. So energy efficiency has become main concern in the portable equipment's to get better performance with less power dissipation. As the power dissipation in a device increases then extra circuitry is necessary to cool the device and to protect the device from thermal breakdown which also results in increase of total area of the device. In order to overcome these problems the power dissipation of the circuit is to be reduced by adopting different low power techniques. The less the power dissipation, the more efficient the circuit will be. From the past few decades CMOS technology plays a dominant role in the design of low power consuming devices. Compared to different logic families CMOS has less power dissipation which made it superior over the previous low power techniques. The power consumption in conventional CMOS circuit is due to switching activity of the devices from one state to another state and due to the charging and discharging of load capacitor at the output node. The power dissipation in conventional CMOS design can be minimized by reducing the supply voltage, node capacitance value and switching activity. But reducing the values of these parameters may degrade the performance of the device. So an efficient low power technique other than CMOS is needed that has less power dissipation compared to CMOS. In the present paper different low power techniques Dual Pass Transistor Logic (DPTL), 2x1 multiplexer based design and Adiabatic logic are discussed and their performance is compared with CMOS design.

II. Binary To Gray Code Converter

The gray code is often used in digital systems because it has the advantage that only one bit in the numerical representation changes between successive numbers. It is also known as Self Complementing code.

Decimal	Binary code				Gray code			
	D	C	B	A	G3	G2	G1	G0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	0
13	1	1	0	1	1	0	1	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

Table 1: Truth table for binary to gray code converter

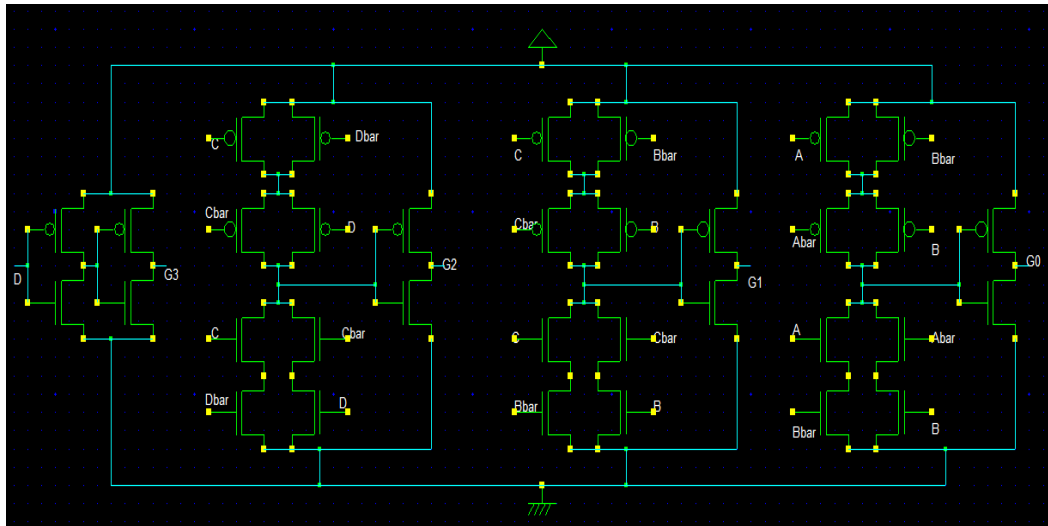


Fig 1: CMOS Binary to Gray code converter

III. Low Power Techniques

Power consumption of a circuit can be reduced by using different techniques depending on the area of application.

3.1.1 Dual Pass Transistor Logic (DPTL)

A logic circuit can be optimized in terms of power and area to a great extent by using DPTL logic. It reduces the power dissipation and transistor count of a logic circuit compared to CMOS design which makes it suitable for low power and portable applications. A basic DPTL cell contains pMOS and nMOS transistors connected in parallel. The binary to gray code converter in DPTL logic can be designed as

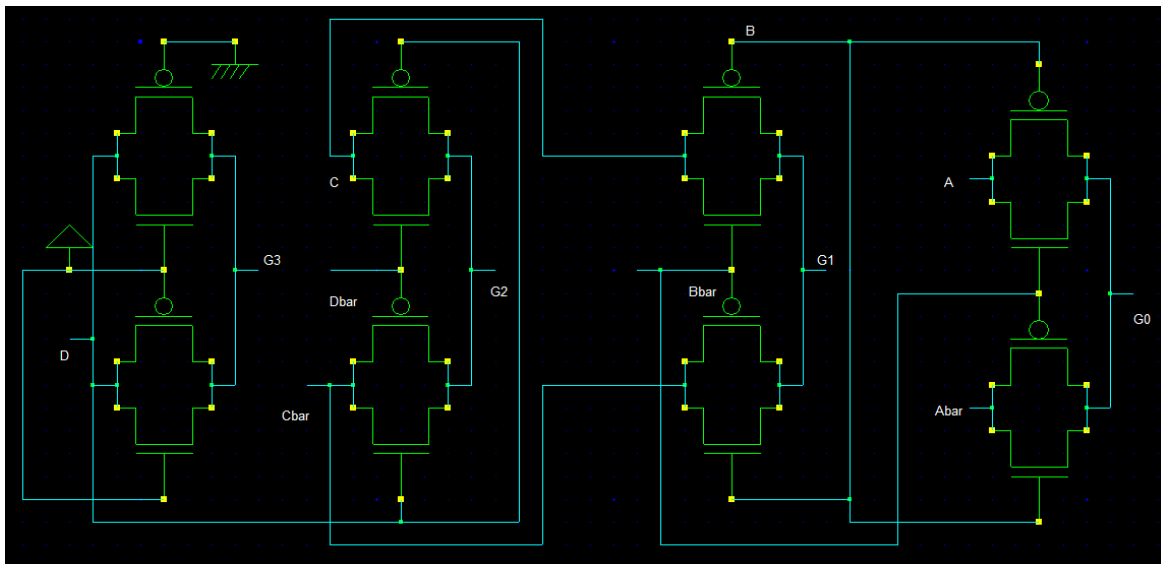


Fig 2: Binary to Gray code converter using DPTL technique

3.1.2 2x1 Multiplexer based design

The logic is implemented using 2x1 multiplexers which has two inputs and one output for each multiplexer with a select line in its structure. The output is generated depending on the selection line only. These multiplexers can be designed with the help of pass transistor logic that uses parallel PMOS and NMOS transistors.

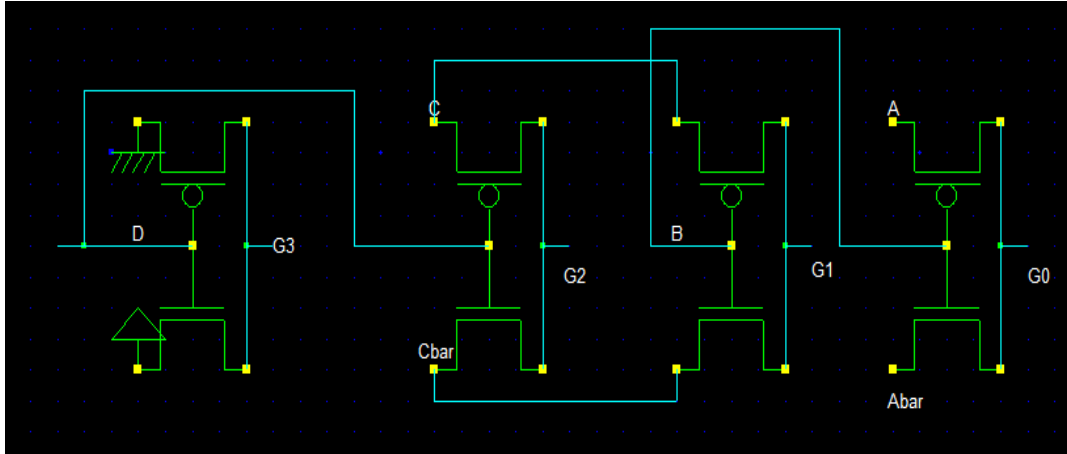


Fig 3: Binary to Gray code converter using 2x1 mux.

3.1.3 Adiabatic Logic

Adiabatic logic is based on charge recovery principle. It reuses the energy which is dissipated during the charging and discharging process of circuit operation. As the name itself indicates that instead of dissipating the stored energy during charging process at the output node towards ground it recycles the energy back to the power supply thereby reducing the overall power dissipation and hence the power consumption also decreases. The adiabatic logic uses AC power supply instead of constant DC supply, this is one of the main reasons in the reduction of power dissipation. The binary to Gray code converter can be constructed using adiabatic logic as

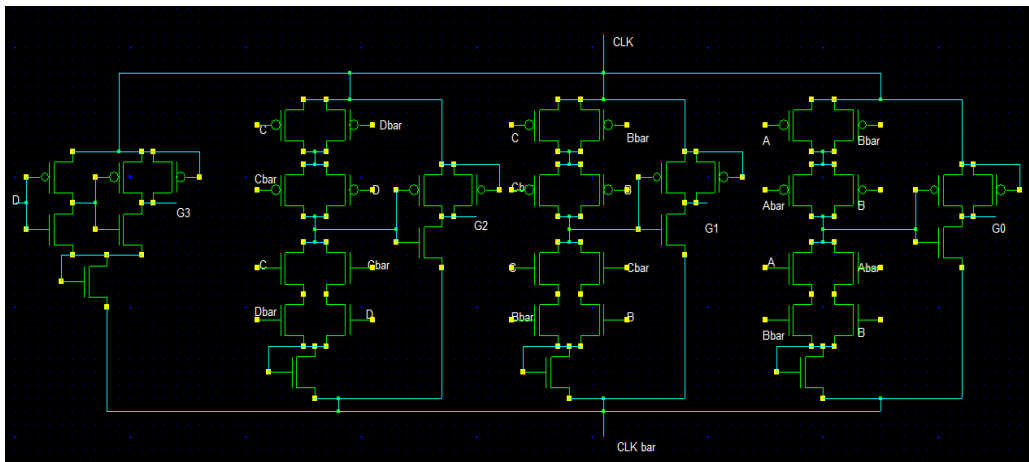


Fig 4: Binary to Gray code converter using Adiabatic Logic.

IV. Simulation Results And Discussion

The simulation results were verified using HSPICE simulation software. The simulation results of binary to gray code converter in conventional CMOS design and different low power techniques were presented in this section.

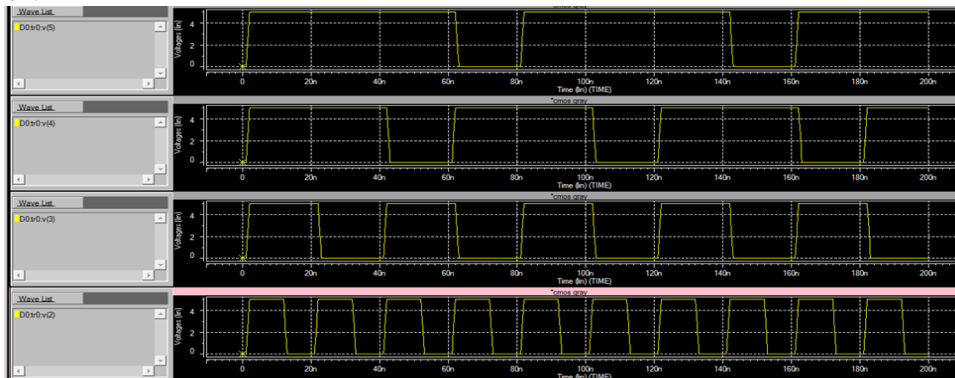


Fig 5: Simulated Waveforms for input binary code

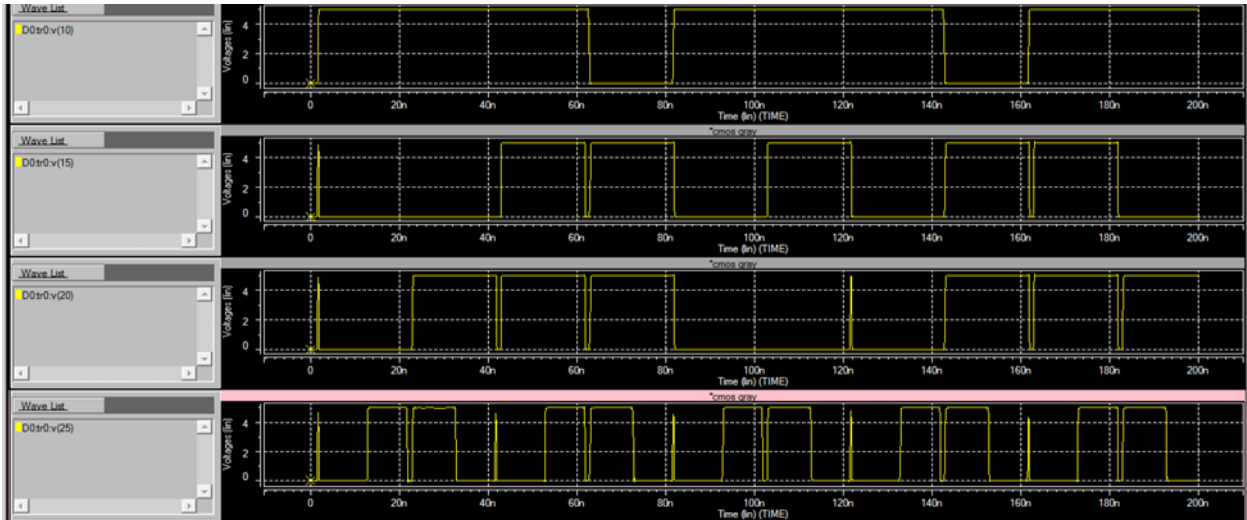


Fig 6: Simulated Waveforms for output gray code in CMOS design

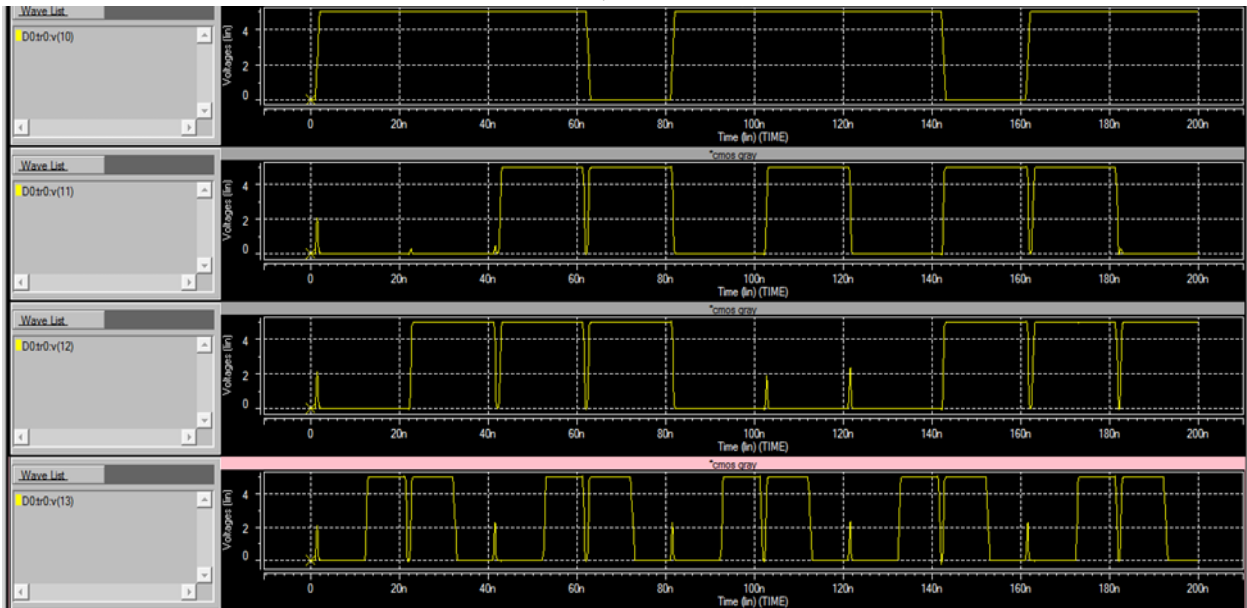


Fig 7: Simulated waveforms for output gray code in DPTL logic.

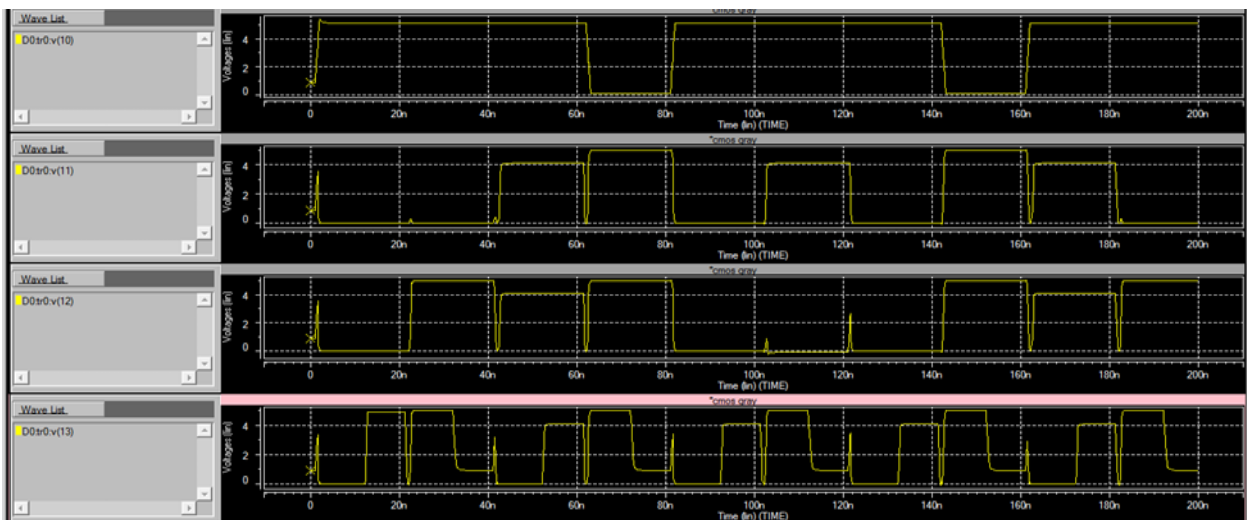


Fig 8: Simulated waveforms for output gray code using 2x1 mux

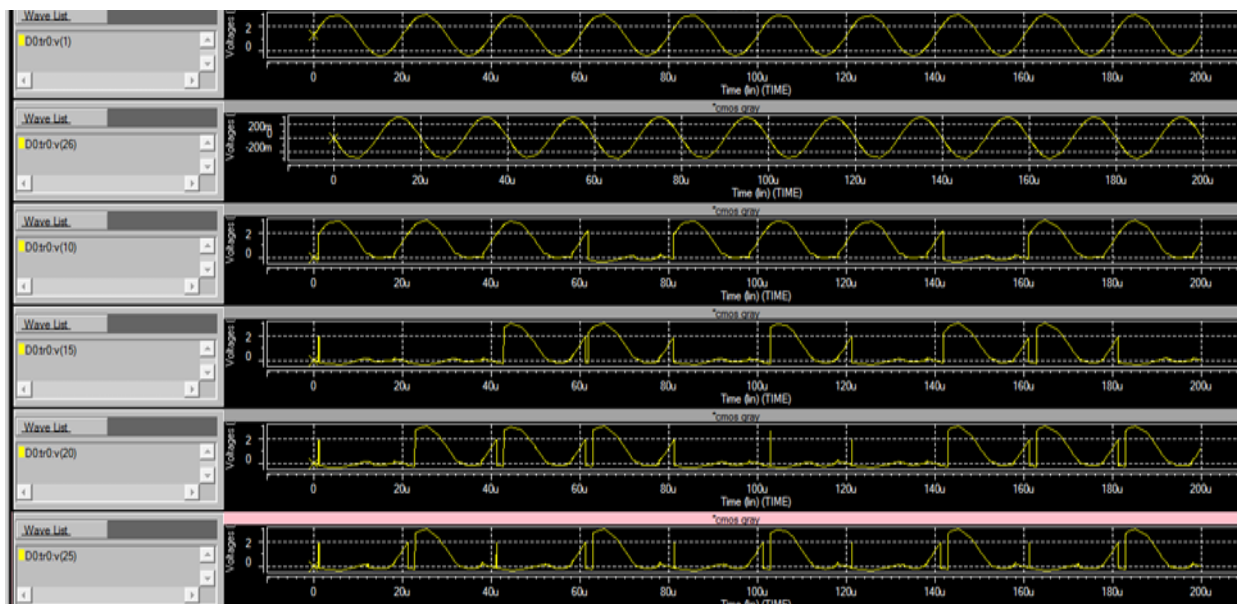


Fig 9: Simulated waveforms for output gray code using Adiabatic Logic.

Table 2: Comparison of Power dissipation and size of binary to gray code converter in different low power techniques

S.No	Logic Style	Power Dissipation (pWatts)	Transistor Count
1.	CMOS	815.2577	40
2.	DPTL	755.0000	24
3.	2X1 MUX	568.7469	12
4.	Adiabatic Logic	53.3354	48

Table 2 shows the power dissipation and transistor count of binary to gray code converter in different low power techniques. The adiabatic logic has less power dissipation compared to other design styles and 2x1 mux has less transistor count compared to other design styles. Depending upon the area of application and circuit structure an appropriate design style can be used to reduce the power dissipation and area.

V. Conclusion

This paper proposes different low power techniques that can be used for the digital circuits. The results were simulated using HSPICE and comparison has been done for different parameters of binary to gray code converter in different low power techniques and CMOS design. The results show that the proposed techniques has less power dissipation compared to conventional CMOS design with less transistor count. These advantages made these logics more convenient for energy efficient digital applications.

References

- [1]. B. Dilli Kumar, M. Bharathi, "Design of Energy Efficient Arithmetic Circuits Using Charge Recovery Adiabatic Logic in International Journal of Engineering Trends and Technology, 2013.
- [2]. Gate-diffusion input (GDI) – A technique for low power design of digital circuits: Analysis and characterization, in Proc. Int. Symp. Circuits and Systems (ISCAS), May 2002.
- [3]. A. Morgenshtein, A. Fish, and I. A. Wagner, "Gate-diffusion input(GDI) – A novel power efficient method fordigital circuits: A detailed methodology," in Proc. 14th IEEE Int. ASIC/SOC Conf., Sept. 2001,pp. 39– 43.
- [4]. R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," IEEE J. Solid-State Circuits, vol. 32, no. 7, pp. 1079{1090, Jul. 1997.
- [5]. K. Yano, Y. Sasaki, K. Rikino, and K. Seki, "Top-down pass-transistor logic design," IEEE J. Solid-State Circuits, vol. 31, pp. 792–803, June1996.
- [6]. A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low- power CMOS digital design," IEEE J. Solid-State Circuits, vol. 27, pp.473–484, Apr. 1992.