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Implementation of High Speed Low Power Combinational and Sequential Circuits using Reversible logic

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Abstract - *Reversible logic has presented itself as a prominent technology which plays an imperative role in Quantum Computing. Quantum Computing devices theoretically operate at ultra high speed and consume infinitesimally less power. Research done in this paper aims to utilize the idea of reversible logic to break the conventional speed-power trade-off, thereby getting a step closer to realize Quantum computing devices. To authenticate this research, various combinational and sequential circuits are implemented such as a 4-bit Ripple-carry Adder, (8- bit X 8-bit) Wallace Tree Multiplier, and the Control Unit of an 8-bit GCD processor using Reversible gates. The power and speed parameters for the circuits have been indicated, and compared with their conventional non-reversible counterparts. The comparative statistical study proves that circuits employing Reversible logic thus are faster and power efficient. The designs presented in this paper were simulated using Xilinx 9.2 software.*

Key Terms - *Reversible logic, Quantum computing, high-speed, less power, speed-power trade-off, Ripple carry adder,*

I. Introduction

Reversible logic is widely used in low power VLSI.Reversible circuits are capable of back-computation and reduction in dissipated power, as there is no loss of information [1]. Basic reversible gates are employed toachieve the required functionality of a reversible circuit.The uniqueness of reversible logic is that, there is no loss ofinformation since there is one-to-one correspondencebetween inputs and outputs. This enables the system to runbackwards and while doing so, any intermediate designstage can be thoroughly examined. The fan-out of eachblock in the circuit has to be one.This research paper focuses on implementation ofreversible logic circuits in which main aim is to optimizespeed of the design. A Reversible adder is designed usingbasic reversible gates. Using this adder, an 8-bit reversibleripple-carry adder is devised and then compared with theconventional 8-bit adder in terms of speed, critical paths, hardware used. Then using the same reversible adder, aWallace tree multiplier has been implemented, andcompared with the conventional Wallace tree multiplier[3].With the known fact that sequential circuits are the heart ofdigital designing, the design for the control unit of areversible GCD processor has been proposed using Reversible logic gates [2].

II. Reversible Logic

Boolean logic is said to be reversible if the set of inputsmapped have an equal number of outputs mapped i.e. theyhave one-to-one correspondence. This is realized employingreversible gates in the designs. Any circuit having onlyreversible gates is capable of dissipating no power.

Goals of Reversible Logic:

A. Quantum Cost: Quantum cost of a circuit is the measureof implementation cost of quantum circuits. More precisely, quantum cost is defined as the number of elementaryquantum operations needed to realize a gate.

B. Speed of Computation: The time delay of the circuitsshould be as low as possible as there are numerouscomputations that have to be done in a system involving aquantum processor; hence speed of computation is a very important parameter while examining such systems.

C. Garbage Outputs: Garbage outputs are those outputsignals which do not contribute in driving further blocks in the design. These outputs become redundant as they are notrequired for computation at a later stage. The garbage outputs make the system slower; hence for better efficiencyit is necessary to minimize the number of garbage outputs [5].

D. **Feedback:** Looping is strictly prohibited when designingreversible circuits.

E. Fan-out: The output of a certain block in the design canonly drive at most one block in the design. Hence it can be said that the Fan-out is restricted to 1

III. Major Several Reversible Logic

3.1 Feynman Gate

It is a 2*2 Feynman gate [13]. The input vector is I (A, B) and the output vector is O(P, Q). The outputs are defined y P=A, Q=AÅB. Quantum cost of a Feynman gate is 1. Figure 1 shows a 2*2 Feynman gate..

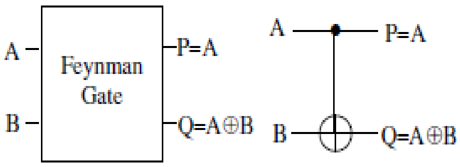

Fig 1: Feynman gate

3.2 Double Feynman Gate (F2G)

It is a 3*3 Double Feynman gate [4].The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P = A, Q=AÅB, R=AÅC. Quantum cost of double Feynman gate is 2. Figure 2 shows a 3*3 Double Feynman gate.

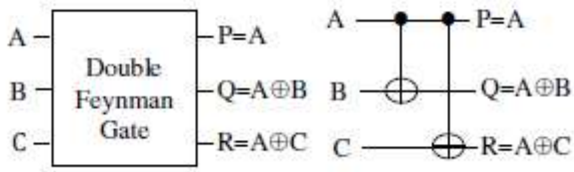

Fig 2: Double Feynman gate

3.3 Toffoli Gate

It is a 3*3 Toffoli gate [6] The input vector is I(A, B, C) and the output vector is O(P,Q,R). The outputs are defined by P=A, Q=B, R=ABÅC. Quantum cost of a Toffoli gate is 5. Figure 3 shows a 3*3 Toffoli gate.

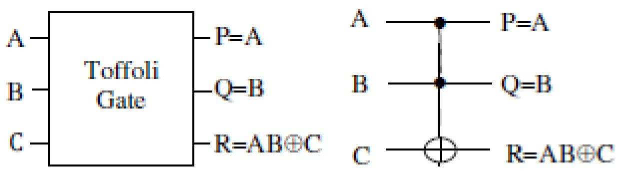

Fig 3: Toffoli gate

3.4 Fredkin Gate

It is a 3*3 Fredkin gate [7]. The input vector is I (A, B, C) and the output vector is O(P, Q, R). The output is defined by P=A, Q= A_ BÅAC and R= A_ CÅAB. Quantum cost of a Fredkin gate is 5. Figure 4 shows a 3*3 Fredkin gate.

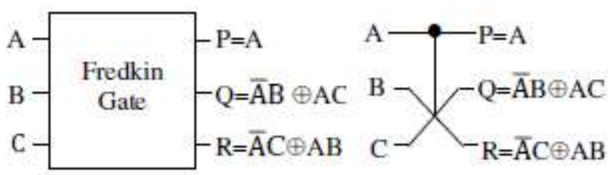

Fig 4: Fredkin gate

3.5 Peres Gate

It is a 3*3 Peres gate [5]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = AÅB and R=ABÅC. Quantum cost of a Peres gate is 4. Figure 5 shows a 3*3 Peres gate.

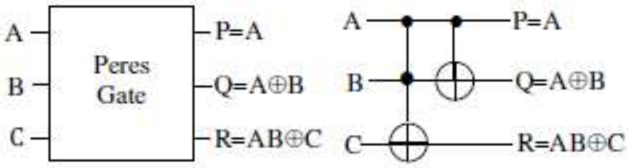

Fig 5: Peres gates

3.6 Double Peres gate

It is a 4*4 Double Peres Gate [6]. The input vector is I(A,B,C,D) and the output vector is O(P,Q,R,S).The output is defined by P=A,Q=AÅB,R=AÅBÅD and S=(AÅB)DÅABÅC. Figure 6 shows a 4*4 Double Peres gate.

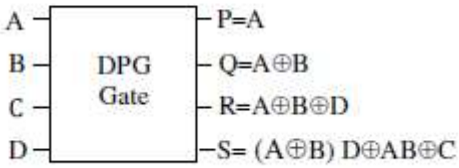

Fig 6: DPG gate.

IV. Reversible 4- Bit Full Adder

The gate used in implementing a reversible ripple-carry full adder is the TSG gate [4]. The TSG gate functions like a full adder. A reversible ripple-carry adder is faster than the non-reversible adder, since the computation of carry in a reversible adder does not require the computation of previous stage carry (as indicated in the critical paths). When previous stage carry is being forwarded in the reversible adder, the computation of previous stage carry and computation regarding sum is done simultaneously whereas in an irreversible adder the next stage carry cannotstart any computation till previous stage carry is fully generated. The critical paths of 4bit reversible and irreversible ripple-carry adders are as shown in fig.7 and fig.8.[6].

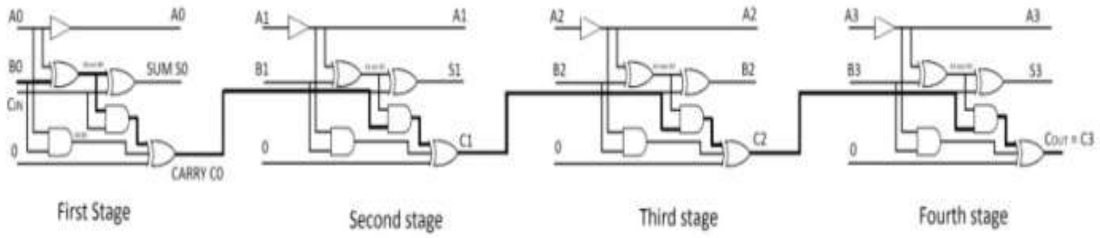

Fig. 7: Critical Path of 4-bit reversible adder

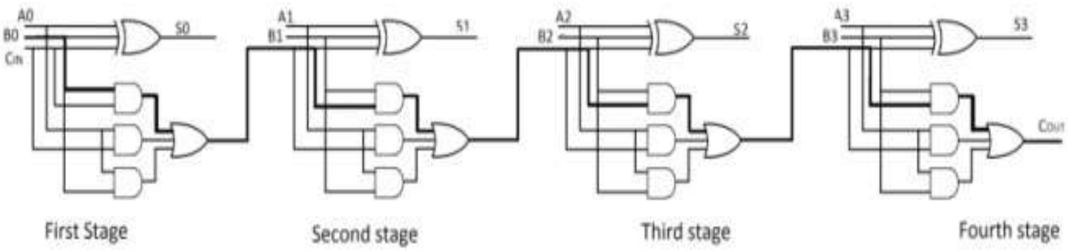

Fig. 8: Critical Path of 4 bit irreversible adder

Furthermore, various parameters of reversible and non reversible adders were observed and compared and are tabulated in Table 1.

Table 1: Comparison of Reversible and Irreversible RCA

Parameter (Virtex5 XC5VLX30 family)	8bit Reversible RippleCarry Adder	8bit Irreversible RippleCarry Adder	Improvement For Reversible Circuit (%)
Time delay	5.062ns	5.547ns	8.74%
Power	267.18mW	290mW	7.87%
Area(No.of .LUTs)	11	13	15.38%

V. Wallace Tree Multiplier

A Wallace tree is an efficient hardwiredimplementation of a digital circuit that multiplies twointegers [5]. The Wallace tree has three steps:

1. Every bit of the multiplicand is multiplied (i.e. AND)by every bit of multiplier, thus yielding n2 results (for n Xn multiplication). Depending on position of the multipliedbits, the wires carry different weights, i.e. weight of bitcarrying result of a5b6 is 65.

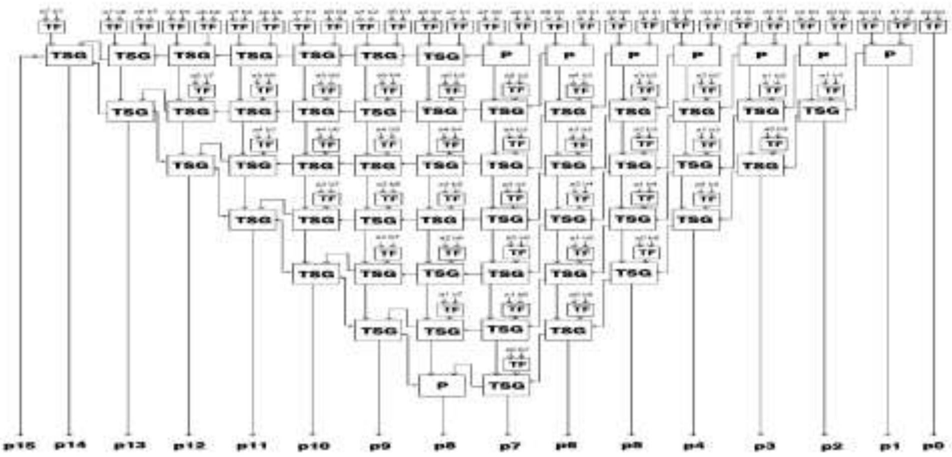

Fig. 9: 8X8 reversible Wallace tree Multiplier

2. The number of partial products is reduced to 2 bylayers of full and half adders.

3. The wires are grouped in two numbers, and addedusing a conventional adder.The circuit diagram of Wallace tree multiplier usingreversible gates is shown in fig. 9. 8bit Wallace tree multipliers were done and the Comparison is as shown in table 2.

Table 2: Comparison of Reversible and Irreversible Wallace Tree Multiplier

Parameter (Virtex5 XC5VLX30 family)	8-bit Reversible Wallace tree multiplier	8-bit Irreversible Wallace tree multiplier	Percentage Improvement For Reversible multiplier
Time delay	9.548ns	11.162ns	14.46%
Power	266.84mW	380.86mW	29.94%
Area(no.of LUTs)	103	117	11.97%

VI. Design Of Control Unit For Gcd Processor

To illustrate the classical and reversible approaches to the Sequential Control Unit Design, reversible logic is employed for a special purpose processor that computes the GCD of two numbers. This GCD processor incorporates standard Euclid’s Algorithm involving Subtract-Compare-Swap operation of two numbers. The basic principle is to subtract smaller of the two numbers repeatedly from the other number until we get the number that divides another

A. Control Unit

Control unit of GCD processor generates the control signals to manipulate the operations in Data-path.Fig. 9: Block diagram of GCD Control Unit.

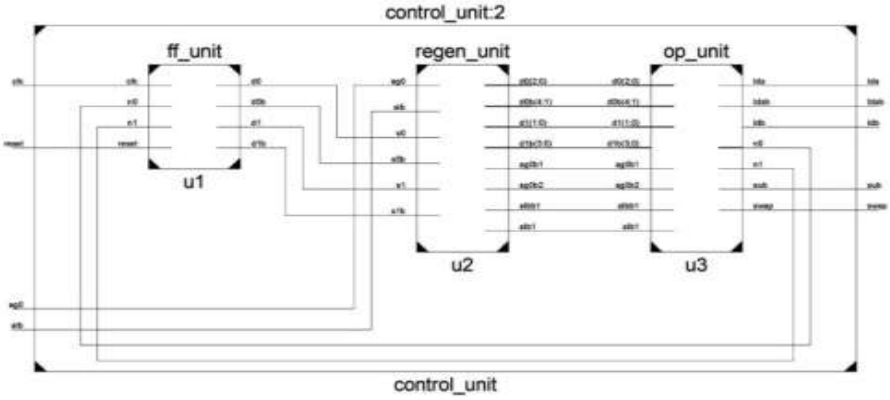

Fig. 10: Block diagram of GCD Control Unit

B. Block Diagram Description:

1) Flip-flop Module:

The control unit for GCD processor requires two Flip-flops as binary state encoding is used for FSM. In this design reversible edge-triggered D Flip-flop is employed for state transitions [7]. Two D-latches are connected in Master-Slave mode to act as an edge-triggered D Flip-flop. Reversible D-latch is designed using Feynman and Fredkin gates .RTL schematic of reversible D flip-flop obtained is shown in fig. 11

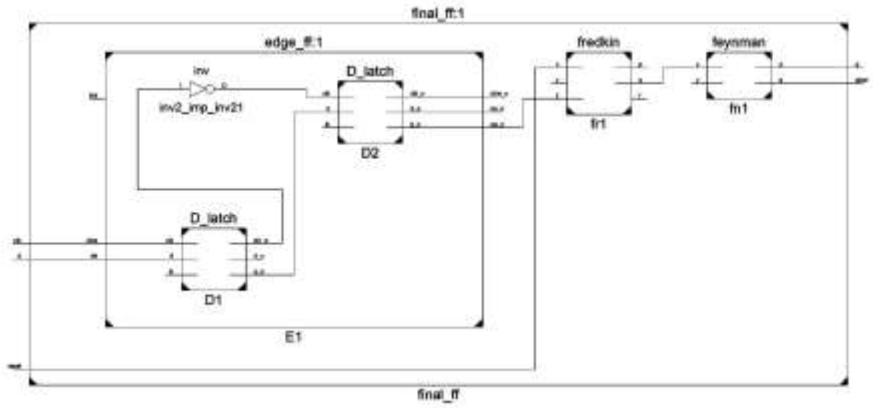

Fig. 11: RTL schematic of Reversible D flip-flop

2) Regeneration Module

To avoid multiple fan-out condition in the design,, it is necessary to duplicate signals used for computation ofoutput and next state. The duplication of input signals isachieved using Feynman gates.

3) Output Module

The computation of the outputs and Next-state signals is done using reversible Fredkin gates. The functioning ofoutput signal is driven by the algorithm.

4. Final RTL schematic:

The complete RTL schematic of GCD control unit isshown in fig. 12.

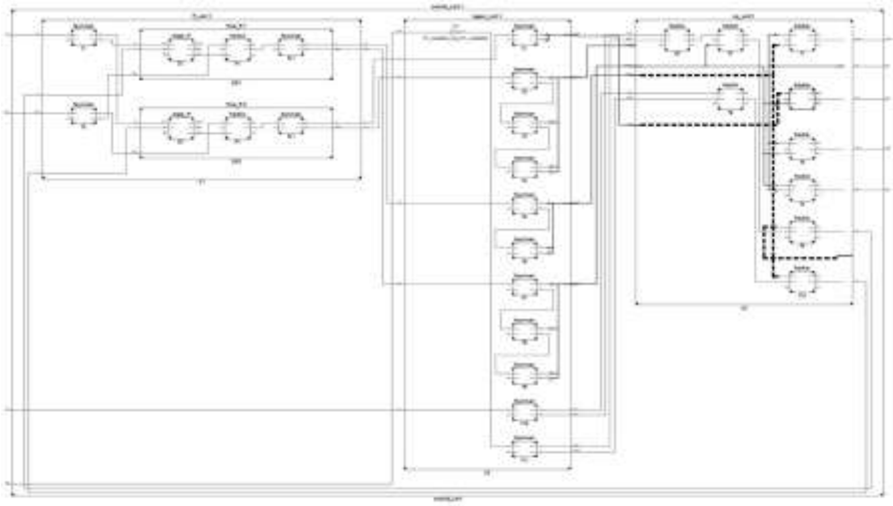

Fig 12: RTL schematic Diagram of GCD Control Unit

5. Speed and power analysis:

Table 3: Comparison of Reversible and Irreversible Control

Parameter (spartan3 xc3s50 family)	Irreversible GCD control unit	Reversible GCD control unit	Percentage Improvement for reversible circuit
Speed(Max Clock freq)	434.33MHz	456.09MHz	5.01%
Power	25.02mW	24.19mW	3.31%

VII. Conclusion

In this paper, it can be seen that the performance of digital circuits can be enhanced using reversible gates and have compared 8-bit ripple carry reversible adder with anirreversible adder in terms of speed and power; there by concluding that reversible designs are faster and power efficient. Furthermore, this concept is extended to combinational circuits such as a Wallace tree multiplier using reversible gates, which were simulated and respective results validate prior interferences. Then a reversible sequential control unit of a GCD processor was designed.Thus, all the designs implemented were compared with their irreversible counterparts, and the speed and power parameters for the reversible designs were observed to have improved significantly.

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