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Low Power Design of Sr Flip Flop Using 45nm Technology

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Abstract:*This paper illustrates the design of low-power, high-performance SR flip-flop. The speedy technical trends are engrossing to decrease the geometrical feature size and power consumption of the integrated circuit in VLSI designs. The proposed design shows the comparison with conventional CMOS circuit on the basis of power consumption and propagation delay and can save up to a significant amount of the power and speed. Therefore proposed design is more optimized than the conventional CMOS design because the efforts have done to use the minimum power during schematic designing. The circuits are simulated at transistor level using Cadence Virtuoso Tool at 45 nm process technology.*

Keywords: *VLSI design SR flip-flop, CMOS technology, power.*

I. Introduction

The relevant choice of flip-flop topologies is an essential step in the design of VLSI integrated circuits for high-speed and high-performance CMOS circuits [1]. Understanding the suitability of flip-flops and selecting the best topology for a given application is an important criterion to fulfill the need of design to satisfy low power and high-performance circuit. In particular, the comparison strategy includes the circuit operation, simulation setup, parasitic estimation, area estimation and power dissipation estimation [2]. An overview of the optimum design strategy is also presented. The Conventional CMOS circuit compared with proposed CMOS circuit using cadence virtuoso tool 45nm technology. And schematic will be the design of both the circuit on the basis of simulation [3].

In this paper cds log window is used as a schematic editor and simulator to verify the architecture of the logic circuit and provides a user-friendly interface for further logic design, simulation, and analysis [4]. The CADENCE allows to work on the layout part of the circuit and gives the analysis of power consumption and other parameters on pressing a single key along with Design Rule Check (DRC).In recent years, with the increase in the frequency of clock and complexity in high-performance VLSI chips, the increase in the power consumption has become the major obstacle to the realization of performance designs [5]. In CMOS, power consumption consists of leakage power and dynamic power includes both switching power and short circuit power [6]. Power consumption has attracted more concern of manufacturer in VLSI circuit design. A flip-flop is a circuit that has two stable states and can be used to store information [7]. A flip-flop also knew as a bistable multi-vibrator when it is used in a finite state machine, the output and next state depend not only on its current input, also on its current input State [8]. It is basically used as a 1-bit data store element, for counting of pulses, and synchronizing variably timed input signals to some reference timing signals[9]. Also in the synchronous system, any error of timing constraints of the flip-flop can cause the overall system to failure [10]. The delay time of a flip-flop is the result of underlying cross-coupled feedback effects. Because of this effect the speed of operation is reduced and an increase in the power dissipation is acquired. So, it is necessary to design memory cells or register circuits achieving high-speed operation while keeping power dissipation to the least level.[11]. In high-performance and low-power applications, power and speed are equally important. The point of optimal energy utilization at a given clock frequency is the point, at which the power-delay product is minimum [12].

II. SR Flip-Flop

The SR flip-flop is the most basic sequential logic circuit known as SR Latch. . The term "Flip-flop" relates to the actual operation of the device, as it can be "flipped" into one logic Set state or "flopped" back into the opposing logic Reset state. This act as the bistable device that has two inputs, one is "SET" meaning the output =1 labeled as S and another is "RESET" meaning the output =0, labeled as R. Hence the SR circuit stands for "Set-Reset".

The reset input sets the flip-flop to its initial state with an output Q that will be either 1 or 0 depending upon set/reset condition. A basic NAND gate SR flip-flop circuit provides feedback from both of its output back to its input in a cross-coupled manner, which is commonly used to store one-bit data.

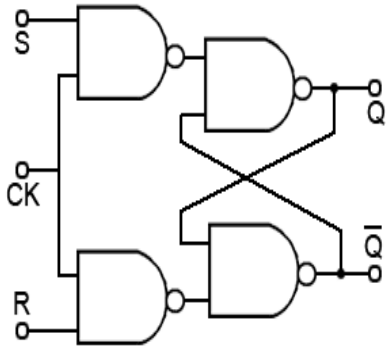

Figure 1: Basic SR flip-flop

Table 1: Truth Table

R	S	Q	Comment
0	0	NC	No Change. Latch remains in present state
0	1	1	SET
1	0	0	RESET
1	1	0	Invalid Condition

When both the inputs are 0 (meaning S = "0" and R = "0") there is no change in output. When S = "1" the output is SET (meaning the output Q = "1") and when R = "1" the output is RESET (meaning the output Q = "0"). The input state of S = "1" and R = "1" is an undesirable or invalid condition and must be avoided.

III. Simulation And Results

In this section comparison of conventional sequential circuits and reduced sequential CMOS circuits has been studied on the basis of power and propagation delay.

The following parameters are taken into account while designing.

Technology	45nm
W(NMOS)	45nm
L(NMOS)	120nm
W(PMOS)	45nm
L(PMOS)	120nm

Table 2: Width (W) and Length (L) for NMOS and PMOS

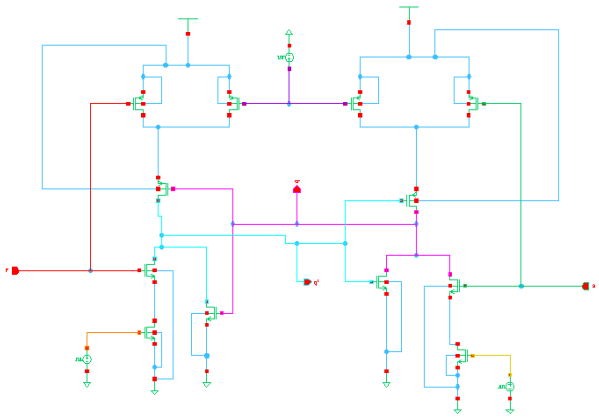

Figure 2: Schematic Design of Proposed Circuit

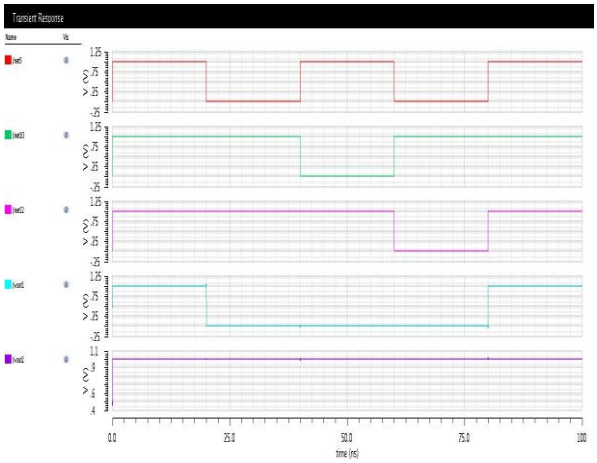

Figure 3: Waveform of Proposed AOI CMOS Circuit

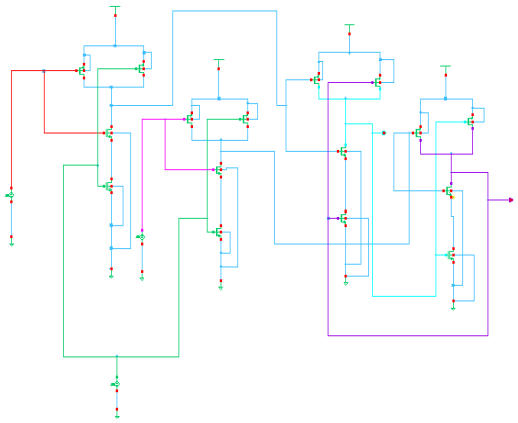

Figure 4: Schematic Design of Conventional CMOS Circuit

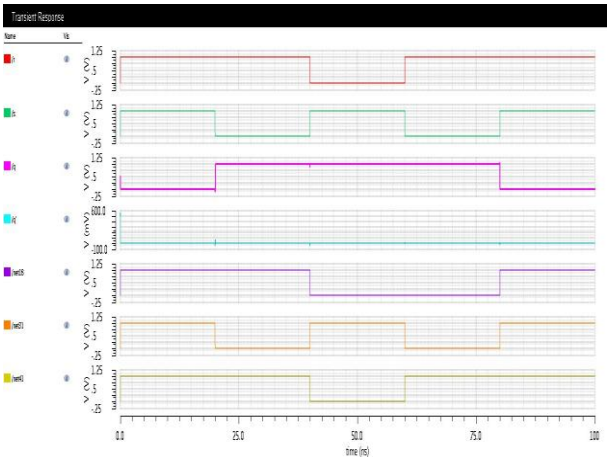

Figure 5: Waveform of Conventional CMOS Circuit

The performance of proposed CMOS circuit is compared with conventional CMOS circuit on the basis some parameters. The performance parameters are Power and propagation delay. From above results, a comparative study can be done between two designing approaches. Table 2 shows comparative analysis.

Circuit	No. of Transistor required	Power Consumption(pw)	Propagation Delay(ps)
Conventional CMOS circuit	16	24.07421	52.457
Proposed CMOS circuit	12	13.3852	21.324

Table 3: Comparative Analysis for Power and Propagation Delay

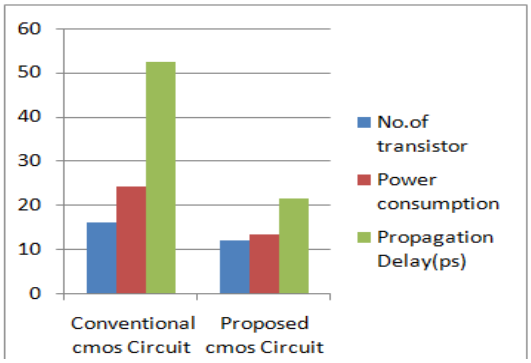

Figure 6

IV. Conclusion

In this work AOI Logic is used for reduction of power dissipation and enhancing the speed of the circuit with no performance degradation. From the comparative analysis result analysis it is clear that the proposed CMOS circuit using AOI logic is more efficient in terms of power and speed. By using this technique, we can reduce both the propagation delay and power consumption up to 60% and 45% respectively. So this design approach can be implemented where power reduction is the primary consideration.

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