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High Speed Level Shifter Design for Low Power Applications Using 45nm Technology

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Abstract : *As the need of handheld devices such as cell phones, speakers, cameras etc., is growing, low power consumption has important design issues for integrated circuits. Level Shifter is an interfacing circuit which can interface low core voltage to high input- output voltage. In order to achieve reduction in power consumption and delay, the proposed level shifter named Single Supply Level Shifter (SSLS) has been designed .In this paper single supply level shifter for low power high speed application have been presented and it shows better performance in terms of power consumption , delay as compared to conventional level shifter . All the circuits are simulated at transistor level using Cadence Virtuoso Tool at 45nm technology with VDD = 1.8V and T = 270 C.*

Keywords : *CMOS, Delay, Level shifter, Power consumption, Single supply level shifter.*

I. Introduction

The most effective and direct way to reduce power dissipation in digital LSIs is to reduce their supply voltage because of their quadratic dependence of the power dissipation on the supply voltage [1]. A level shifter is an interfacing circuit which can interface low core voltage to high input- output voltage. Power dissipation in VLSI circuit consists of dynamic and static power dissipation . Dynamic power dissipation is mainly due to the charging and discharging of the load capacitor. The static power is determined by the leakage current through each VLSI circuits can be reduced by scaling supply voltage and capacitance [2]. For any application, understanding the suitability of circuits and selecting the better topology is an important criterion. The conventional level shifter compared with single supply level shifter using cadence virtuoso tool 45nm technology and schematic will be the design of both the circuit on the basis of simulation.

In this paper, we used cds log window as a schematic editor and simulator to verify the functionality of logic circuits. CADENCE software used for designing the chips and printed circuit boards and gives the analysis of delay, power consumption , area and other parameters along with design Rule Check (DRC). Proposed level shifter and conventional level shifters use two voltage supplies, input voltage supply (Vin) and output voltage supply (Vout) [3]. The conventional level shifter circuits suffer from the contention between the pull up and pull down transistors which leads to the increase in delay and also the power consumption because of the DC leakage path from the power source to ground [4]. The conventional level shifters have disadvantages of delay variation due to different current driving capabilities of transistors, large power consumption and failure at low supply core voltage VddL [5].

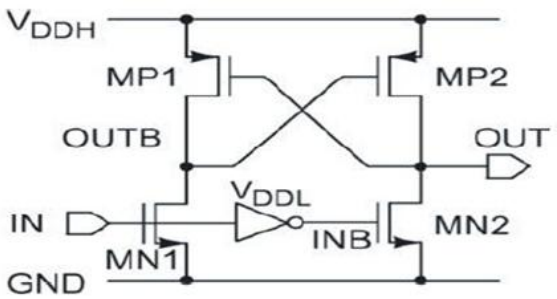


Figure 1: Block diagram of level shifter [5]

Basic Level shifter consists of two pmos transistors MP1 and MP2 act as a cross coupled load, two nmos transistors MN1 and MN2 and two voltages VDDH and VDDL. This paper is organized as follow: Section I gives the introduction of the level shifter, power dissipation in CMOS circuits and overview of single supply level shifter. Section II describes the various level shifter circuits such as conventional level shifter and

single supply level shifter. After that, Section III presents the experimental results and analysis in terms of power consumption and propagation delay. The last Section IV concludes the paper followed by the references.

II. Level Shifter Circuit

2.1 Conventional Level Shifter

The conventional level shifter using cross- coupled PMOS load is shown in Fig. 2. Thick gate oxide transistor was used for MN11, MN12, MP11 and MP12 to overcome high voltage stress. The gate source voltage of MN11 and MN12 supply latching voltage on node T1 and T2. This voltage is used for cross-coupled MP11 and MP12 to positive feedback action which result in fully VddH voltage in node T1. When V_A is low, MN11 and MP12 are turn on and MN12 and MP11 are turn off. At that time if V_A switches to high, following procedure is take place. MN11 off, MN12 on, MP11 on, it results T1 switch low to high and MP12 gets off. Finally the transition time from low voltage to high voltage is decided by the current driving capability of MP11. Pull-down nmos has to overcome the PMOS latch action before the output change state, so the size of MN11 and MN12 are much larger than MP11, MP12 [6].

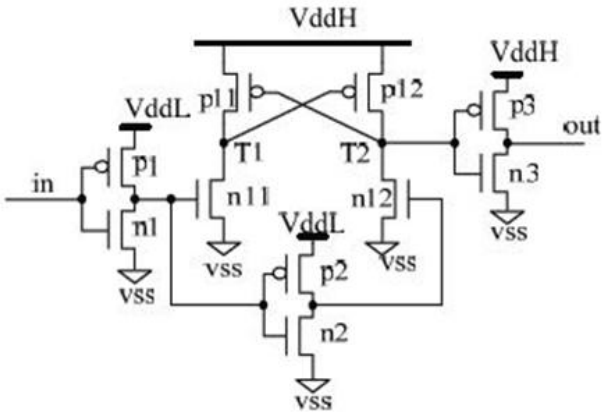


Figure 2: Conventional level shifter [7]

The conventional level shifter has two disadvantages in actual implementation. First, because of the thick gate oxide transistor's (n11, n12) high threshold voltage, it cannot operate at the core voltage VddL under 1V. Second, current driving capability of n11 and n12 are decided by core voltage VddL, but those of p11 and p12 are controlled by the I/O voltage VddH. So when I/O voltage VddH changes, it will make different current driving capability result in delay variation in level shifter. Therefore, it is not adequate for wide range voltage application in a given core voltage [7]. The conventional level shifter has large delay because it suffers from contention between the pull-down transistors (MN1 and MN2) and the pull-up transistors (MP1 and MP2). The contention problem gives rise to the increase in both delay and power consumption. In particular, when the low voltage(VddL) changes, the problem of contention gets severer because we can not get rid of the contention in both cases where VddL is relatively high and low by proper sizing of transistors [8].

2.2 Single Supply Level Shifter

Single level shifter requires only one supply VDDH to convert low voltage signal to the higher voltage has been proposed. The threshold drop across the NMOS MN1 provides a virtual VDDL to the input inverter. The output stage is a half latch which pulls up the input of the inverter to VDDH in order to avoid leakage. The main purpose of designing of schematic diagram of single supply level shifter is to extract lower level from input signal will be high (VDDH), it means MN2 is turned ON and output is pulled to VSS. MN1 will be get higher than VDDH and MN3 will be OFF. Therefore when input is VDDL then output will become VDDH as shown in Fig. 3 [3-9].

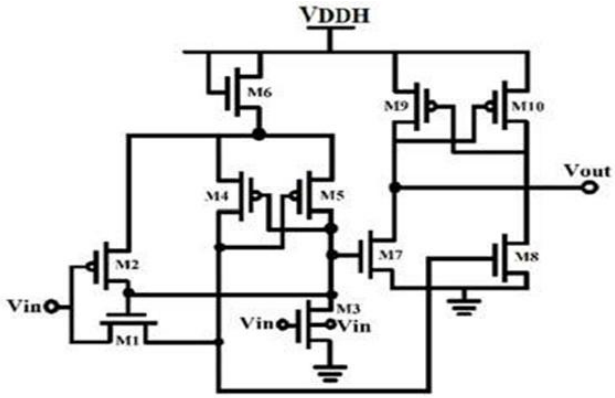


Figure 3: Single supply level shifter [10]

The single supply level shifter allows communication between modules without adding any extra supply pin. Single supply level shifters have advantages over dual supply in terms of pin count, congestion in routing and overall cost of the system. Another benefits of using single supply is flexible placement and routing in physical design. Single supply level shifters dissipate higher leakage power due to increase in leakage currents when input supply level is lower or VddH is higher than input supply level by more than threshold voltage [11].

III. Simulation And Results

In this section as a comparative analysis using 45nm Cadence GPDK technology the conventional level shifter is compared to the single supply level shifter on the basis of power consumption and propagation delay. The availability of high efficiency power supplies and the availability of a multi-VTH CMOS technology are the important factors affecting the optimum supply voltages in a multi-VDD system [12]. Table 1. shows the following parameters are taken into account while designing.

Table 1: Width (W) and Length (L) for NMOS and PMOS

Technology	45nm
W(NMOS)	45nm
L(NMOS)	120nm
W(PMOS)	45nm
L(NMOS)	120nm

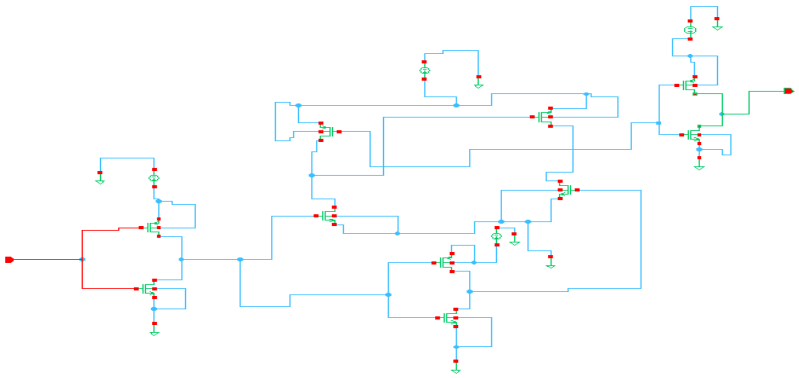


Figure 4: Schematic Design of Conventional level shifter CMOS Circuit

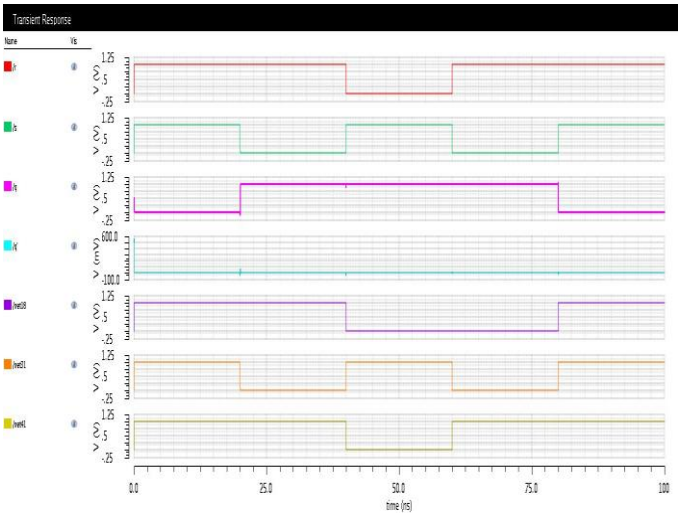


Figure 5: Simulation Waveform of Conventional level shifter CMOS Circuit

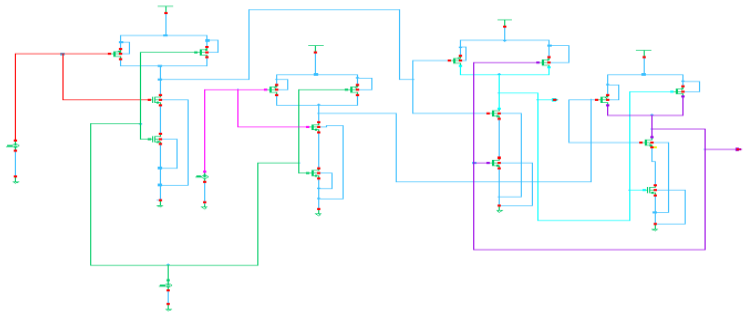


Figure 6: Schematic Design of Single supply Level shifter CMOS Circuit

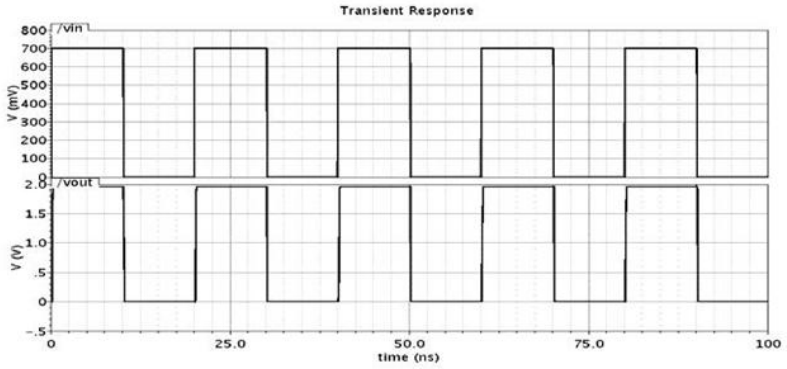
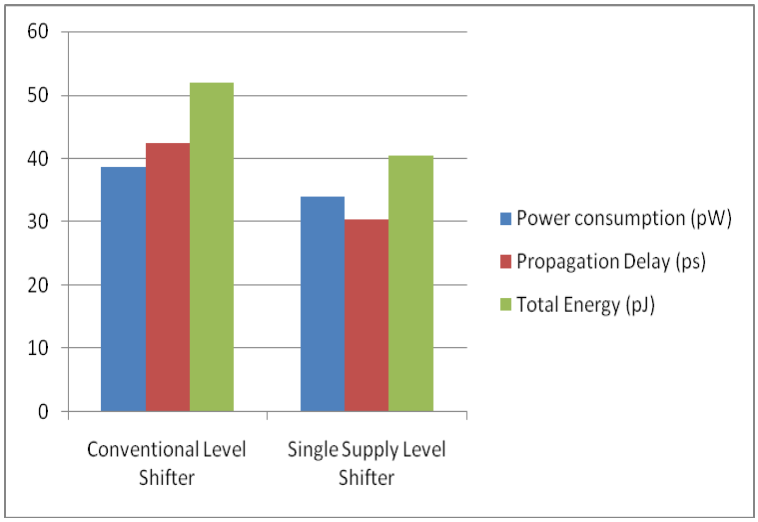


Figure 7: Simulation Waveform of Single supply level shifter CMOS Circuit

From above results, a comparative study can be done between two designing approaches. Table 2 shows comparative analysis on the basis of design parameters such as power consumption , propagation delay and total energy

Table 2: Level Shifter Design Parameters Analysis

Level shifter Configurations	**Power Consumption (pw)**	**Propagation Delay (ps)**	**Total Energy (pJ)**
Conventional level shifter	38.567	42.425	52
Single level shifter	33.864	30.385	40.5



Graph 1: Graphical representation of Level Shifter Circuits

IV. Conclusion

In this paper, two level shifters namely Conventional Level Shifter and Single Supply Level Shifter are proposed and evaluated in terms of power and delay performance. The design of level shifter circuits is simulated with a 45nm CMOS technology. Conventional level shifter has power consumption of 38.567pw and delay of 42.425ps. Single supply level shifter has power consumption of 33.864pw and delay of 30.385ps. As a result, by using single supply level shifter we can reduced power and delay upto 45% and 50% respectively. This improves overall performance of system by reducing complexity and cost of system.

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