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Designing and Simulation of High- k , N-channel MOSFET devices using Tina Pro

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***Abstract**: This paper focuses on the development of 80nm channel length of high-k (TiO_2) n-channel (NMOS) and p-channel (PMOS) enhancement mode MOSFETs which emerged due to replacement of SiO_2 by high-k (TiO_2) MOSFETS, as there were many problems while using SiO_2 like high leakage current, short channel and electron tunneling effect.*

***Keywords**: Simulation of the fabrication process was carried out by using Tina Pro Software to obtain more accurate process parameters & the results were then compared with NMOS using SiO_2 as gate dielectric.*

I. INTRODUCTION

Here we will be discussing about the role of gate dielectric in (MOSFET) devices, and their criteria for the selection of high-k materials. Furthermore, materials preferred for gate dielectrics both high-k & low-k materials. So, to start with gate dielectrics which is the one used between its gate and substrate. When any metal and a semiconductor or any dielectrics form an interface, charge transfer takes place across the interface. In state-of-the-art processes, the gate dielectric is subjected to its important role, including [6]:

a) Interface to the substrate is electrically cleaned.
b) High capacitance is required to increase the trans- conductance of MOSFET device.
c) To avoid dielectric breakdown and leakage due to quantum tunneling, high thickness of channel is required.

The capacitance and thickness constraints directly oppose each other. For silicon based substrate MOSFETs, the gate dielectric considered is SiO_2 as it offers high impedance. As we know thermal oxide has a very clean interface [6].

MOSFETs are backbone of the integrated-circuit industry till date. The reason behind is the perfection of the SiO2/Si interface. As MOSFET dimensions have scaled, correspondingly larger values of the oxide capacitance (Cox) are required. The oxide capacitance is mandatory for inverting the surface to a sufficient sheet charge density in order get the desired current for the particular given supply voltage and for avoiding short channel behavior [6].

Here some of the defects are formed in the gate oxide at the SiO2/Si interface due to flow of charge carriers. The solution to this can be an insulator with higher dielectric constant whose properties can be dependent on the material as well as on the processing technology. Initial high-k dielectric was TiO_2 and later on other dielectrics were introduced by many researchers like Al_2O_3, ZrO_2, Ta_2O_5, HfO_2, $ZrSi_xO_y$, Y_2O_3, Ya_2O_3 for submicron MOSFET [5].

II. CRITERIA FOR SELECTION OF GATE DIELECTRIC

As silicon dioxide (SiO_2) has excellent dielectric properties that lead to the evolution of microelectronics during the past decades.[5] Due to reduction in feature size integrated circuit performance has been improved, but there are some disadvantages due to scaling factor. So, there emerged a need for high dielectric constant rather than using SiO_2.

III. Materials Selected For Gate Dielectric

Based on strength of material dielectric is divided in two categories namely: Low-k and High-k.

A. LOW-k

A low-k as the name specifies the one with small dielectric constant. Although there is availability of large number of materials with lower dielectric constants but in terms of integrity to a manufacturing process only some of them are suitable. So, efforts have been made in direction of these classes of materials [2]. Some of these materials are defined below:

a) Fluorine-doped Silicon Dioxide

Here, SiO_2 doping is done with fluorine in order to generate fluorinated silica glass, dielectric constant range is from 3.9 to 3.5 [1].

b) Carbon-doped Silicon dioxide

Here, doping of SiO_2 with carbon is done, dielectric constant is 3.0 [5].

c) Porous Silicon dioxide

Different methods are applied for creating larger voids or pores in SiO_2 dielectric. Voids may have a dielectric constant of approximately 1, so the dielectric constant of the porous material can be reduced by raising the porosity of the film.

d) Porous Carbon-doped Silicon dioxide

By UV curing method, methyl groups in carbon doped silicon dioxide can be removed and pores can be defined to the carbon doped silicon dioxide low-k materials [4].

B. High-k

The term high-k dielectric defines a material with a high dielectric constant k that will allow increase in gate capacitance without the associated leakage effects. Such dielectric constants are defined below:

a) Aluminum oxide (Al_2O_3)

This material has following characteristics like high permittivity, high band gap, high band discontinuities, and good break down voltage. But the main problem is that the high processing temperatures (1000^oC) the mobility of electrons shows a flat band voltage shift in the positive direction.

b) Titanium dioxide (TiO_2)

This is an alternative gate dielectric material suitable for deep submicron MOSFET applications. It is advantageous too as it has dielectric constant of 80, bandgap as 3.5eV for amorphous films and 3.2 eV for crystalline films which are good for acting as an insulator.

c) Zirconium oxide (ZrO_2)

ZrO_2 is referred due to its dielectric constant (k~25) higher band gap (~5.8eV). It is thermodynamically stable with Si, but crystallization temperature is about 500^oC, which is low for ULSI processing.

Gate Dielectric Material	Dielectric constant (k)	Energy Band Gap Eg (eV)	Conduction Band Offset ΔEc (eV)	Valence Band Offset ΔEc (eV)
SiO_2	3.9	9	3.5	4.4
Al_2O_3	8	8.8	3	4.7
TiO_2	80	3.5	1.1	1.3
ZrO_2	25	5.8	1.4	3.3
HfO_2	25	5.8	1.4	3.3
Ta_2O_5	25	6	1.5	3.4
Y_2O_3	13	6	2.3	2.6
Ya_2O_3	27	4.3	2.3	0.9

Table 1: High-k dielectric materials and their properties

IV. Role Of Simulation Software

TINA is an acronym of "Toolkit for Interactive Network Analysis". TINA Design Suite is a powerful and affordable circuit simulator and PCB design software package for analyzing, designing, and real time testing of analog, digital, HDL, MCU, and mixed electronic circuits and their PCB layouts. It also analyzes SMPS, RF, communication, and opto-electronic circuits which generate and debug MCU code using the integrated flowchart tool and also test microcontroller applications in a mixed circuit environment. A unique feature of TINA is that it can bring the circuit to run with the optional USB controlled TINA Lab II and Lab Xplorer hardware, which turns the computer into a powerful, multifunction T&M instrument.

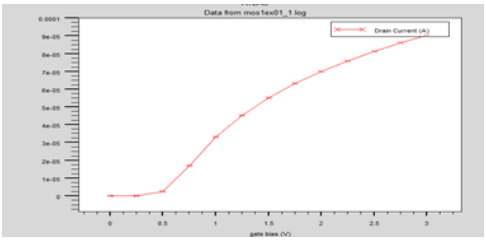
V. Simulation Results

Simulations of the both high-k devices (NMOS and PMOS) are done by using Tina Pro. Device simulation is done for calculating the electrical behavior of semiconductor devices. It also helps in calculating some of the design parameters such as sheet resistance, channel surface concentration, gate oxide thickness.

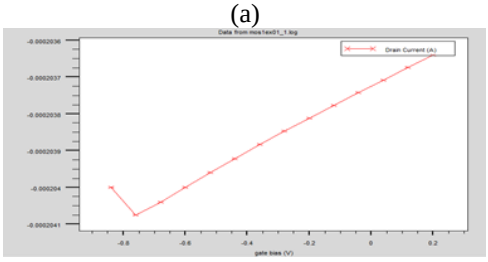
a. Determination of Threshold voltage

Threshold voltage is the one which determines the requirements for turning the transistor on or off. According to the simulation results, the threshold voltage for NMOS with TiO2 is around to -0.74V while for

NMOS with SiO2,V_t is equal to 0.23V and for PMOS with TiO2, V_t is equal to -0.24V. Figure shows the I_d-V_g characteristics for the transistors with V_t.



(a)



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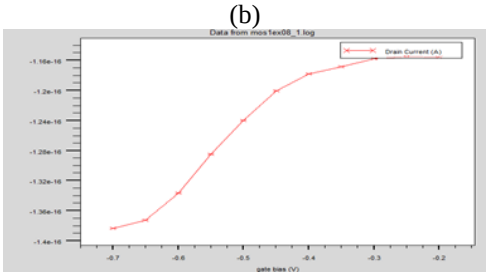
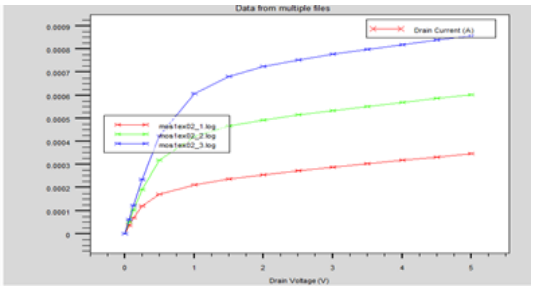


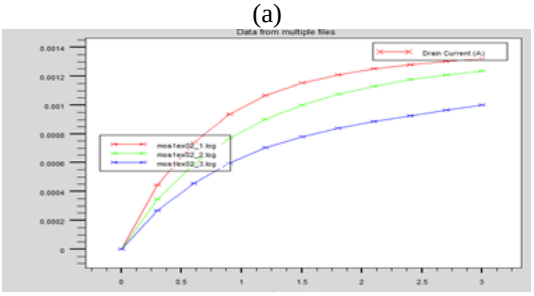
(c)

Figure2: The I_d-V_g curve for (a) NMOS with SiO_2 as gate dielectric (b) NMOS with TiO_2 as gate dielectric and (c) PMOS with TiO_2 as gate dielectric; obtained from Tina Pro simulator.

b. MOSFET V-I Characteristics



(a)



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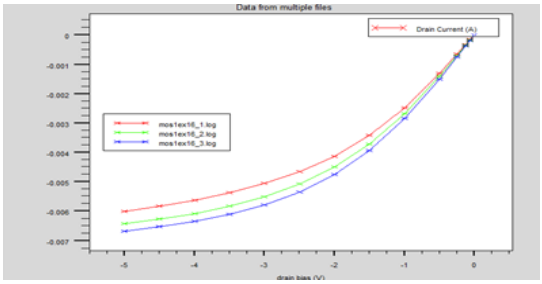
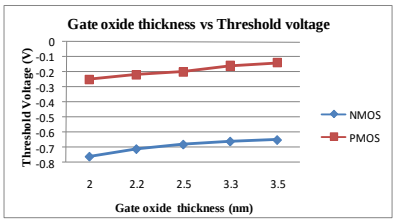


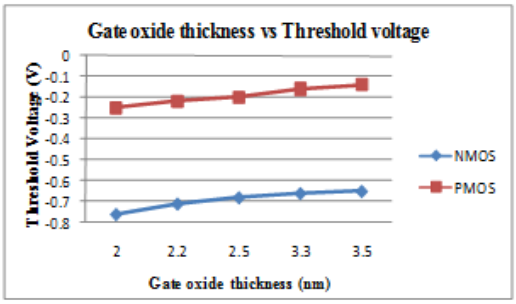
(c)

Figure 3: Family of I_d vs. V_{gs} curve for (a) NMOS with SiO_2 as gate dielectric (b) NMOS with TiO_2 as gate dielectric and (c) PMOS with TiO_2 as gate dielectric; obtained from Tina Pro simulator.

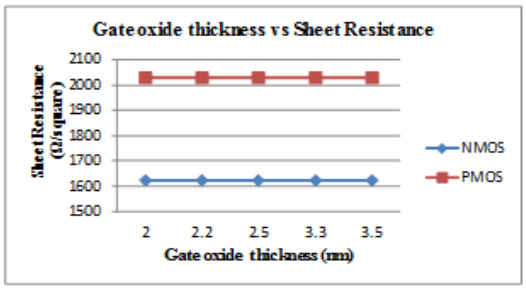
c. Effect of Drain Voltage and Threshold Voltage



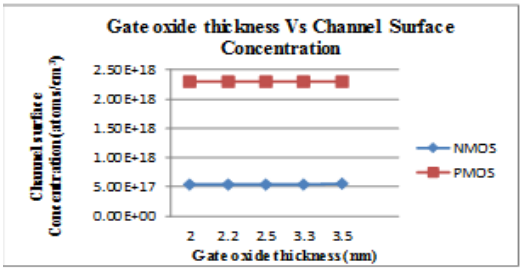
d. Effect of gate oxide thickness on device parameters like Threshold voltage, Sheet resistance and Channel Surface concentration.



(a)



(b)



(c)

FIG 4: EFFECT OF GATE OXIDE THICKNESS ON DEVICE PARAMETERS (A) THRESHOLD VOLTAGE (B) SHEET RESISTANCE (C) CHANNEL SURFACE CONCENTRATION

E. EFFECT OF HIGH-K ON THRESHOLD VOLTAGE

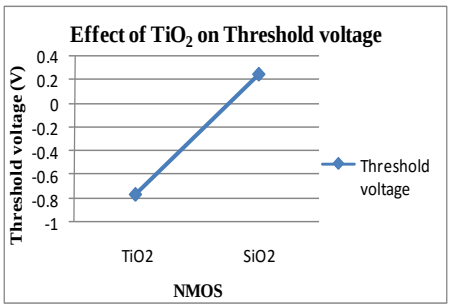


Fig 5: Effect of High-k on Threshold voltage

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