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Comparative Analysis of Gate Diffusion Input Based Full Adder

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Abstract : *Adder forms the basis of many processing operations making it one of the most important components in ALU design. Improving its performance can enhance the performance of the overall processing system. In this paper a full adder design is presented using GDI technique. The main objective is to get reduced delay and power consumption. In the presented design delay and power consumption is calculated and further compared to full adder conventional design logic. Overall comparison is done in terms of time delay, power consumption and number of transistors used. The power consumption is approximately reduced to 25% while the time delay is approximately reduced to 50%, making an effective and efficient full adder logic design. Implementation of the design is done using schematic editor and the simulation is done in Cadence environment at 45nm CMOS process technology.*
Keywords: *GDI, CMOS, full adder, time delay, power consumption.*

I. Introduction

The basic building blocks in the arithmetic unit of any digital signal processor or application specific integrated circuits are full adder. Portability being the main issue and the increasing demand of consumers in today's technical era. Rating and demand of these devices depends upon speed, small silicon area, longer sustainability and reliability. Enhancing the performance abilities of basic Full Adder unit can enhance the performance of overall arithmetic unit and thus improving the complete system. Key limitations being speed and power consumption in various electronic devices, focus should be on improving these parameters [1, 2]. Conventional CMOS design of full adder is presented. CMOS full adder contains a total of 15 PMOS and 15 NMOS transistors to generate output at switch level design. All the PMOS and NMOS transistors used are having same W/L ratio. The parameters of transistors should be adjusted individually to obtain optimized results in time domain [3].

Addition operation of 3 input bits is performed by full adder. Full adder basically consists of three inputs and two outputs. The input variables or bits are having two unknown values and the third input bit is an input carry bit which has been taken into account due to some previously existing or rather previously performed addition operations. The two output variables are expressed by sum and output carry. Sum being the result of addition operation and carry being the generated bit which will act as input carry for the next addition operation [4- 7]. Fig. 1 shows the gate level logic diagram of Full Adder.

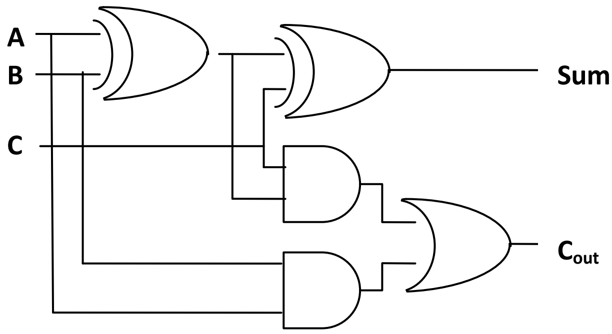

Fig. 1. Gate level logic of Full Adder Circuit

Relation between inputs A, B and C_{in}, where C_{in} is the input carry, and outputs Sum and C_{out}, where C_{out} is the output carry, is expressed by the following relations given by equation (1) and (2).

$$Sum = A \oplus B \oplus C \quad (1)$$

$$C_{out} = (A \cdot B) + (B \cdot C_{in}) + (A \cdot C_{in}) \quad (2)$$

The truth table of full adder is shown with the help of Table 1.This truth table comprises of Sum and Carry (C_{out}), which are the main adder operations. In this the significant input is C_{in} which is the carry propagated from previous addition operation. Investigation of different logic styles can be done from different point of view. Eventually, one performance aspect is favored at the cost of other performance aspects. It can also be said that, application specific design constraints can be favored and has its place in cell library development. This could further be told as, logic design suited for one function may not be appropriate for another one [8-11]. For example, static approach presents robustness against noise effects, so automatically provides a reliable operation. So the issue related to ease of design cannot be resolved easily.

Table 1: Truth Table of Full Adder

A	**B**	C_{in}	**Sum**	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Thus, important measures should be taken while designing a static logic style for realizing a specific logic function [12, 13].

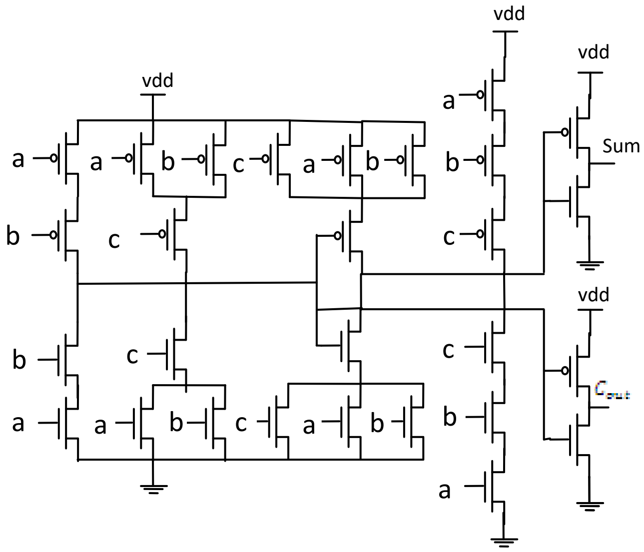

Fig. 2. Conventional Full Adder

Fig. 2 shows a conventional full adder design. A Complementary CMOS full adder design with 28 transistors is shown. It is formed by the combination of PMOS pull up transistors and NMOS pull down transistors. Robustness and Scalability are one of the important features of full adder. The complementary MOS logic circuit has the major advantage of layout regularity and that of the stability, which is at low voltage due to the complementary transistor pairs and smaller number of interconnecting wires or routers. But its power consumption and transistor count are relatively high, which in this case is 30, for low power arithmetic circuits. Other circuits can also be designed using less number of transistors depending upon different area of implementation [14-16].

II. Design Logics

(i) Gate Diffusion Input (GDI) based Full Adder

The basic description of GDI cell consisting of two transistor network is shown in fig. 3. N,G and P being the three inputs. The source terminal of NMOS is acting as one input terminal and source terminal of PMOS is acting as another input terminal. The output is taken from the drain terminal of both the transistors. The supply and ground are connected to the bulk of PMOS and NMOS respectively as shown in fig. 3.

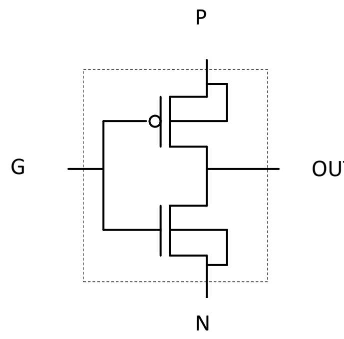

Fig. 3. Basic GDI Cell

The PMOS will produce its output as strong logic 1 and weak logic 0. Similarly the NMOS produces its output as strong logic 0 and weak logic 1. When G is 1 then the nmos is turned ON and the N input passes to the output. Similarly when G is set as 0 then the pmos is turned ON and the P input passes as output through pmos. If NMOS is switched, the N input passes through the nmos transistor and if the input N is at logic 1 then the output will be weak logic 1. Similarly if the PMOS is turned ON then if the P input terminal is at logic 0 then the output is weak logic 0. The main disadvantage of using GDI cell is that it produces degraded output.

A GDI Based Full Adder design is implemented in this paper, which is obtained for getting reduced time delay and reduced power consumption. The Sum bit is obtained from output of the second stage of XOR circuit while the Carry bit (Cout) is calculated by multiplexing operation of B and Cin, which is controlled by (A XNOR B) operation. All of these features give the GDI cell two additional input pins to use which makes it significantly flexible than conventional full adder CMOS design. The advantage of this genius design is that it is very power efficient without using much number of transistor counts. One of the major disadvantages of a GDI cell based design is that it requires twin-well CMOS or silicon on insulator (SOI) process to realize the switch level design, which gives degraded output. Thus, the GDI chip is more expensive to design and implement. In addition to this problem, if standard p-well CMOS process is used, the GDI faces a problem of lacking driving capability which leads to more expensive and more complex design to be realized on the chip.

(ii) Conventionally designed full adder

A conventionally designed full adder is having a basic full adder design. This full adder is having three inputs and two outputs. Here two inputs are new bits and third input is a previous carry input, summed together to generate a new carry and sum value. The full adder here is implemented using two half adder logics. Besides using two half adders it is also using an OR logic to completely design a Full adder CMOS design.

III. Schematic Designs

(i) Gate Diffusion Input (GDI) design schematic

In this paper implementation of full adder is done using GDI cell based design, as shown in fig.4. This full adder is designed using 10 transistor logic as shown in fig.4. The three inputs are represented by A, B and C. The output of the full adder design is represented by sum and Cout. Consider an instant where the input A, B and C are changing from 010 to 000.

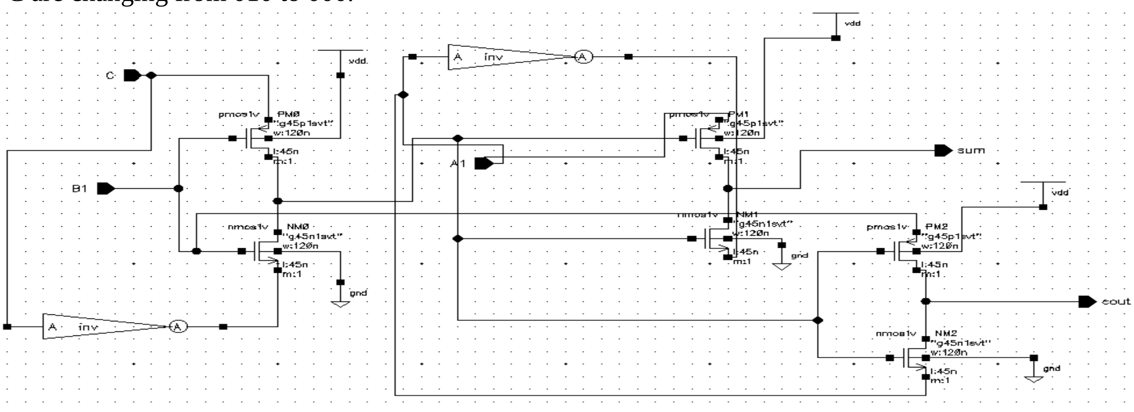

Fig. 4. GDI based Full Adder Design Schematic

In that case the output should result in logic 1 to logic 0 at the sum output. But as discussed earlier the output resulted out of inputs 010 are degraded in form, which acts as minimal voltage for the next stage resulting in a weak logic 0 at the output when the inputs A, B and C changed to 000 respectively. The schematic of inverter used in GDI based full adder is shown in fig. 5.

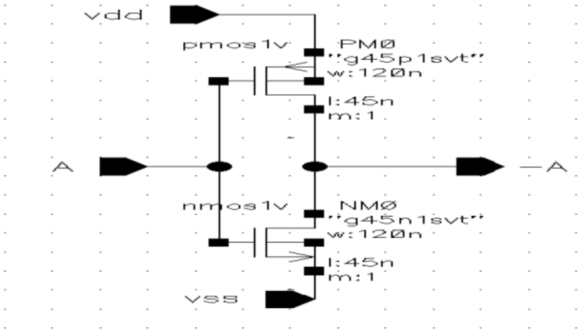

Fig. 5. Inverter circuit used in GDI based Full Adder Design Schematic

(ii) Conventionally designed Full Adder Schematic

The design schematic of full adder design using two half adders and one OR gate is shown below. This design is using a total of 30 transistor counts. The design schematic of conventiall full adder design is shown below in figure 6. Internal schematic of half adder and OR gate is shown in fig. 7 and 8 respectively.

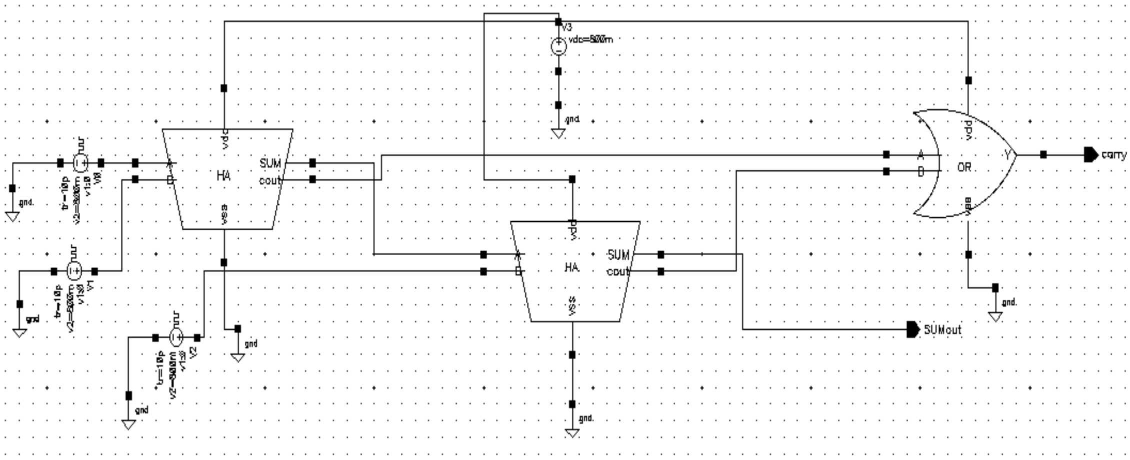

Fig. 6. Conventional Full Adder Design Schematic

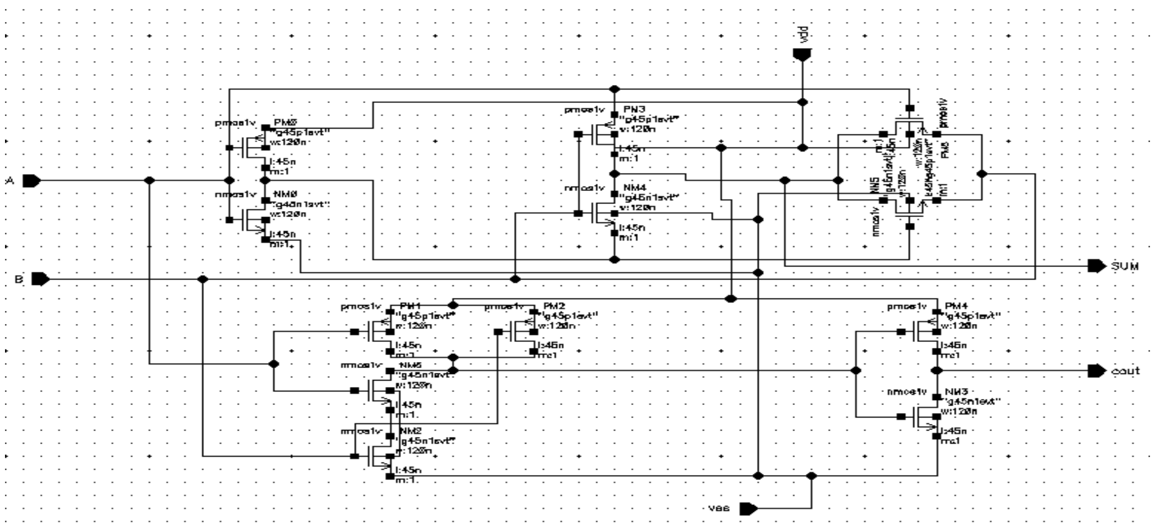

Fig. 7 . Half Adder Design Schematic

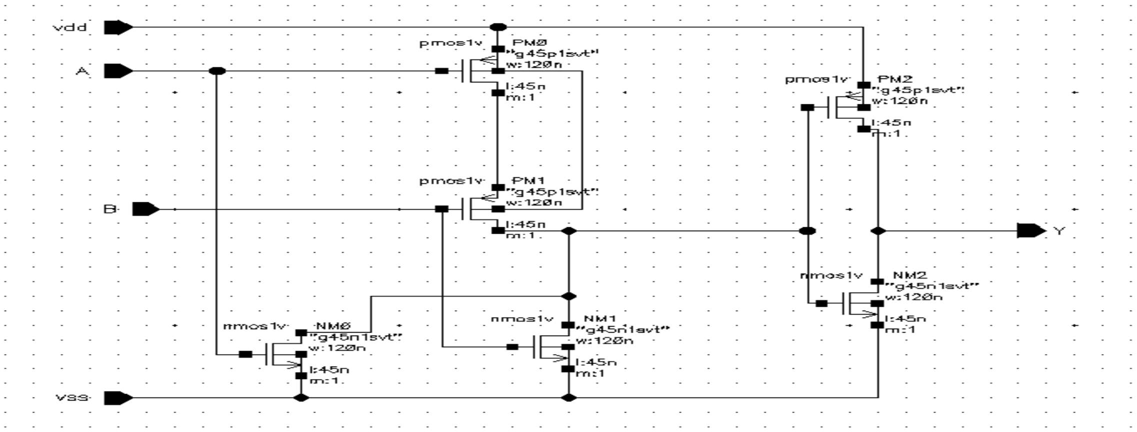

Fig. 8. OR gate Design Schematic

IV. Result & Analysis

The analysis of the full adder is done using the GDI (Gate Diffusion Input) technique in CADENCE environment. The schematic is constructed using 45nm technology. The logic output for the full adder designed using GDI technique is obtained. The designed schematic is compared with the conventional CMOS Full Adder design logic cell. The corresponding design schematic waveform for the conventional CMOS based Full Adder is as shown below in figure 9 & 10.

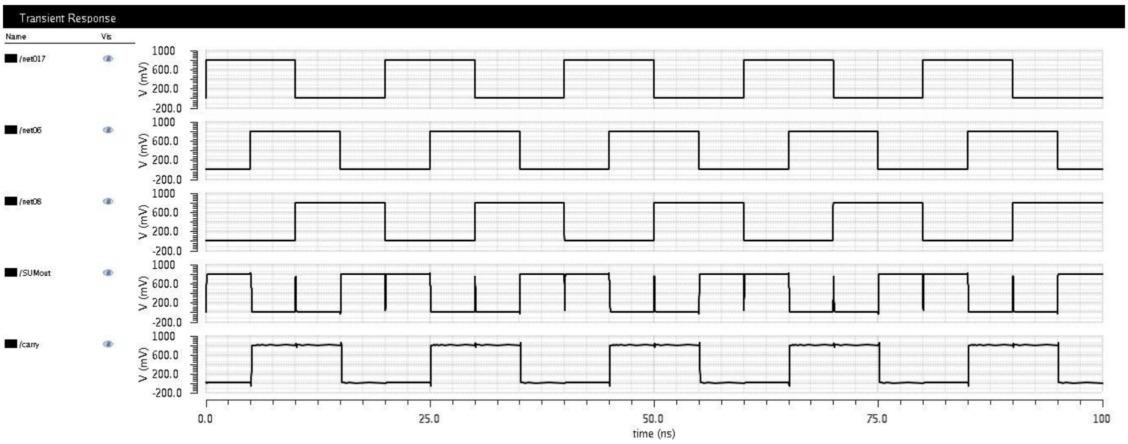

Fig. 9. Output Waveform of Conventional Full Adder

The GDI waveform is compared in sense of delay and power consumptions with the conventional design and the results are shown in figure 9 & 10.

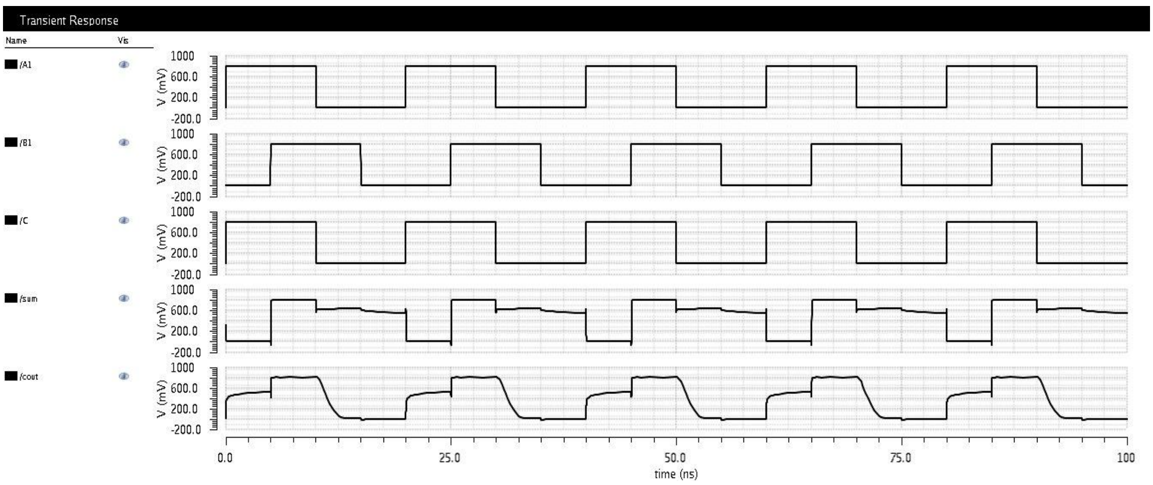

Fig. 10. Output waveform of GDI Based full adder design.

Both the adders are designed and compared using the power consumed in the circuit and the delay produced in the device during the simulation phase. The results obtained are as shown below in the Table 2.

Table 2: Parameter Comparison for Full Adder.

Parameter	Conventional design	GDI design
Power consumption	24.146nW	6.1176nW
Delay	110.0ns	55.38ns
Transistor Count	30	10

It can apparently be seen from the above table and waveforms that the time delay obtained at the rising edge of sum and selected input, in case of conventional full adder design logic, is 110.0ns, which is significantly greater than that obtained for GDI based full adder design given by 55.38ns. Also the power consumption, obtained as 6.1176nW, is apparently low in GDI based full adder design as compared to conventional full adder design, given by 24.146nW.

V. Conclusion

In this paper two types of full adder logic designs are implemented, stimulated, analyzed and compared. Using a conventional form of full adder an a GDI based full adder. From the analysis done in table 2. It is very clear that the power consumption in GDI based full adder design is approximately quarter value of conventional full adder design, which is a significant difference in results, providing a low power full adder design. The GDI based design is having a total power consumption of 6.1176pW, where as the conventional full adder design is having a power consumption of 24.146pW. The time delay obtained from the analysis is also reduced to approximately half of its value then the time delay provided by conventional design. The GDI based design logic is having a delay of 55.38ps which is half of the delay produced by conventional full adder 110.0ps. Hence the GDI based full adder design is improved in performance from the conventional design.

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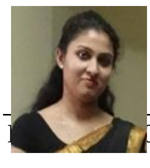

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