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# Bit Error Measurement of Digital Modulation Schemes Using FPGA for Software Defined Radio

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***Abstract:*** *Nowadays, we hardly find any field which is not advancing rapidly, modern communication systems are also advancing at a faster rate. So it is mandatory we must design the techniques to evaluate the performance of such modern communication systems like Software Defined Radio (SDR), Cognitive Radio using reconfigurable devices like FPGA. This paper presents the technique for the performance measurement of digital modulation schemes since the digital modulation schemes are superior as compared to analogue modulation schemes. The performance characteristics like bit error rate(BER), SNR, SNDR can be used to evaluate the performance of digital modulation techniques. Bit error rate (BER) is the principle measure of performance of a data transmission link. The system will be able to measure the performance of more than one modulation scheme. This paper presents the results of BER for digital modulation schemes;Verilog HDL is used to implement the proposed techniques. And MATLAB is used to display the final results of BER versus different values of SNR.*

***Keyword****: Bit Error Rate (BER), signal to noise ratio (SNR),signal to noise and distortion ratio (SNDR), software defined radio (SDR), field programmable gate array (FPGA).*

## I. Introduction

Thewireless system development using the latest communication techniques is increasingly limited by the design productivity. It is critical to verify the design characteristics at the earliest possible stage of design to minimize costly design iterations. At the physical (PHY) layer, the bit error rate (BER) performance metric is widely used to measure the reliability of the communication systems. Monte Carlo (MC) simulation techniques have been widely used to generate BER versus a range of expected signal-to-noise ratio (SNR) conditions. However, the execution times of software-based MC simulations of the baseband layer on workstations can be extremely long, especially for increasingly complex communication systems [1]. Another method to measure the BER is the Bit Error Rate Tester (BERT) very costly which costs more than 8lakhs to 10lakhs as well as it will require more power for its operation. Fig. 1 shows the comparison of the BERT and the FPGA board which has been used in the proposed design.

Digital modulation technology is an important content of modern communication. Modulation is essential in

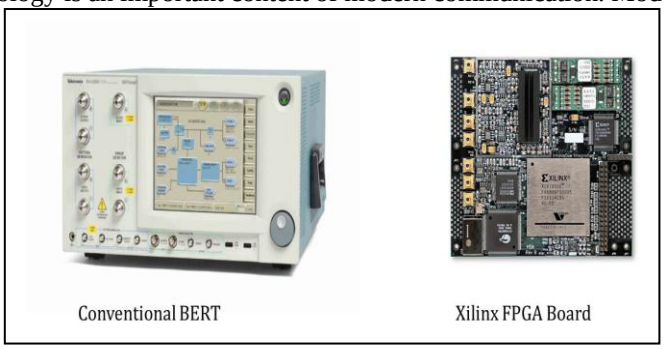


Fig. 1 Comparison of BERT and FPGA Board

transmitting two or more signals in the same time because it avoids interference between the signals and also ensure that errors are avoided during transmission. In order to transmit the digital information is as a series of ones (1) and zeros (0) over long distances, different modulation schemes are used which are Binary Phase Shift Keying (BPSK), Binary Amplitude Shift Keying (BASK), Frequency Shift Keying (BFSK), Quadrature Phase Shift Keying (QPSK). The bit error rate (BER) performance metric is widely used to measure the reliability of the communication systems.Bit error rate (BER) is the ratio between the numbers of error bits received to the total number of bits received. The design of an all-digital, binary-phase-shift-keying (BPSK)

demodulator is described, the project details the design of the components (e.g., Booth multipliers and pseudorandom noise (PN) generators) and the simulation of the entire system [2].

The rest of this paper is organized as follows. Section IIbriefly presents the different digital modulation schemes. Section III presents the implementation BER measurement process. Sections IV gives methodology usedand V presents the experimental results and VI gives applications of system. Finally, Section VII makes some concludingremarks with section VII discussing future scopes for the system.

## II. Different Digital Modulation Schemes

*A. Binary Phase Shift Keying*

In a BPSK, the phase of the sinusoidal carrier signal is changed according to the message while keeping the amplitude and frequency constant (Fig. 2).

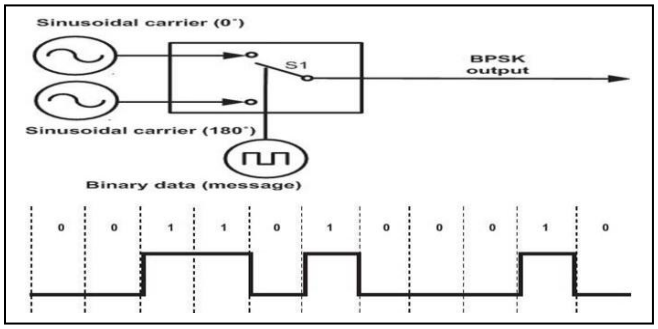


Fig. 2 Basic circuit and waveform of BPSK Modulation

*B. Binary Amplitude Shift Keying*

In a Binary Amplitude-Shift keying, the amplitude of the sinusoidal carrier signal is changed according to the message level, while keeping the frequency and phase constant (Fig. 3).

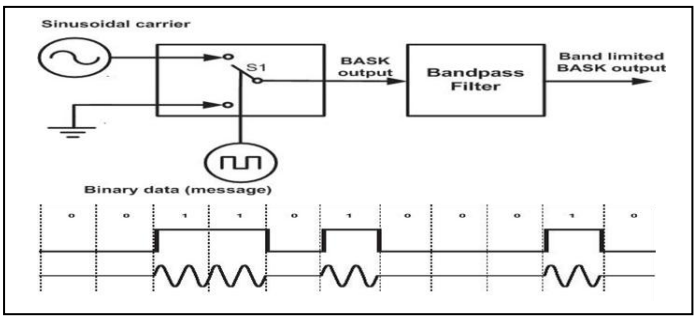


Fig. 3 Basic circuit and waveform of BASK Modulation

*C. Binary Frequency Shift Keying*

In a BFSK modulation process, the frequency of the sinusoidal carrier signal is changed according to the message level. It keeps the amplitude and phase constant (Fig. 4).

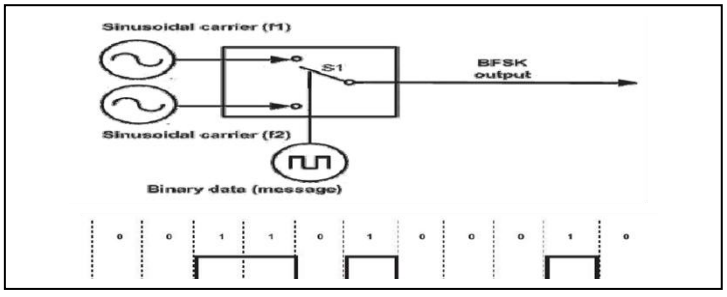


Fig. 4 Basic circuit and waveform of BFSK Modulation

## III. Implementation of Ber Measurement Process

The proposed system is having the modulator and demodulator for the digital modulation schemes which are implemented using Verilog Hardware Description Language. The simulation of the BER calculation is done using the MATLAB software. For verification and synthesis of the Verilog codes of modulation schemes XILINX ISE Simulator has been used. The implementation of this synthesized code has been done on Spartan3 FPGA hardware kit.

## IV. Methodology Used

The following steps are used for the implementation of the overall system. Fig. 5 gives the flowchart of the system.

1. START.
2. Generate the input/modulating signal i.e. random data stream using PRPG.
3. Generate the carrier waveforms.
4. Modulate the modulating signal with carrier wave.
5. Add the noise in the output of modulator block.
6. Demodulate the signal obtained after adding the noise.
7. Measure the BER of the output signal of the demodulator.
8. Display the final results of BER graphically.
9. STOP.

## V. Results

The results of work done are given in this section. The RTL schematic for BASK modulation is shown in Fig. 6with device utilization for the same is shown in Fig. 7.Technology schematic for BASK is represented in Fig. 8.The RTL schematic for BPSK modulation is shown in Fig. 9 with device utilization for the same shown in Fig. 10. Technology schematic for BPSK is represented in Fig. 11.The RTL schematic for QPSK modulation is shown in Fig. 12 with device utilization for the same shown in Fig. 13. Technology schematic for QPSK is represented in Fig. 14.Simulation results for BER of BPSK modulation are presented in fig. 15.Simulation results for BER of QPSK modulation are presented in fig. 16.

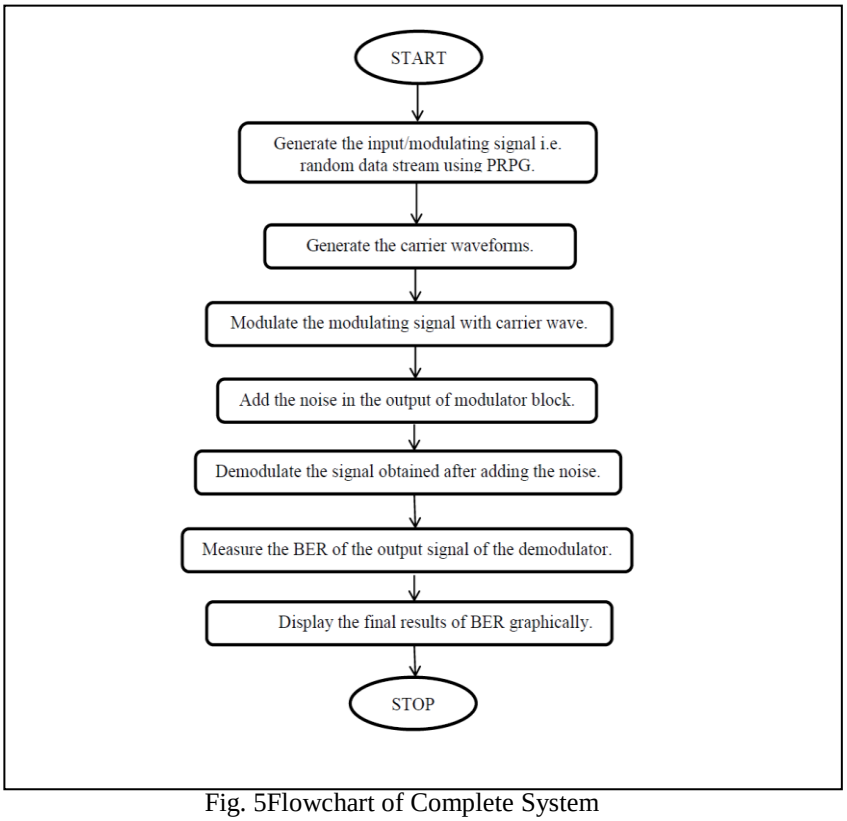


Fig. 5Flowchart of Complete System

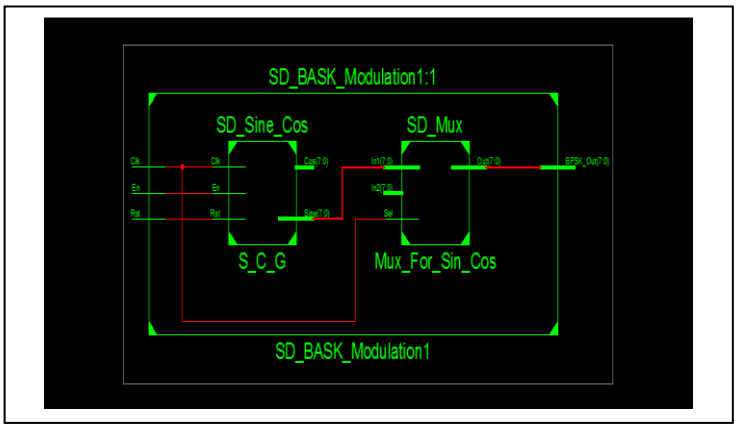


Fig. 6RTL schematic for BASK modulation

| Device Utilization Summary | | | | |
|---|---|---|---|---|
| **Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** |
| Number of Slice Flip Flops | 16 | 3,840 | 1% | |
| Number of 4 input LUTs | 32 | 3,840 | 1% | |
| Number of occupied Slices | 16 | 1,920 | 1% | |
| Number of Slices containing only related logic | 16 | 16 | 100% | |
| Number of Slices containing unrelated logic | 0 | 16 | 0% | |
| Total Number of 4 input LUTs | 32 | 3,840 | 1% | |
| Number of bonded IOBs | 11 | 97 | 11% | |
| Number of BUFGMUXs | 1 | 8 | 12% | |
| Average Fanout of Non-Clock Nets | 2.44 | | | |

Fig. 7Device utilization summary forBASK Modulation

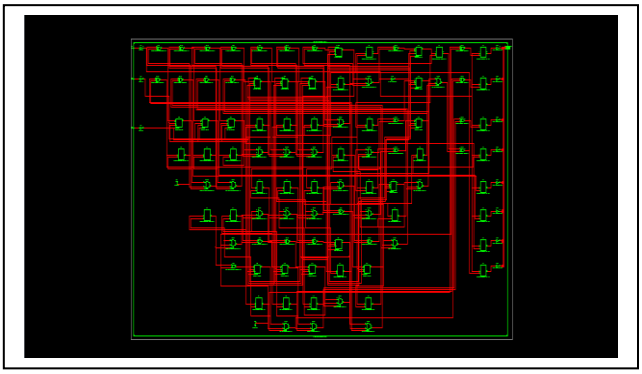

Fig. 8 Technology schematic forBASK Modulation

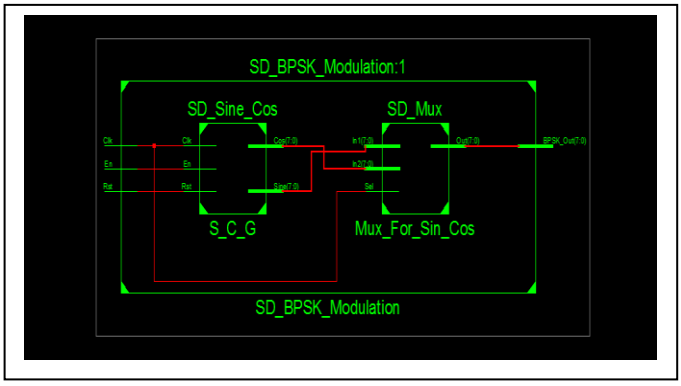


Fig. 9RTL schematic for BPSK modulation

| Device Utilization Summary | | | | [-] |
|---|---|---|---|---|
| **Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** |
| Number of Slice Flip Flops | 16 | 3,840 | 1% | |
| Number of 4 input LUTs | 40 | 3,840 | 1% | |
| Number of occupied Slices | 20 | 1,920 | 1% | |
| Number of Slices containing only related logic | 20 | 20 | 100% | |
| Number of Slices containing unrelated logic | 0 | 20 | 0% | |
| Total Number of 4 input LUTs | 40 | 3,840 | 1% | |
| Number of bonded IOBs | 11 | 97 | 11% | |
| Number of BUFGMUXs | 1 | 8 | 12% | |
| Average Fanout of Non-Clock Nets | 2.44 | | | |

Fig. 10Device utilization summary forBPSK Modulation

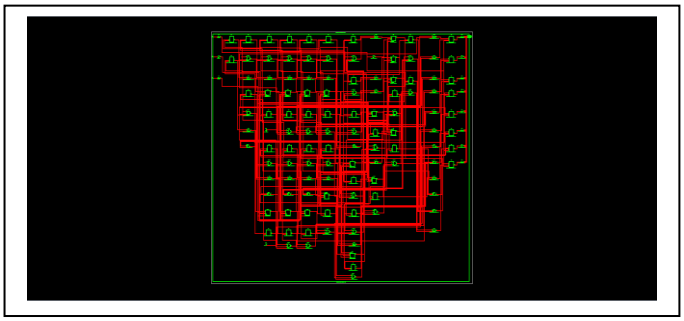

Fig.11Technology schematic forBPSK Modulation

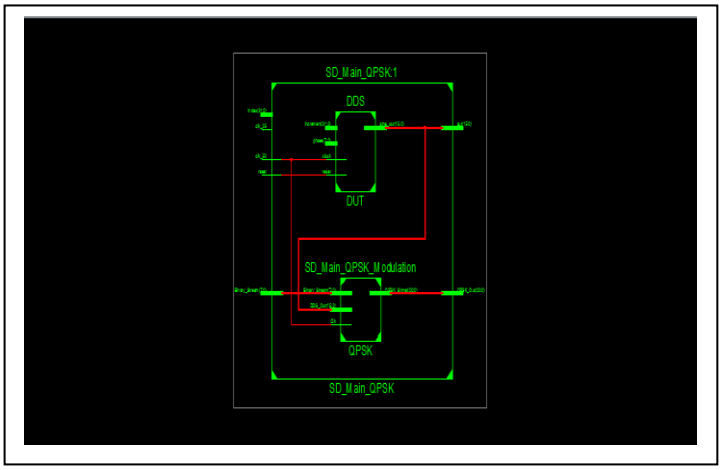


Fig. 12RTL schematic for QPSK modulation

| Device Utilization Summary | | | | [-] |
|---|---|---|---|---|
| **Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** |
| Number of Slice Flip Flops | 13 | 3,840 | 1% | |
| Number of 4 input LUTs | 25 | 3,840 | 1% | |
| Number of occupied Slices | 22 | 1,920 | 1% | |
| Number of Slices containing only related logic | 22 | 22 | 100% | |
| Number of Slices containing unrelated logic | 0 | 22 | 0% | |
| Total Number of 4 input LUTs | 25 | 3,840 | 1% | |
| Number of bonded IOBs | 47 | 97 | 48% | |
| Number of RAMB16s | 1 | 12 | 8% | |
| Number of MULT18X18s | 2 | 12 | 16% | |
| Number of BUFGMUXs | 1 | 8 | 12% | |
| Average Fanout of Non-Clock Nets | 1.47 | | | |

Fig. 13Device utilization summary forBASK Modulation

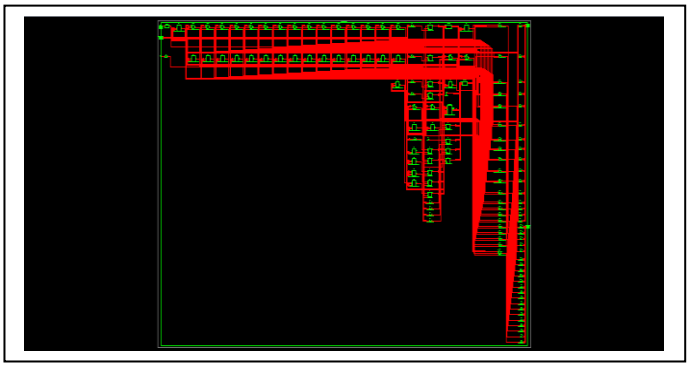

Fig. 14Technology schematic forQPSK Modulation

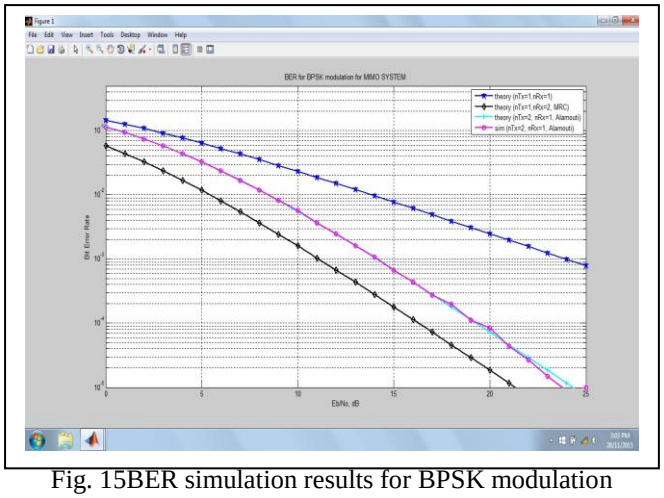


Fig. 15BER simulation results for BPSK modulation

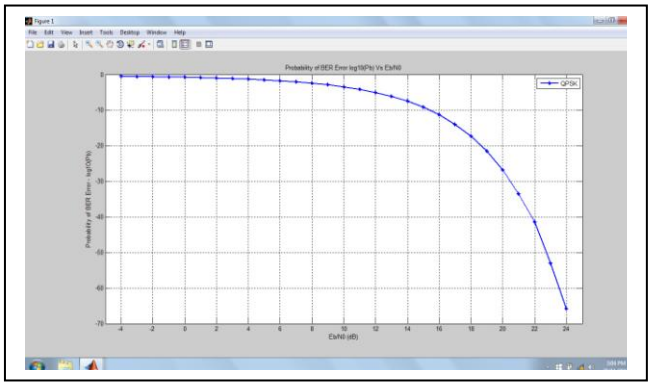


Fig. 16BER simulation results for QPSK modulation

## VI. Applications

The system has the applications for the measurement of performance and checking the reliability of the networks like Commercial Communication Systems, Wireless Communication Systems, Optical Networks, Software Defined Radios and many more.

## VII. Conclusion

The system has many advantages because of the use of its implementation on FPGA like gives fast results and reconfigurable design since using FPGA, productivity increases since time of design is reduced, cost is less as compared to conventional performance measurement methods.
It consumes less power.

## VIII. Future Scope

The system can be implemented as a standalone system with implementation of all modulation schemes as well as calculations of BER on a single FPGA. This system can be used to measure more than one performance parameters for the advanced modulation schemes which are presently used in modern communication systems.

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