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Modeling and Comparative Analysis of Logic Gates for Adder and Multiplier Applications -A VLSI based approach

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Abstract: *The logic gates are the fundamental building blocks of VLSI and embedded applications. These gates can be designed using several design techniques and implemented at different levels of architectures. This paper focuses on design and evaluate the performance of logic gates used in the Adders and Multiplier using various design technique like CMOS design GDI design and PTL design. These different design styles have pros and corns with reference to performance measure as Delay, Power consumption, Area and Gate Count. The design and simulation of logic gates is performed on CADENCE Design Suit 6.1.6 using Virtuoso and ADE Environment at GPDK 180nm technology. Comparative study between logic gates designed using CMOS, GDI and Degenerated PTL technique is presented in this paper, with performance measure as Number of transistor (Gate count), Power, Delay, Area and Power Delay Product.*

Keywords: *Logic Gate, CMOS design, GDI design, Degenerated PTL design, CADENCE, 180nm technology, Area, Power and Delay.*

I. Introduction

Very Large Scale Integrate (VLSI) circuits are consequential for designing of high performance and portable devices. The performance parameters like speeds, area, cost and power are the main parameters plays important role in the VLSI technology. The basic logic gates are fundamental components and accommodate as the building blocks to VLSI digital logic circuits utilizing combinational logic. The logic gates mainly used in to perform binary calculations, which in term is used within adder and multiplier blocks, and also found in Comparator, Compressor, Code converter, Error detecting or Error correcting and Parity checker [2].

The principle of operation on basic gates is that the circuit operation on two voltage levels considered in to logic levels as logic 0 and logic 1.When applied inputs either logic 0 or logic 1 will get a output gate replication depends upon the particular logic of the gate. In this paper we are consider the basic logic gates are AND, NAND, OR, NOR, XOR and XNOR. The gates can be designed using different design styles, we have considered Complementary Metal Oxide Semiconductor (CMOS) design, and Gate Diffusion Input (GDI) design and Degenerated Pass Transistor Logic design for our consideration. Comparative analysis of the gates with these design style is coated with respect to power, delay, speed and area as performance measures.

II. Literature Review

The following references are some of the papers that we have referred in our design and that related to design of basic gates in different design styles. From [1] the working and principle of logic gates is obtained and their behavior with basic functionality and operation is given. From [2] the design of universal gates using CMOS and Stacking design technique is provided and comparative analysis is coated. From [3] the study and design of XOR gate and AND gate design using CMOS (Complementary Metal Oxide Semiconductor), PTL (Pass Transistor Logic), CPL (Complementary Pass Transistor), DVL (Double Value Logic) and GDI (Gate Diffusion Input) techniques is made and comparative study is performed with three main parameters as area, delay and power. In [4] the authors focus on various CMOS logic designs technique to analyzed different parameters like power, area and delay. In [5] detail description and working about GDI technology is provided, and the basic gates are designed using GDI design style and observed the simulation results.

III. Various Design Technique For Basic Gates

A. CMOS Design style

CMOS is the most commonly used technique in the digital circuits. It's a combination of pull-up PMOS network, it will set the output is logic 1 and pull-down NMOS network, it will set the output is logic 0.Both the network cannot be activated and deactivated at a time. The advantages of this design technique of

logic gates output level is not degraded (Full swing output), increase the operation speed (Delay reduced) and more power, area consumption because number of transistor require designing a gate.

B. GDI Design Style

Gate Diffusion Input is same as the CMOS inverter, it has smaller area than the CMOS design and implemented in complex logic function. Construction this design style using three inputs, they are C (common input to both PMOS and NMOS), F1 (source or drain input of PMOS), F2 (source or drain input of NMOS). The supplied inputs or can of P and G can be Vdd or can be grounded or can be input signal depending on the circuit to be designed by using logic levels of the input and output. The advantages of this design technique are used less number of transistor compare to CMOS design technique and high performance (reduced the delay). Main drawback is output voltage level is degraded (reduced voltage swing) and power consumption high.

C. Degenerated PTL Design Style

Degenerated Pass Transistor Logic is family of Pass Transistor Logic (PTL).This is one of the design style used to overcome the PTL design technique and reduce the degraded output voltage level. Design of basic logic gates using this technique reduced the threshold loss problem, reduced the delay (minimum number of transistor used), lesser power dissipations and smaller area.

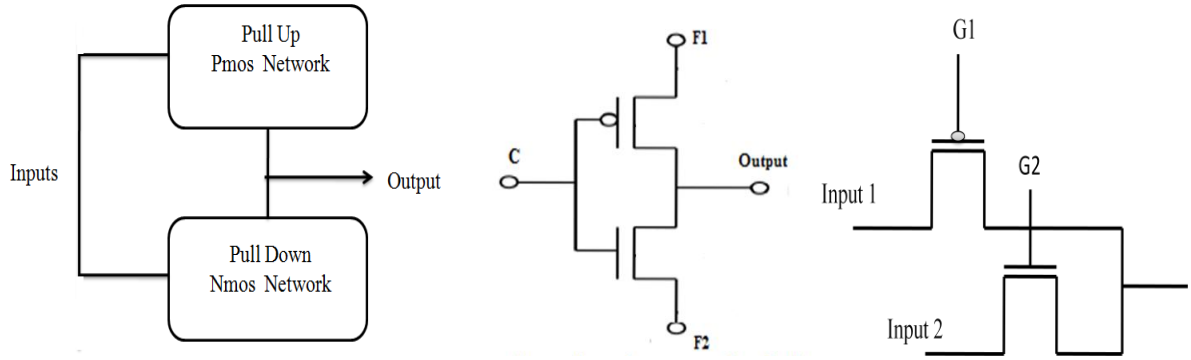

Figure 1: Functional diagram of (a) CMOS, (b) GDI and (c) Degenerated PTL.

IV. Results And Discussion

The design and functional verification of all the basic gates is performed on the CADENCE Design Suite 6.1.6 using Virtuoso and ADE environment at GPDK 180nm technology, the functional verification is performed by providing a Vpulse from analog library and the time duration such that it covers all the combination for the test inputs so that the output can be verified.

A. Simulation Result

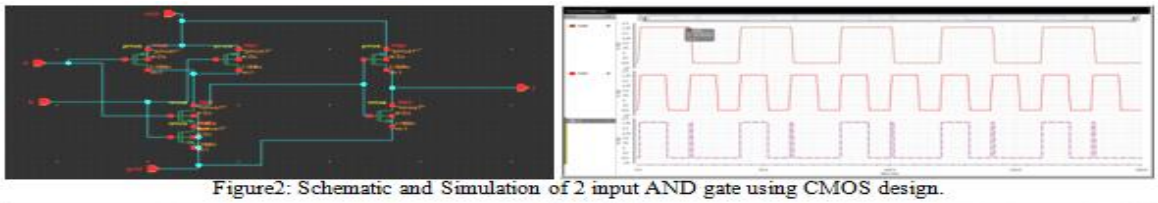

Figure2: Schematic and Simulation of 2 input AND gate using CMOS design.

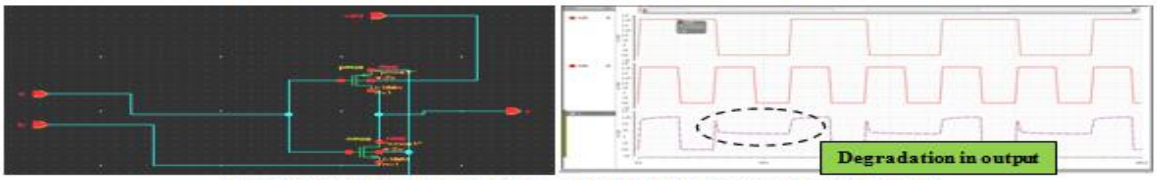

Figure 3: Schematic and Simulation of 2 input AND gate using GDI design.

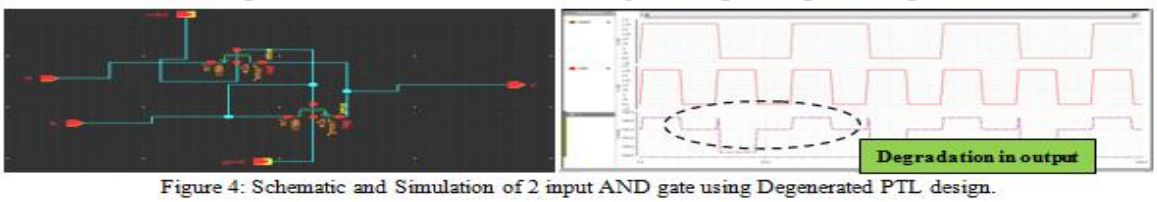

Figure 4: Schematic and Simulation of 2 input AND gate using Degenerated PTL design.

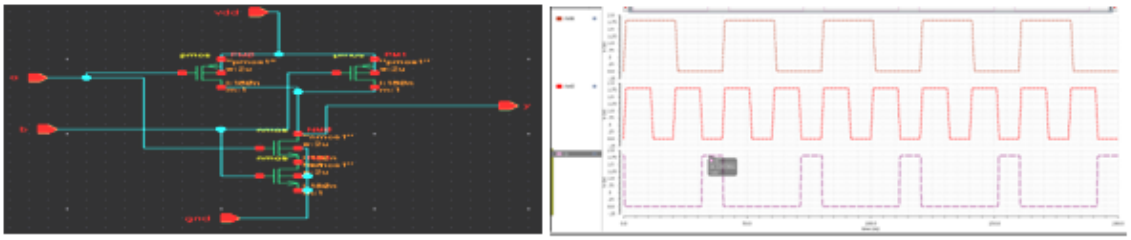

Figure 5: Schematic and Simulation of 2 input NAND gate using CMOS design.

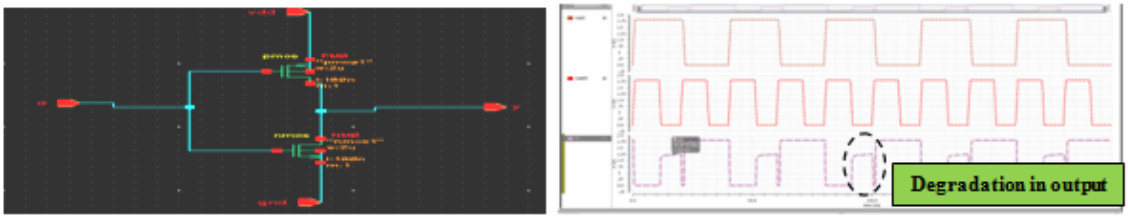

Figure 6: Schematic and Simulation of 2 input NAND gate using GDI design.

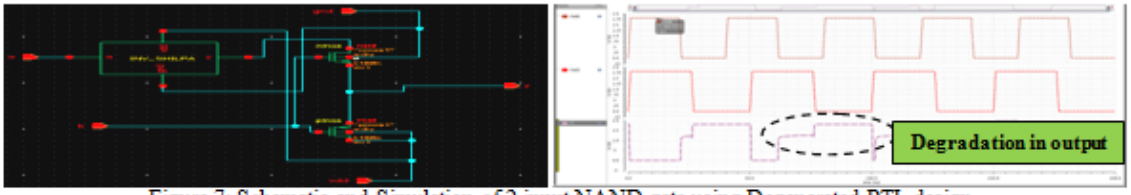

Figure 7: Schematic and Simulation of 2 input NAND gate using Degenerated PTL design.

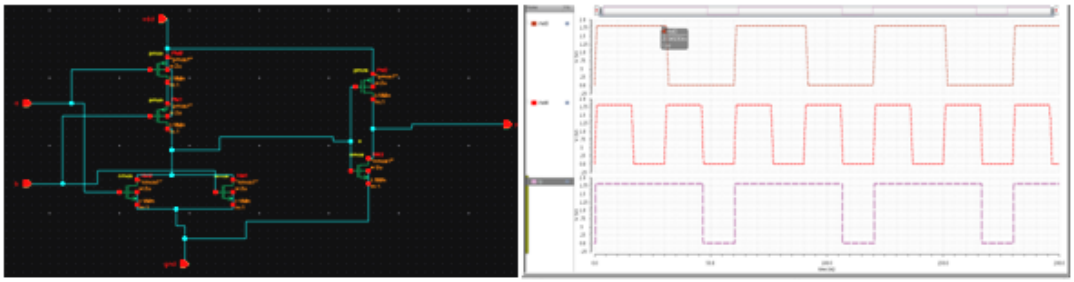

Figure 8: Schematic and Simulation of 2 input OR gate using CMOS design.

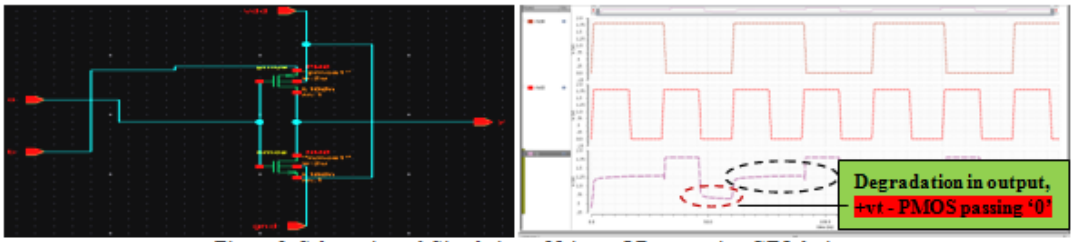

Figure 9: Schematic and Simulation of 2 input OR gate using GDI design.

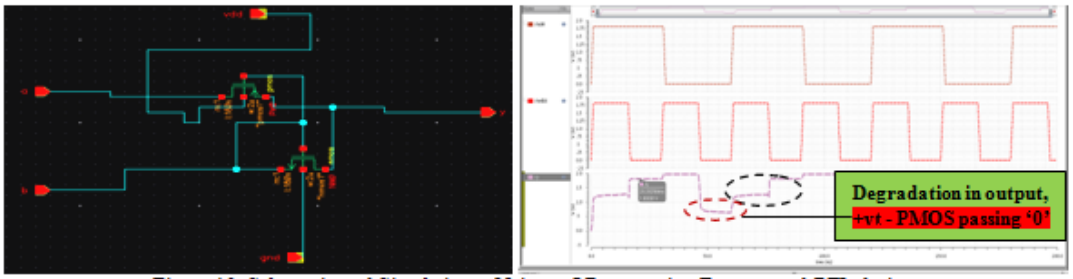

Figure 10: Schematic and Simulation of 2 input OR gate using Degenerated PTL design.

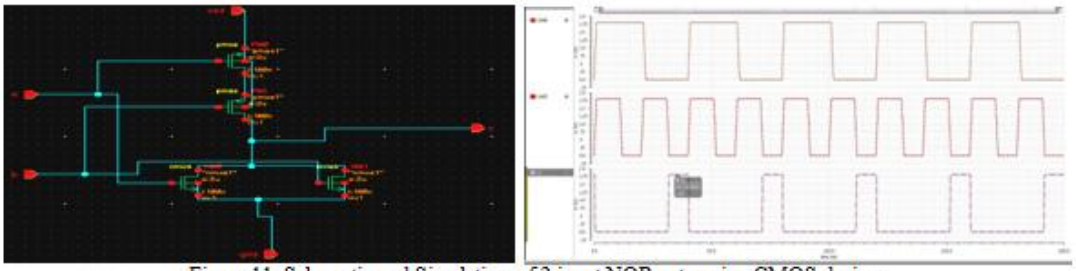

Figure 11: Schematic and Simulation of 2 input NOR gate using CMOS design.

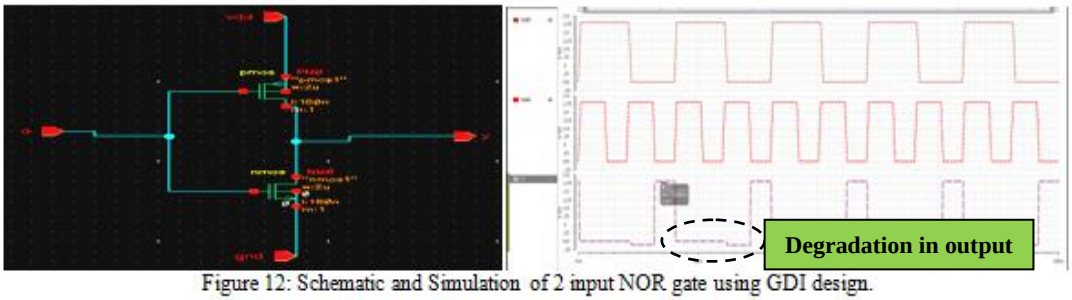

Figure 12: Schematic and Simulation of 2 input NOR gate using GDI design.

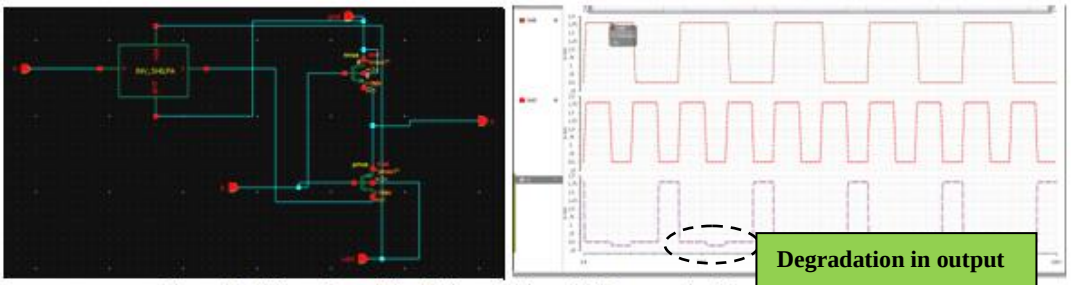

Figure 13: Schematic and Simulation of 2 input NOR gate using Degenerated PTL design.

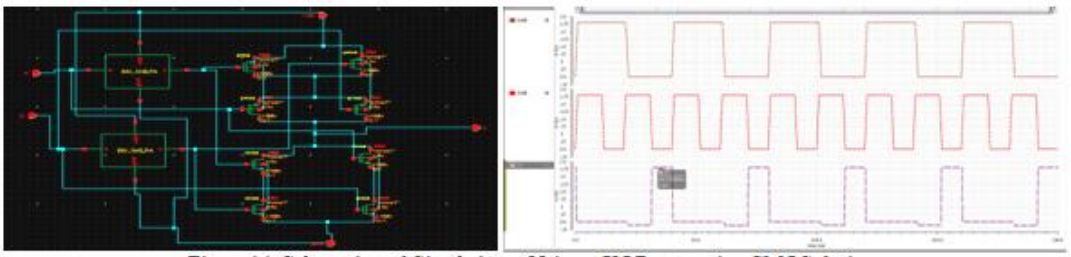

Figure 14: Schematic and Simulation of 2 input XOR gate using CMOS design.

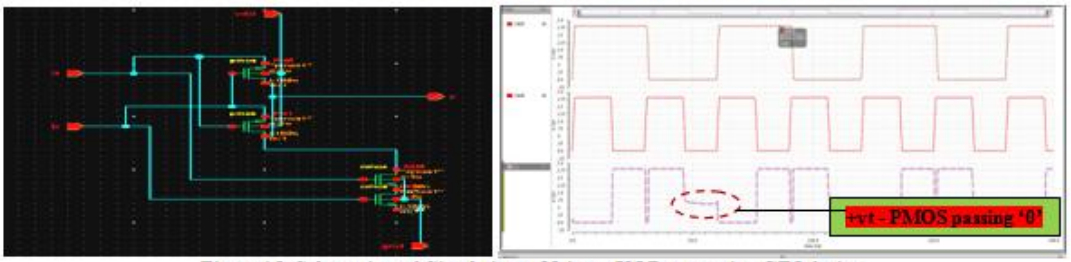

Figure 15: Schematic and Simulation of 2 input XOR gate using GDI design.

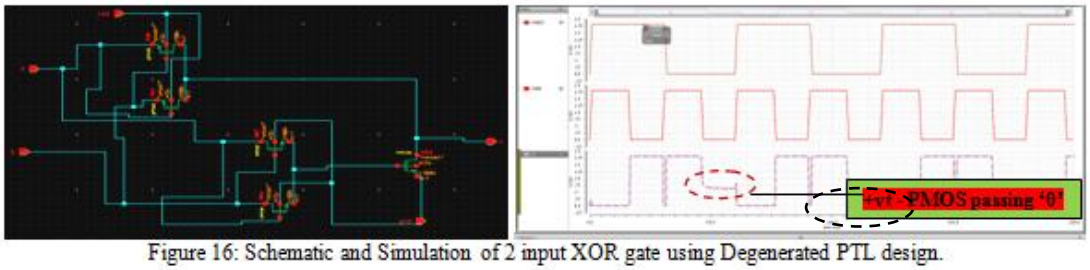

Figure 16: Schematic and Simulation of 2 input XOR gate using Degenerated PTL design.

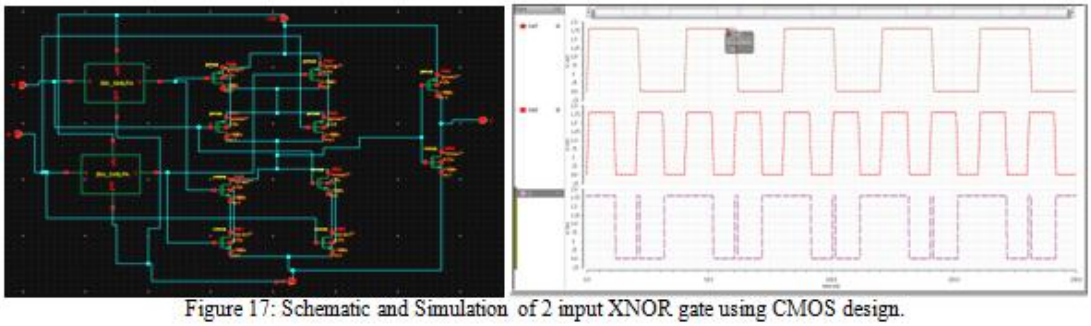

Figure 17: Schematic and Simulation of 2 input XNOR gate using CMOS design.

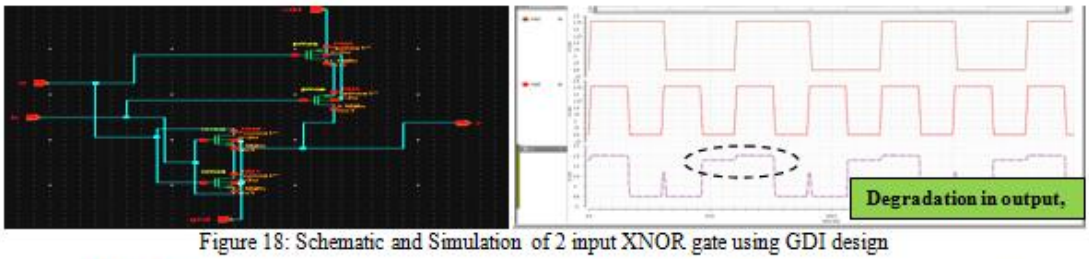

Figure 18: Schematic and Simulation of 2 input XNOR gate using GDI design

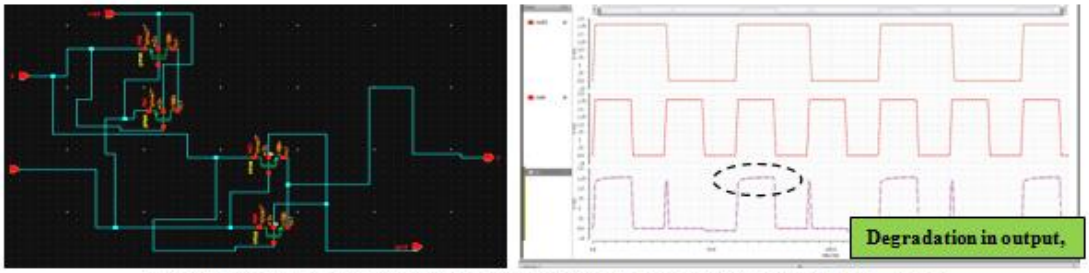

Figure 19: Schematic and Simulation of 2 input XNOR gate using Degenerated PTL design

B. Comparative Analysis

The logic gates considered and designed in this paper are with different design technique like CMOS, GDI and DPTL, the prime concern in the design is to get better output voltage with minimum number of transistor count, less delay and low power consumption, hence the performance measure are number of gate/transistor count, delay and power. The comparative result are shown in tabulation

Table 1: Comparative analysis of logic gates with reference to **Delay**

Design style/ logic gate	AND	OR	NAND	NOR	XOR	XNOR
CMOS	11.2E-9	46.26E-9	75.95E-12	85.81E-12	35.00E-9	11.03E-9
GDI	16.02E-9	46.06E-9	72.82E-12	74.48E-12	30.0E-9	16.07E-9
DPTL	16.02E-9	46.06E-9	72.82E-12	74.48E-12	29.95E-9	16.01E-9

Table 2: Comparative analysis of logic gates with reference to **No of Transistor Count (Gate Count)**

Design style/ logic gate	AND	OR	NAND	NOR	XOR	XNOR
CMOS	06	06	04	04	12	14
GDI	02	02	02	02	04	04
DPTL	02	02	04	04	05	04

Table 3: Comparative analysis of logic gates with reference to **Power**

Design style/ logic gate	AND	OR	NAND	NOR	XOR	XNOR
CMOS	3.827E-8	5.307E-9	1.101E-7	2.183E-9	1.361E-9	2.549E-8
GDI	5.307E-9	1.114E-8	2.687E-8	1.013E-8	2.272E-8	1.640E-8
DPTL	3.829E-8	9.582E-9	5.681E-8	7.469E-9	2.954E-8	2.395E-8

V. Conclusion

In this paper, we have designed basic gates like AND, NAND, NOR, OR, XOR and XNOR gates using CMOS, GDI and Degenerated PTL technique. A comparative analysis of all the basic gates is made using different design styles is coated here. This paper provides the bases to select the design style for a logic gate to be selected for adder or multiplier based on the requirement of the design, the gate can be selected by the designer by taking the best out of performance measures considered. These design technique are suitable for arithmetic and logic processing and in VLSI applications where a low power, high speed and area prime concerns.

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