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Design and Implementation of Citrus Classification Architecture on Fpga

Nishwinpal[1], Kiran Kumar V G[2]
[1]*ECE Department, Sahyadri College of Engineering and Management, Mangalore, India*
[2]*Associate Professor, ECE Department, Sahyadri College of Engineering and Management, Mangalore, India*

Abstract: *Fruit classification is an emerging technique to classify the quality of fruits in large quantities. In this paper, we propose the design and implementation of citrus classification architecture on FPGA. The input color image is separated into R, G and B component and applied to Gaussian filter for smoothening of high frequency edges. The binarization technique is applied to smoothened image to obtain the limited range of representation to increase the visibility. The mean filter is applied as post processing filter to remove remaining noise. Finally the pixel classification block is used to classify the rotten part using blue color as reference feature. The system is implemented of Spartan 6 LX45 FPGA board and is observed that the proposed system is better compared to existing system.*
Keywords: *Pixel Classification, Citrus, Mean Filter, Binarization, Gaussian Filter etc.,*

I. Introduction

Certain part of Indian economy is based on agriculture which is the backbone. Directly or indirectly most of the population is dependent on this occupation. One of the main sources of producing vitamins for human body is fruits. It is almost harvested all over the globe; several kinds of fruits are grown in different part of the globe. One of the kinds is citrus fruits which produces large amount of vitamin C and vitamin B. Large quantity of citrus fruits are grown in India, and it is one of the reasons for economical growth with increase in exports of better quality fruits to foreign countries. The process from harvesting to packaging in a food processing industry constitute of several steps. The fruits are obtained in large numbers i.e. in tons from various farms. The obtained fruits have to be sorted or graded according to the quality or to different ripeness levels together with it we have to find whether there are any defective fruits between them. In the early decades the fruits were sorted or graded by evaluating manually i.e. using the traditional hand picking evaluation. Categorization of fruits and vegetables can be done on the basis of physical attributes like mass, dimension, shade, figure, precise gravity, and provide freedom from diseases depending on the different climatic conditions. Presently recognized methods for categorizing of fruits and vegetables which are labor-intensive grading and computerized grading.

Categorization of fruits and vegetables in the clean form for quality is critical, as the people are becoming quality concern day by day. Additionally, upon advent of fruits and vegetables at the processing centers, they should be categorized rigorously for fineness in quality. The unripe properly ripe and over ripe fruits and vegetable are ought to be categorized out for the best properties. The different methods used to categorize the fruits depended on their shape, size and certain other parameters using computer vision algorithms designed using software. This required larger computational time and resources. The existing systems used artificial neural networks with different classifiers and together with it different color model variation methods were used with computer vision algorithms. The existing systems provided various efficient results with certain drawbacks such as efficient classification for sized based approach the uncertainty of normal sized rotten fruit was harder to classify. This paper proposes a design to categorize the citrus fruit into different grades based on the image feature, the purpose of designing the architecture on FPGA is to reduce resource utilization and increase the processing speed and also increase categorizing efficiency which was comparatively less using the system designed earlier.

This paper is organized as follows: The Section 1 discusses brief introduction. The Section 2 deals with proposed system design and methodology followed by mathematical approach in Section 3. The Section 4 provides the results and discussions. Conclusion mentioned at the last.

II. Proposed System Design And Methodology

2.1 Proposed System Design

The proposed system block diagram constitutes of Top view model and blocks present in each subsystem. The top view block diagram basically constitutes of input image which is divided into three channels (R/G/B) and three channels are given into three different subsystem the output obtained from the subsystem are given into pixel classification block where the result obtained will be two conditions either ripe / rotten. The proposed block diagram is as shown in figure1 below.

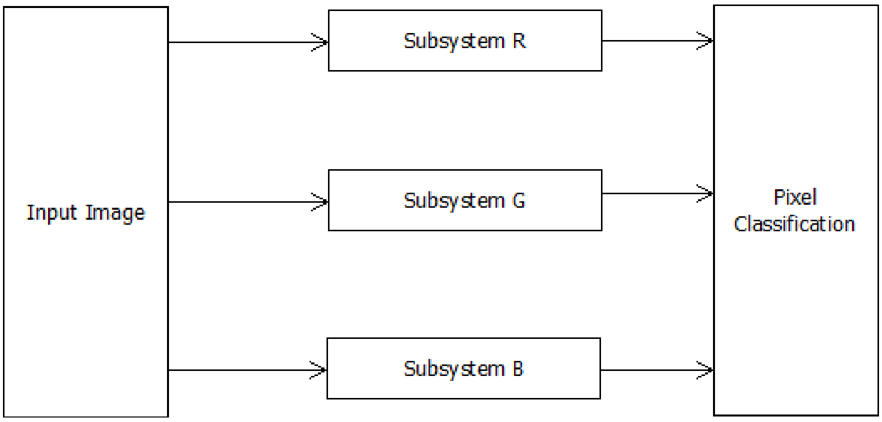

Fig. 1 Proposed Top View Model

The each subsystem constitutes of Gaussian filter, binarization (thresholding and adaptive thresholding block), mean filtering. Each of this block is designed in such a way to perform specified operation on the image and the output obtained is transferred to pixel categorization unit which will be shown next block diagram. The following block diagram fig. 2 shows the inner view of each subsystem.

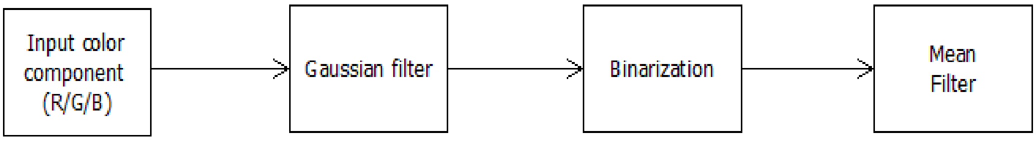

Fig. 2 Inner View of Each Subsystem

The next block diagram represents the pixel categorization unit. This is designed using maximum value counter and 1- bit shifter which divides the value by 2 and a comparator. The obtained values from the three subsystems are given to the pixel categorization unit as shown in the fig. 3 below which provides the categorized result.

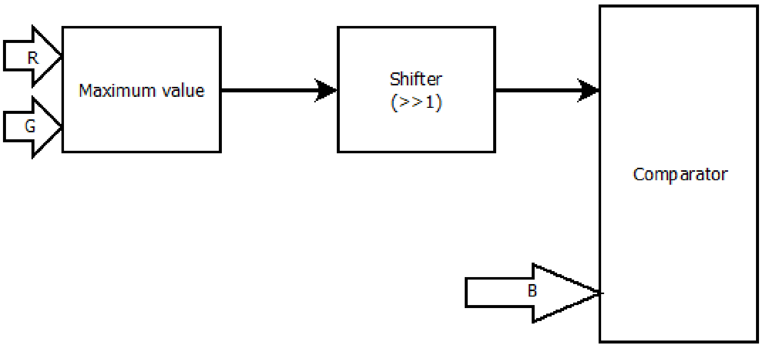

Fig. 3 Pixel Categorization Unit

2.2 Methodology

1) The proposed system methodology begins with splitting the color image into three different channels i.e. RGB using system generator Xilinx block set. Once the channel are split the image is resized according to our requirement i.e. it is resized to a matrix of 256 X 256 and then it is transferred to frame serialization block in fig. 4 where the 2-Dimensional data is converted into 1-Dimensional data and transmitted serially.

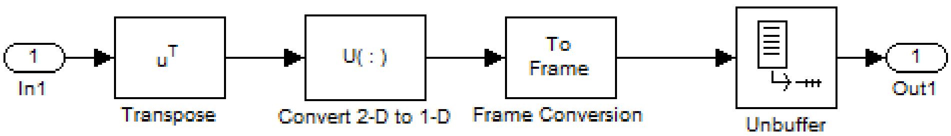

Fig. 4 Frame Serialization

2) The serialized data is transmitted into subsystem which constitutes of Gaussian filter for removal of noise present in the image and for smoothening purpose. The Gaussian filter designed here is of 3x3 moving window architecture shown in fig. 5. The mathematical equation is given in next section for the design.

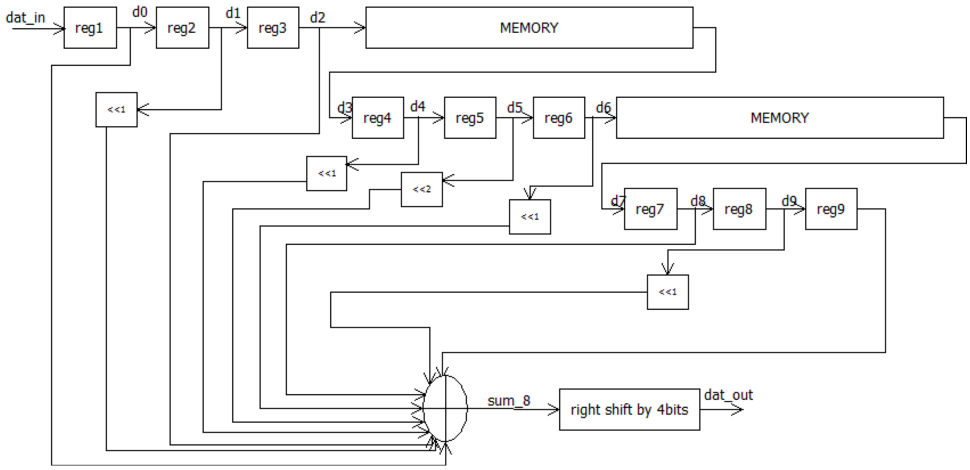

Fig. 5 Gaussian Filter Design

3) The filtered data is sent to the binarization block where the data is compared whether the value is less than 250 and greater than 63 if this condition is satisfied than the output of the binarized value is set to 255. If the condition is not satisfied it is set to 0. The output image is mentioned in the results section

4) The output from the binarization module is given to the mean filter. Which is also designed using 3x3 moving window shown in fig. 6. The calculation of value for the design is given in the mathematical section. The mean filter is used to retain edges and it also used as a filter to remove noise.

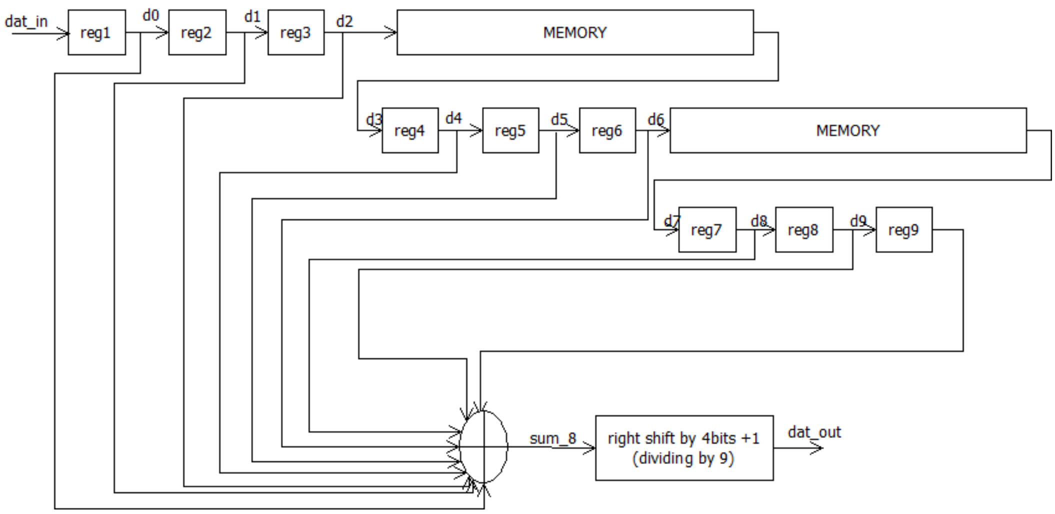

Fig 6 Mean Filter Design

5) The output from the mean filter is given to the counter. The counter is designed in such a way that the only if the pixel value from the mean filter output is greater then and equal to hundred the counter counts else the count remains same.

6) Once the counter count all the pixels, the output from the three subsystem counter are taken and the counter values from the R and G subsystem are given maximum calculator which provides the count that whether R or G is maximum as the output. This is then given to one bit right shift module from where the output will be obtained.

7) From there the output from the shift and B counter is taken to the comparator which compares between the two values and outputs '1' if the pixel value contains more number of blue values or green values which represents Raw or Rotten condition and outputs a '2' if it contains required amount orange pixel value according to the design which represents the ripe condition. This will be displayed in the output terminal.

This is the overall working methodology of the design, where the each module of subsystem and pixel categorization are designed first by writing the code using Xilinx 14.5 software in VHDL language and later the code will be put Black Box used in system generator and the connections will be made as per the design specification where we obtain the software model and it will be tested.

Once the software model is created and tested then we will generate the hardware model to by following certain procedure to design the hardware model. Once the hardware model is generated a single black box is created which contains all the individual blocks created in software model. After this the required or necessary connections are made. Once all requirements are completed the overall code is dumped into the Digilent Spartan-6 FPGA and tested.

III. Mathematical Models

3.1 Gaussian Filter Mathematical Model

One dimensional Gaussian filter is defined by the following equation. This is used for blurring and removes noise from the image. σ is the standard deviation used in the distribution with 0 mean. With this we obtained bell shaped Gaussian distribution.

$$G_{1-Df}(m) = \frac{1}{\sqrt{2\pi\sigma}} e^{-\frac{m^2}{2\sigma^2}} \qquad (1)$$

The standard deviation plays a major role in Gaussian distribution. This is useful when designing fixed length kernel. The Gaussian function is used in several research areas; the main function of using this is distribution frequency for noise or data. And also works as smoothening operator. This function will never have zero value and also the function is always symmetric. When processing images we will be using 2- dimensional Gaussian function, which is just the product of two 1-dimensional Gaussian functions this is given by the following equation:

$$G_{2-Df}(m,n) = \frac{1}{2\pi\sigma^2} e^{-\frac{m^2+n^2}{2\sigma^2}} \qquad (2)$$

Point spread function is obtained by using the two dimensional Gaussian function. Image is convoluted with the two dimensional Gaussian function to remove noise. Here we have used 3x3 moving window architecture as shown in the figure above, by substituting the value of co- ordinates of m and n we obtain the values from the equation as in the matrix given below:

$$G_{2-Df}(m,n) = \frac{1}{16}\begin{bmatrix} 1 & 2 & 1 \\ 2 & 4 & 2 \\ 1 & 2 & 1 \end{bmatrix} \qquad (3)$$

By convoluting the above value with image pixel value we get the filtered output. The standard deviation value is taken 1 here by varying standard deviation value we can vary the effectiveness of filter to get more effective result. By changing standard deviation value we get different matrix value.

3.2 Mean filter Mathematical Model

For reducing the quick pixel to pixel changes in the grey level images for the smoothening. Smoothing can be performed by applying an averaging mask which calculates a weighted sum of the greylevels pixels in a neighborhood and changes the value centre pixel with the new greylevel value. The blurring and retaining the brightness of the image using all positive coefficients for mask and sum as one. It is one of the basic smoothing filters. This is designed using the following equation given below

$$\mathrm{M}_{\mathrm{n}_{x,y}} = \frac{1}{mn} \sum_{(\mathrm{a,t}) \epsilon \mathrm{n}_{x,y}} \mathrm{f(a,t)} \qquad (4)$$

By using the above equation with 3x3 window architecture and applying the co-ordinates in the equation we get following matrix value which will convoluted with image pixel value to obtain the mean or average value for the centre pixel value and it is continued all the pixels in the image are calculated. Like all other convolution this is also dependent on kernel based design which depends on the shape and size of the neighborhood image pixels to be sampled to calculate the mean.

$$\mathrm{M}_{n_{x,y}} = \frac{1}{9}\begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} \qquad (5)$$

After convolution of the image pixel with the given matrix value we will obtain mean filtered output.

IV. Results & Discussions

The proposed technique was designed using software Xilinx 14.5. The language used was VHDL and block diagram was designed in system generator and implemented on Spartan 6 FPGA board. The system was tested for different citrus fruit images and the hardware utilization was reported. Table 1 shows the hardware resource utilization for existing and proposed method. Fig. 8 to 10 shows the results of fruit classified as raw, ripe and rotten fruit.

Table 1: Hardware Utilization of Proposed Method

Device Utilization Summary (estimated values)			**[-]**
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	778	54576	1%
Number of Slice LUTs	2321	27288	8%
Number of fully used LUT-FF pairs	249	2850	8%
Number of bonded IOBs	27	218	12%
Number of BUFG/BUFGCTRL/BUFHCEs	1	16	6%

1) Design Of Software Model

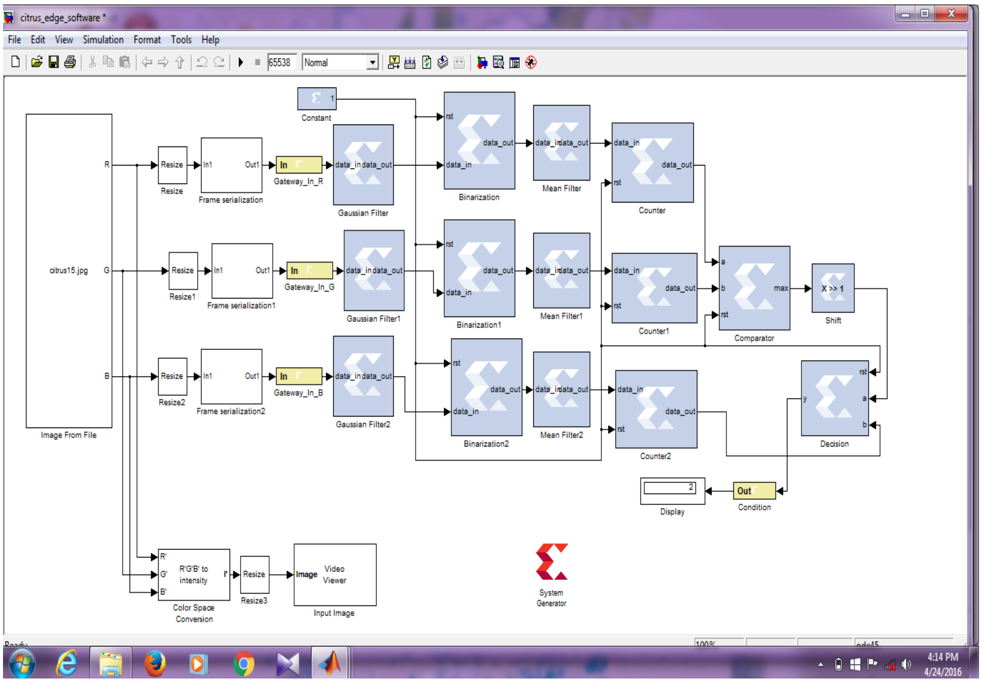

Fig. 7 Software Model Design

2) Output generated from software model
A) Raw Fruit

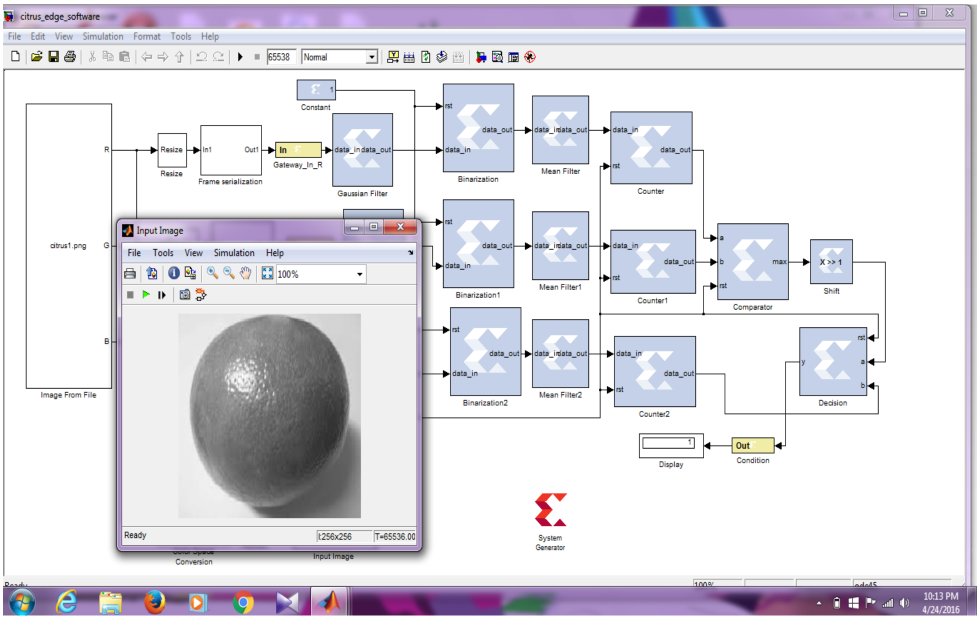

Fig. 8 Output Representing Raw Fruit

B) Ripe Fruit

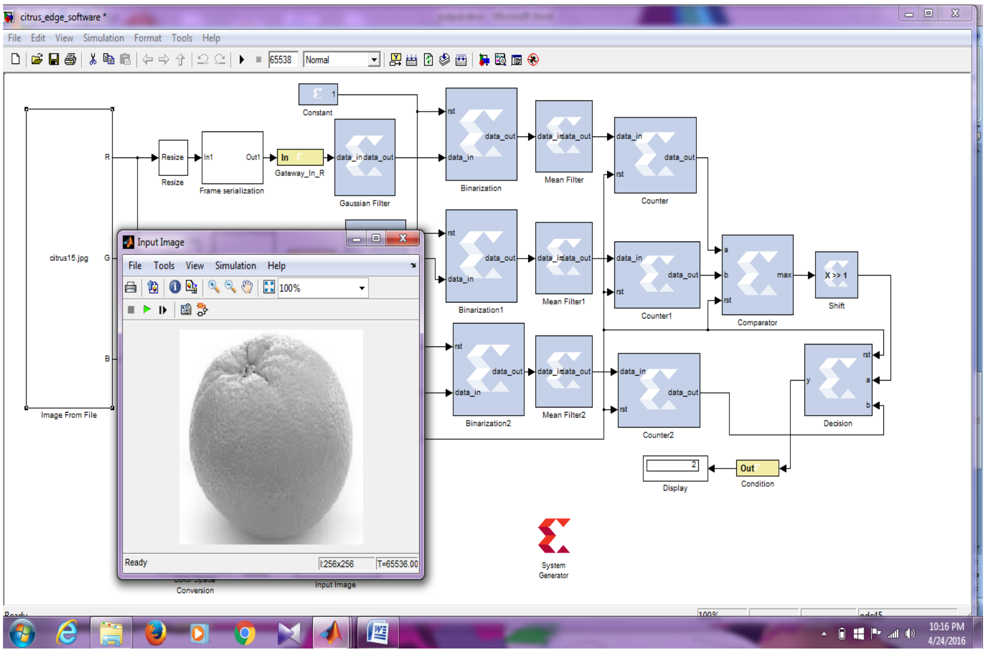

Fig. 9 Output Representing Ripe Fruit

C) Rotten Fruit

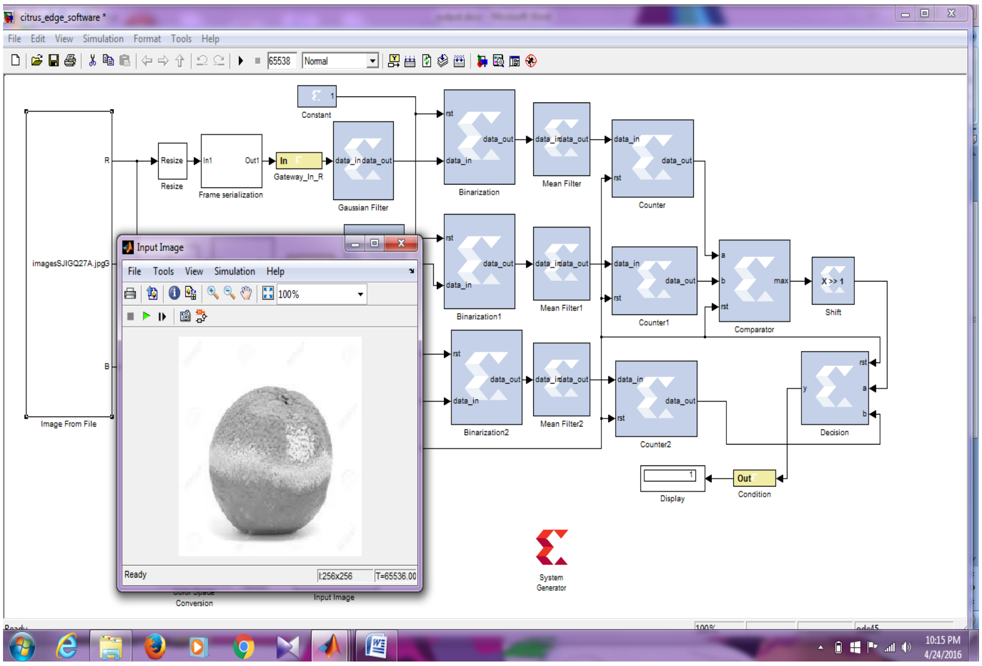

Fig. 10 Output Representing Rotten Fruit

3) The Hardware Model Design Using System Generator For Citrus Classification

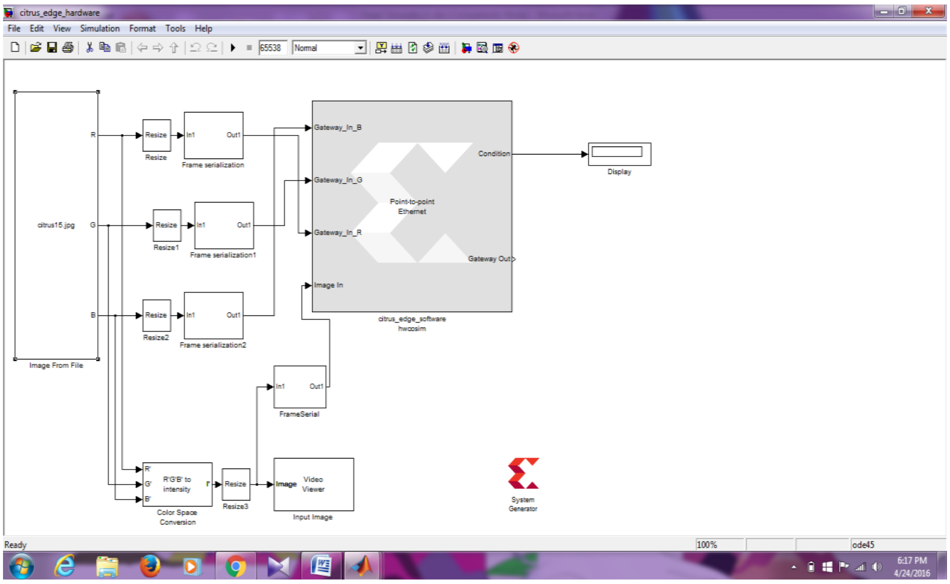

Fig. 11 Hardware Model Design

The comparison between existing and proposed method is shown in Table 2 and it is observed that the Hardware utilization parameters i.e., Number of slice LUT's, occupied slices and DSP48 slices are less compared to existing method.

Table 2: Comparison between Present and Existing System

Resource utilization	Existing system [1]		Proposed system	
	Used	Available	Used	Available
Number of slice registers	735	184307	778	54576
Number of slice LUTs	4550	92152	2321	27288
Occupied slices	1714	23038	1369	6822
DSP48A1 slices	64	180	0	58

V. Conclusion

In this paper, implementation of citrus classification hardware for accurate classification of citrus fruit was proposed. The proposed algorithm was designed on Spartan 6 LX45 Board and the results were observed and validated with optimized parameters compared to existing methods. In Future, this method can be extended to classify accurately for different types of fruits.

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