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Analyzing the Impact of Sleep Transistor on SRAM

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Abstract: *Low Power SRAMs have become a critical component of many VLSI chips. Power can be reduced by using either dynamic or static power reduction techniques. Power gating is one of the most effective static leakage reduction methods. In power gating sleep transistors are used. They disconnect the cell from power supply during sleep mode leading to 91.6% less static power dissipation but they also helps in reducing the dynamic power by reducing the power supply to the cell. In this paper the effect of sleep transistor in active mode is implemented and resulting SRAM is found to dissipate 32% less power than conventional SRAM.*

Keywords: *SRAM (Static Random Access Memory); 6T (Six transistors); 8T (Eight transistors); BL (Bit Line); WL (Word Line); WS (Word Select)*

I. Introduction

Power Gating is a low power technique used in deep sub-micron technology. Power gating is performed by shutting down the power for the portion of circuit in order to reduce the standby leakages. Power Switch (PS) is the basic element used in power gating circuits to shut down the power in the portion unused. Appropriate sizes of PMOS, NMOS or both are used as Power switch cells. NMOS and PMOS differ in the fact that they switch different power supply rails VSS and VDD respectively. They are also known as sleep transistors. They are turned OFF during the sleep mode and turned ON during the active mode for normal operation. The PMOS sleep transistor is used to switch VDD supply thus connected between circuit and power supply hence named as "header switch". The NMOS sleep transistor connected between circuit and GND controls VSS supply and hence called as "footer switch". Power Gating can be implemented in two ways:

1: Fine Grain Power Gating
2: Coarse Grain Power Gating.

Each approach has various tradeoffs. In Fine Grain technique there is a Sleep transistor added to each individual gate known as MTCMOS. Advantage of Fine Grain scheme is we can use existing cell synthesis, place and route tools by simply replacing simple gate with MTCMOS gate. However Fine Grain scheme add a sleep transistor to every MOS gate used thus significantly adding to the area requirements. Whereas in Coarse Grain scheme sleep transistor are added between permanent supply rails and GND i.e. for whole block only two transistors are required thus reducing area overhead. SRAM with coarse Grain power gating scheme is presented in this paper. A PMOS is inserted between power supply VDD and SRAM cell also NMOS is inserted between GND and SRAM cell. Both the sleep transistors are controlled using signal S and S_bar (compliment of S).

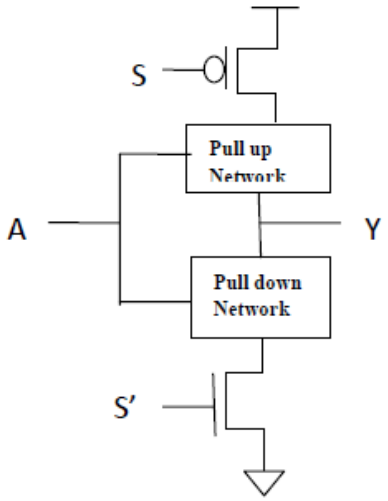


Fig 1: Sleep transistors approach [9]

Turning OFF the sleep transistor in sleep mode breaks the short circuit path connecting the power supply and ground thus reduces leakages in Sleep mode. They remain ON during active Mode for normal operation.
The contribution of this paper is:

- Power gating technique which reduces standby leakage current is studied.
- Effect of sleep transistors in active mode.

The rest of the paper is organised as under:
In section II, conventional 6T SRAM is studied. Also sleep transistor approach is applied on 6T SRAM. In section III, power estimation is performed and the results are compared. Finally conclusion is drawn in the section IV.

II. Conventional 6T SRAM Cell

Conventional 6T SRAM cell consist of two cross coupled inverter connected to input bitlines using the pass transistors. Wordline (WL) controls these pass transistor enabling them only during read and write operation. Input signal is applied to the bitlines which is passed through the pass transistor to the cell.

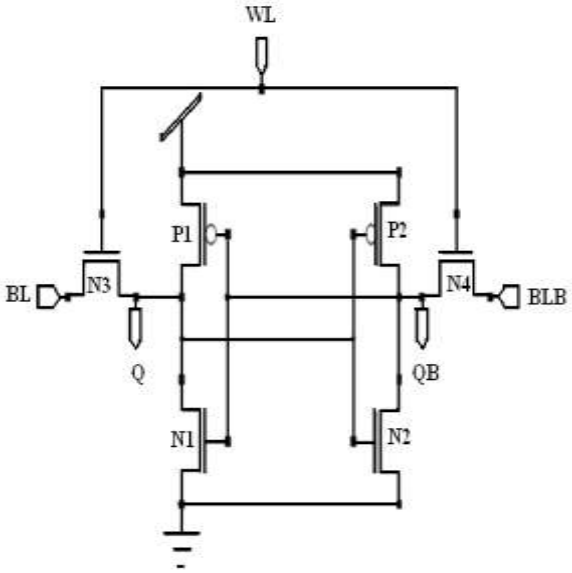
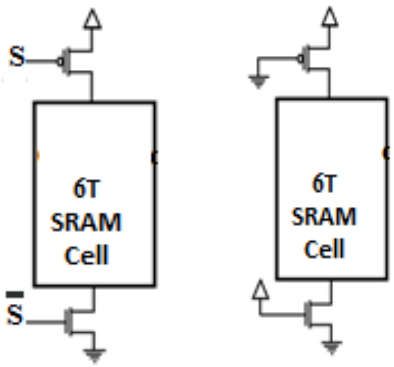


Fig 2: 6T SRAM Cell [10]

Reduction in feature size leads to increased Subthreshold and gate leakages causing a major contribution to static leakages. To reduce this we uses sleep transistor both PMOS and NMOS along with the 6T SRAM cell. They are turned OFF during Standby/Idle mode thus reducing the leakages by 91.6%. But in Active Mode both the sleep transistor are ON which causes a little drop in supply voltage and since power dissipation depends quadratically on VDD thus a reduction in power dissipation is also observed during active mode. In active mode S is lowered to zero such that PMOS is turned ON whereas S_bar is raised to 1 volt turning NMOS ON.



(a) (b)

Fig 3(a): Sleep transistor based 6T SRAM. (b): Sleep transistor based 6T SRAM in ACTIVE mode.

III. Simulations And Results

Fig 6 shows the 6T schematic with sleep transistor in active mode whereas Fig 7 shows the simulation output waveform of sleep transistor based 6T SRAM with both the sleep transistor ON for normal operation. Power calculation, Schematic simulation and layout are done on CADENCE VIRTUOSO tool.

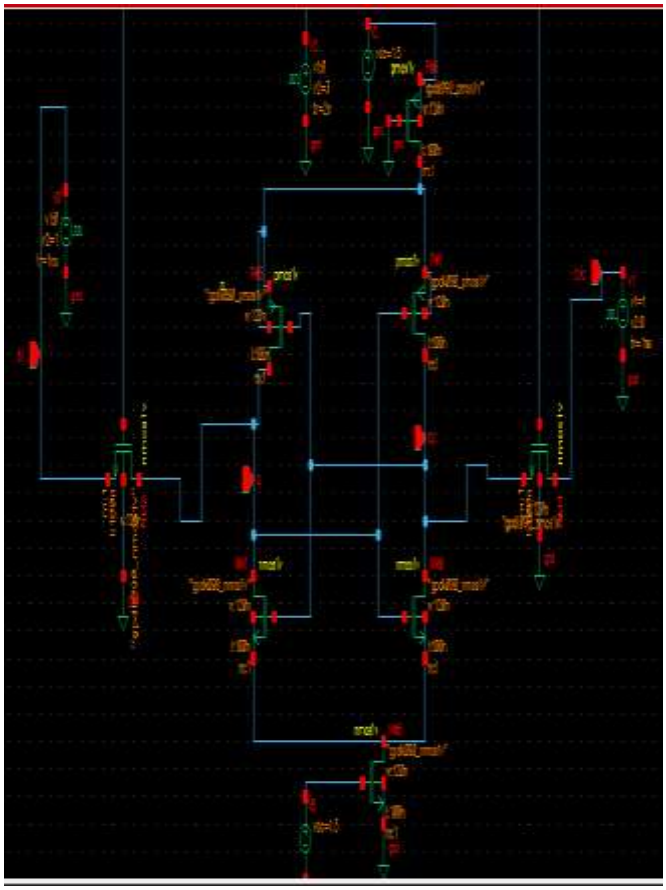


Fig 4: Schematic of 6T SRAM with sleep transistor in active mode

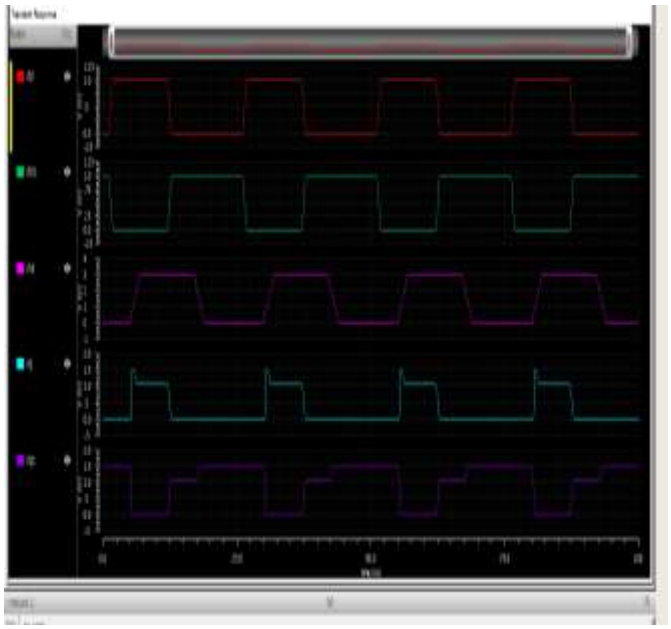


Fig 5: Output simulation waveform of 6T with sleep transistor operated in active mode

Table 1: Comparison of Power Dissipation and Delay between 6T SRAM and 6T SRAM with sleep transistor

	Avg Power Dissipation	Delay
6T SRAM	44.684uW	411.3 ps
6T SRAM with sleep transistor	30.274uW	122 ps

IV. Conclusion

Sleep transistor are turned OFF during sleep mode leading to 91.6% reduction in Static Power dissipation. However in active mode they are ON. A small amount of voltage drop occurring cause's reduction in power supply to cell, since dynamic power is quadratically proportional to VDD. Hence 6T SRAM with sleep transistor in active mode have 32.25% less power consumption than conventional 6T SRAM cell. Small size sleep transistor are required for large reduction in static power and large size sleep transistor are required to bound the voltage drop hence sizing of PMOS and NMOS sleep transistors are also very critical.

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