IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 7, Issue 5, Ver. I (Sep.-Oct. 2017), PP 40-47
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Carbon Nanotubes FET based high performance Universal logic using Cascade Voltage Switch Logic

Mitali Sharma[1], Rajesh Mehra[2]
[1](P G Scholar, ECE Department, NITTTR, Chandigarh, India)
[2](Head of ECE Department, NITTTR, Chandigarh, India)

Abstract : *The paper proposes the design of efficient universal logic gates for nanotechnology. The basic component used in the design is Carbon Nanotubes instead of the conventional silicon based units. The extraordinary properties of the carbon nanotubes such as high thermal & electrical conductivity, flexibility, high tensile strength provides the added advantages for adopting the CNTs for the design of electronic circuits. Along with these properties, the CNTs give a great opportunity of scaling the circuit design to the nano regime. The logic gate designed using the CNTFETs along with cascade voltage switch logic had proved to be an achievement that can be further taken to the high end complex circuits. The design of the logic gate proposed in this paper is designed using the 32nm Stanford CNTFET technology and is compared with the conventional CMOS based CVSL circuits. The parameters used for the design analysis are the frequency, power consumption, PDP along with the number of transistors used. It was found that the power consumption for both the logic gates is 52.6% and 55% less than the conventional CMOS based NAND and NOR logic respectively and the delay is 28.2% and 24% less. The obtained results show a significant improvement and the work can be taken up further for high end circuits.*

Keywords- *CNTFETs, CVSL, NAND Gate, NOR gate*

I. INTRODUCTION

In the growing era of nanotechnology, the electronic devices are moving fast towards the nanotechnology. One such step in this ladder is the adoption of Carbon nanotubes field effect transistors. Carbon nanotubes field effect transistors have captured almost every sphere of the technological aspect of electronic devices. The characteristics that carbon nanotubes have make them an excellent pick for all high level and complex circuits and devices The unique properties that carbon nanotubes possess makes them ideal choice for all high end applications and is even seen as a viable option as a replacement of conventional CMOS technology. The design of the electronic circuits using CNTFETs results in a high performance, low power consuming devices. The strength and compactness are the other important characteristics of CNTFETs. The circuits designed using the carbon nanotubes FETs extremely high speed and have size in the pico scale. The tensile strength and inertness are the other added characteristics of CNTFETs. The advancements in carbon nanotubes FETs will give a way to all the technological research to move towards the nanotechnology regime. Another step in this improvement is the adoption of Cascade voltage switch logic. The Cascade voltage switch logic is the logic that can be used in designing the circuits that help in achieving better results in comparison to the conventional logic circuits. The use of the CNTFETs along with the cascade voltage switch logic in construction of the logic gates is a bench mark achievement as using these gates any simple or complex circuits can be constructed efficiently. The universal gates are the basic logic gates that are used in the construction of any simple or complex electronic logic devices may it be the comparators, multiplexers or the RAMs to ALU. The universal logic gates are the building blocks of the electronics, as these gates are used in the construction of each and every type of logic circuits with the combination of other logic circuits. So the improvement in the basic unit will automatically leads to the improvement in the whole circuits design and will prove to be a great achievement in almost every sphere of technological aspect.

II. CARBON NANOTUBES

The Carbon is an element that is chemically available in a number of different forms. These are known as allotropes The Carbon atom has a number of allotropes. These allotropes are available in various dimensional forms. The allotropes available in the 3-dimensional structure are diamond and graphite. Further low dimensional (0D, 1D, 2D) allotropes are also available. These low dimensional allotropes of Carbon are collectively known as Carbon Nanomaterial. The graphite allotrope has a 2-dimensional structural material known as the Graphene. Grpahene is the 2D single layer of Graphite [1]. The atoms of the Carbon in the Graphene are placed in hexagonal or honeycomb lattice. The Carbon nanotubes are formed by rolling these

graphene sheets like a cylinder. The diameter for these tubes scale to nanometers range (10^{-9} meters) and the length varies from nanometers scale to centimeters scale. These sheets can take up two different forms depending upon the way it is rolled up, i.e. it depends upon the chirality [2]. The Carbon nanotubes have many different structures. These structures differ in length, layer count and thickness. The forms taken up by the nanotubes are metal and semiconductors depending upon the way these sheets are rolled up. The layers of graphene that make up the carbon nanotubes take up the shape of a hexagon, The carbon molecules takes up apexes of this hexagonal arrangement. The semiconductor form of carbon nano tubes are used in the design of Carbon nanotubes field effect transistor (CNTFET) [2]. The basic structure of how graphene sheet looks like is shown below in figure 1. These sheets consist of a mesh like structure with a series of carbon atoms. These sheets when rolled up are called as the carbon nanotubes.

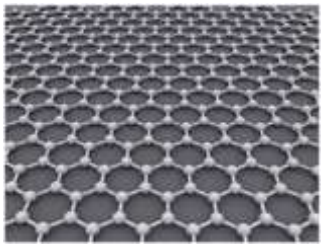

Figure 1: Structure of Graphene

The basic structure of carbon nanotubes is as shown below in figure 2. The structure of carbon nanotubes is basically of two types. The type of nanotubes depends on the shell count that constitutes the tubular structure.

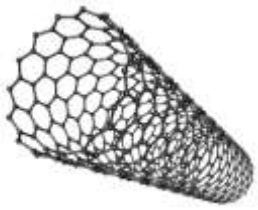

Figure 2: Structure of Carbon Nanotubes

It may have one wall, two walls or multiple walls. The two types of carbon nanotubes are as explained below:
Single walled Carbon Nanotubes (SWCNTs): This type of carbon nanotubes consists of only single layer of grapheme cylinder. This layer can be of metal or semiconductor material.
Double walled Carbon Nanotubes: This type of nanotubes lies n between of the single walled and multi walled. They have exactly two layers of tubes rolled up at specific angles. **Multi walled Carbon Nanotubes (MWCNTs)**: This type of carbon nanotubes consists of both the metal and semiconductor layer of cylinder materials. These are arranged in the concentric cylinder pattern. The metallic cylinder negates the properties of semiconductor material. Thus this type of CNTs is usually not preferred for the industry applications [3]. The structure of all these types of CNTs is shown below in figure 3 The structure of all these types of carbon nanotubes are as shown below in figure 3, where a represents the Single walled CNTs and b represents the double walled CNTs and (c) Multi walled CNTs [1].

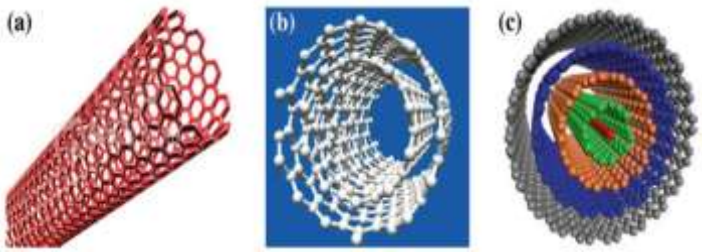

Figure 3: Types of Carbon Nanotubes

III. CARBON NANOTUBES FIELD EFFECT TRANSISTOR

The Carbon nanotubes field effect transistors are basically the field effect transistor that makes use of the carbon nanotubes or an array of these tubes instead of the silicon. The nanotubes are used as the channel material. Carbon nanotubes FETs are in a way similar to the MOSFETs. Similar to the structure of MOSFETs, CNTFETs have 3 terminals, viz. source, drain and gate. The basic structure of carbon nanotubes FET is as shown below in figure 4 [4]. The gate terminal controls the current that flows from the source to drain terminal. When gate terminal is on, the channel present in the FETs, allows the flow current to from source to drain through it. The difference between the MOSFETs and the CNTFETs is in the type of channel present in them [5]. The MOSFETs use heavily doped Silicon material as channel material and the CNTFETs use the carbon nanotubes as the main component for the channel used for the flow of current [6].

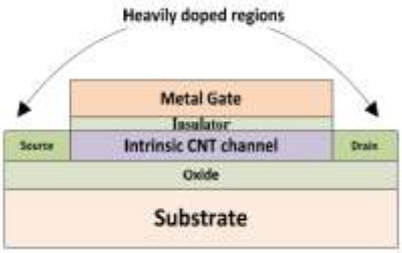

Figure 4: Schematic Diagram of a Carbon Nanotubes FET

As is seen from the figure 3, the CNTFET is a four terminal device just like the conventional silicon based MOSFETs. It consists of the intrinsic Carbon nanotubes based channel. The channel is separated from the metallic gate terminal with the help of the insulator sandwiched between the two layers. The current enters into the device through the source terminal and flows through the CNT based channel and leaves the device from the end terminal which is the source terminal. The source and drain terminal acts as the interconnection for connecting more devices [7-8]. In spite of having a structural similarity, there is vast difference in the performance and characteristics. MOSFETs have been replaced with the CNTFETs due to a number of setbacks faced by them. Some of them include the short channel effects, high leakage current, reliability issues and many others. With the increasing trend of the nanotechnology, the CNTFETs replaced the MOSFET devices. With the decrease in the size, the scaling down of the MOSFETs becomes difficult. CNTFETs on the other hand offers high temperature resistance, strong inter bonds that provides strength at such a small size, large transconductance, high electron hole mobility and many others. Thus Carbon nano tubes based FETs have become an ideal substitute for the transistor material. The CNTFETs are categorized into two categories, one based on their geometry and the other based on their operation. Based on the geometry, there are top gated, bottom gated and the coaxial gated CNTFETs and based on the operation type, there are Schottky barrier and MOSFET type CNTFETs available for the use. The type of it chosen depends upon the type of application for which the CNTFET is considered [9-10].

IV. CASCADE VOLTAGE SWITCH LOGIC

Cascade voltage switch logic (CVSL) is a type of logic used to design the digital logic circuits. The basic concept used in this logic is that it requires both the true and complementary form of inputs. For designing the circuit, two complementary NMOS structures are designed [11]. The NMOS structure is connected to the cross coupled network pair of pull up PMOS devices. The basic design for the simple CVSL Circuits is as shown below in figure 5 [12].

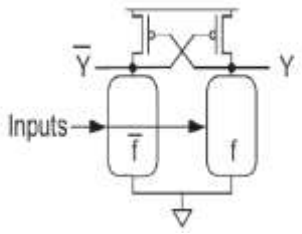

Figure 5: Basic CVSL circuit

As it is clear from the circuit, it consists of a pair of pull down N trees which are similar to one another and another pair of pull up P devices among which cross coupling is done. The 'f' is pull down network and it evaluates the logic while the $\bar{f}$ makes use of the inverted inputs that are arranged in compliment. The working principal is as explained below:

1. Whenever the circuit is triggered with input, one of the pull down network will be in ON state while the other will be in OFF state.
2. The networks that will be ON, while make the output LOW. This LOW output will turn the PMOS transistor to ON state and it will pull the other output to HIGH state.
3. When the output of the opposite network gets HIGH, the other PMOS transistor will be turned OFF. Therefore no power dissipation will occur [13].

The CVSL has following advantages that make it a great choice for designing the logic devices.

1. It offers low power dissipation as during any input cycle one of the transistor network remains in OFF state.
2. The delay time for any simulation cycle is very less, thereby enhancing the speed of the simulation.
3. It improves the on chip transistor area by reducing the number of transistor required for any circuit design [13].

V. UNIVERSAL LOGIC GATES

The universal logic gates are the logic gates that can be used to construct all logic circuits. The NAND and NOR are the two types of universal logic gates. All the gates present in the logic families can be build up using the combination of these two logic gates say it be and Inverter, AND gate or the OR logic gate. Any complex gate combination can also be constructed using the combination of these two. The logic gate taken into consideration in this research paper is the NAND logic gate. As is the name, the NAND logic gate is made using the combination of the logical AND gate and the NOT logic connected in a series combination. In simple terms the NAND gate is basically the NOT of AND logic gate or the complementary form of logical AND gate. As is seen, it is the series combination of the logical AND gate connected with the NOT gate. The symbol for the logical NAND gate and NOR gate is as shown below in figure 6.

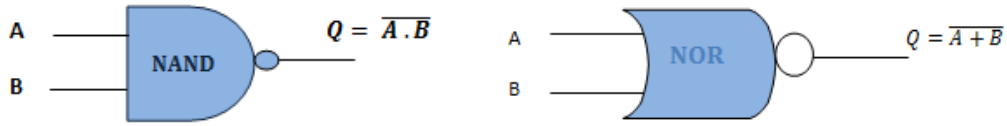

Figure 6: NAND and NOR logic gate Symbolic Representation

The logical expression for the NAND gate is as shown below in equation 1.

$$Q = \overline{A.B} \tag{1}$$

$$Q = \overline{A+B} \tag{2}$$

The truth table for the 2 input NAND gate is as shown below in table 1.

Table 1: Truth table for 2-input Universal Logic

A	B	NAND	NOR
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	0

As is seen from the truth table, that the output of the NAND logic gate is high if any input to the logic gate is low. The NAND gates are considered as the building blocks as they are used in the construction of all other logic gates. In practice it is the most commonly used logic function. This is the reason they are referred to as the "Universal Gate". The NAND gates are available in various IC packages such as 7400 IC series, 74LS00 Quadruple IC and many others [14-15].

VI. CNTFET BASED PROPOSED DESIGNS

The design and analysis of the universal logic gates is done using cascade voltage switch logic. The transistor base used is the carbon nanotubes based carbon nanotubes field effect transistors (CNTFETs). The circuits are designed using the Cadence Virtuoso simulator and the schematic chosen for the design is the 32nm Stanford CNTFET library for CNTFETs and the 90nm standard cell library for the Silicon based CVSL circuit designs. Suitable biasing is done to make the circuits fully functional. The circuits designed are the universal logic NAND and NOR gates. Firstly the NAND logic circuits are designed. The first circuit designed is the CMOS based NAND logic gate using the cascade voltage switch logic and the next circuit designed is the Carbon nanotubes field effect transistor based NAND logic gate using the cascade voltage switch logic. These circuits are as shown below in the figure 7 and 8 respectively.

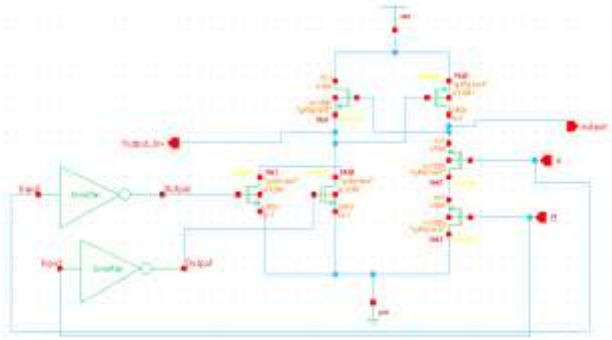

Figure 7: CMOS based NAND gate using CVSL

Figure 8: CNTFET based NAND gate using CVSL

As is seen from the above two figures, the circuit design is exactly the same for both the designs. The only difference lies in the material of the channel used. Both the circuits are implemented using the cascade voltage logic. As per the logic of CVSL, at the end of each cycle, we get two outputs. For any set of inputs, we use the true and complementary form of both the inputs for each and every cycle. Thus at the end of each cycle we get true and complemented outputs. For this circuit one is the NAND logic and the other is the inverted output of the NAND logic. That means at the end of each cycle, we get the output for the NAND as well as the AND logic. The CNTFET based circuit is used for making a comparison with CMOS based logic gate circuit. Similar to the CMOS based implementation, at the output both the NAND and AND logic are obtained. Both the circuits are compared based on a set of parameters. Similar to the NAND logic, the NOR logic is designed implementing the cascade voltage switch logic. Two circuits are designed, one NOR logic based on CMOS and the other logic based on the carbon nanotubes based FETs. The circuits designed are as shown in the figure 9 and 10 for the CMOS and CNTFET based NOR logic respectively.

Figure 9: CMOS based NOR gate using CVSL

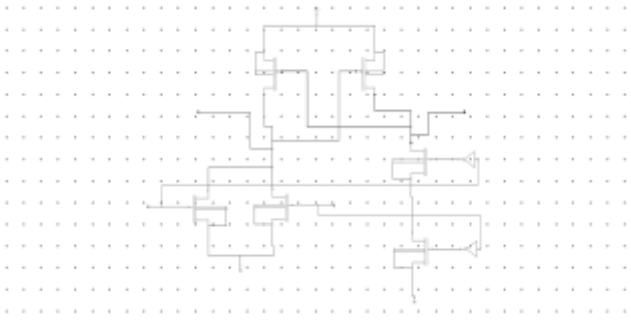

Figure 10: CNTFET based NOR gate using CVSL

VII. RESULT ANALYSIS

The analysis for the universal gates is done using the CVSL (Cascade voltage switch logic) in the Cadence Virtuoso environment. The output for both the universal logic gates are obtained. The schematic designed with the proposed logic is compared with the CMOS technology and the CNTFET based circuit. The corresponding schematic design output waveforms are as shown below in figures 11 and 12 respectively for the CNTFET based NAND and NOR logic.

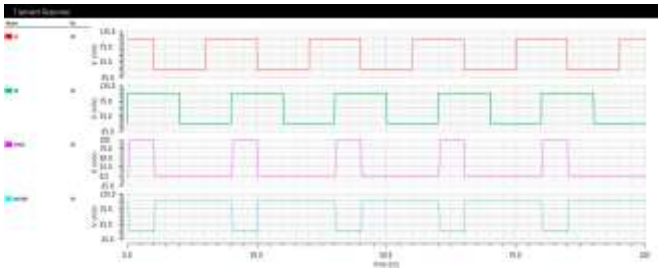

Figure 11: Waveform of CNTFET based NAND gate using CVSL waveform

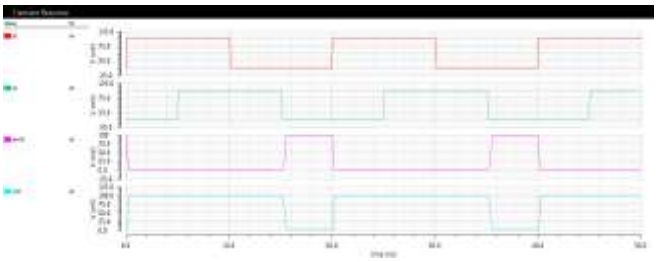

Figure 12: Waveform of CNTFET based NOR gate using CVSL waveform

To make a comparative analysis, a number of different parameters are chosen. These parameters are observed for both the CMOS and CNTFET based design of both the logic gates. The parameters taken into consideration are the delay, power consumption, power delay product. The transistor count along with the number of cycles is observed. The parametric analysis for NAND logic for both type of circuits along with the previous work done and observed summed in a tabular form is as shown below in table 2 [9]. All these parameters are observed taking the same frequency.

Table 2: Performance Analysis for NAND Logic Gate

Parameter	Previous CNTFET Work	CNTFET based NAND Gate using CVSL	CMOS based NAND Gate using CVSL
Frequency	1.00E+09	1.00E+09	1.00E+09
Power	2.83E-08	6.602E-12	13.942E-12
Delay	7.24E-13	19.43E-12	27.22E-12
PDP	2.05E-20	1.28E-22	3.79E-22

Transistor Count	10	10	10
Number of Cycles	2	1	1

It can be clearly seen from the above table that the delay obtained at the selected edge of the output and input, for conventional CMOS based NAND gate is 27.22ps which is very high as compared to the one obtained in case of the CNTFET based NOR gate which is 19.43ps. Also the power consumed by CNTFET based NAND gate is 6.60pW which is again considerably low than the CMOS based NAND gate which is 13.94pW. Now next is the parametric analysis of the NOR logic gate. The observed parameters are summed up below in the table 3.

Table 3: Performance Analysis for OR Logic Gate

Parameter	CNTFET based NOR Gate using CVSL	CMOS based NOR Gate using CVSL
Frequency	1.00E+09	1.00E+09
Power	5.97E-12	13.325E-12
Delay	18.81E-12	24.81E-12
PDP	1.12E-22	3.30E-22
Transistor Count	10	10
Number of Cycles	1	1

As is seen from the above table, the results obtained from the simulation of the proposed carbon nanotubes FETs based NOR logic gate are much more improved and efficient than the conventional CMOS based NOR logic even when the frequency and the number of transistors used are identical. The power consumption for the CNTFET based NOR logic is 5.97 pW whereas the one consumed in the CMOS based NOR logic is 13.325pW, which is very high. Also the delay occurring in the circuit is 24.81ps in case of CMOS based NOR while it is only 18.81 ps in CNTFET based NOR, which is a significant difference. Also the power delay product is almost one-third of the one in the CMOS based design.

VIII. CONCLUSION

In this work, universal logic gates, NAND and NOR logic are designed, simulated, analyzed and compared. From the observations summed up in the table 2 and 3, it is very much apparent that the power consumption in case of the CNTFET is almost 50% less than that in the case of the conventional CMOS based NAND logic and 55% less in NOR logic, in spite of designing them using the same logic which is cascade voltage switch logic, which is a significant improvement in the design. Also it is observed that the in comparison to previously design CNTFET based NAND gate, the CVSL based CNTFET circuits have shown a benchmark improvement in all the parameters. The time delay in the circuit is also reduced significantly to about 40% less than the conventional CMOS based circuit for NAND and 24% less in NOR logic. Thus the proposed design of the universal gates gate using CNTFET have shown a significant improvement in the design parameters when even the number of transistors used and the logic implemented are the same. Thus the CNTFETs can be used further in the design of much more complex and larger circuits with parameters having much better performance than the conventional CMOS based circuits.

IX. REFERENCES

[1] B.K. Kaushik, M.K. Majumder, "Carbon Nanotubes Based VLSI Interconnects", Springer Briefs in Applied Sciences and Technology, pp. 17-37, 2015.

[2] Rajendra Prasad Somineni, Y Padma Sai, S Naga Leela, "Low leakage cntfet full adders", IEEE Proceedings of Global Conference on Communication Technologies, pp. 174-179, April 2015.

[3] Swati Sharma, Rajesh Mehra, "Area & Power Efficient Design of XNOR-XOR Logic Using 65nm Technology", National Conference on Synergetic Trends in engineering and Technology, pp. 57-60, April 2014.

[4] Atheer Al-Shaggah et. All, "Carbon Nanotubes Field effect Transistor Models Performance and Evaluation", IEEE Jordan Conference on Applied Electrical Engineering and Computing Technologies, pp. 8-13, December 2013.

[5] Ronak Zarhoun, Mohammad Hossein Moaiyeri, Samira Shirinabadi Farahani, and Keivan Navi, "An Efficient 5-Input Exclusive-OR Circuit Based on Carbon Nanotubes FETs", Electronics and Telecommunications Research Institute Journal, Volume 36, Number 1, pp. 89-98, February 2014.

[6] Tanuja Dogra, Rajesh Mehra, "Design Analysis Of Nand Gate Using Cascode Voltage Switch Logic", National Conference on Advancement in Solid State Devices & Circuits, pp. 43-45, March 2013.
[7] Sanjeet Kumar Sinha, Saurabh Chaudhury, "Advantage of CNTFET Characteristics Over MOSFET to Reduce Leakage Power", IEEE International Conference on Devices, Circuits and Systems, pp. 1-5, March 2014.
[8] Sheng Lin, Yong-Bin Kim, Fabrizio Lombardi "CNTFET-Based Design of Ternary Logic Gates and Arithmetic Circuits", IEEE Transaction on Nanotechnology, Volume 10, Number 2, pp. 217-225, March 2011.
[9] Anjali Sharma, Richa Sharma, Rajesh Mehra, "Low power TG full adder design using CMOS nanotechnology", IEEE International Conference on Parallel, Distributed and Grid Computing, pp. 210-213, December 2012.
[10] Ali Keshavarzi, Arijit Raychowdhury, Juanita Kurtin, et al., "Carbon Nanotubes Field-Effect Transistors for High-Performance Digital Circuits—Transient Analysis, Parasitics, and Scalability", IEEE Transactions on electron devices, Volume 53, Number 11, pp. 2718-2726, November 2006.
[11] Dae Woon Kang, Yong Bin Kim, "Design of Enhanced Differential Cascade Voltage Switch Logic (EDCVSL) Circuits for High fan In Gate", IEEE transactions, pp. 309-313, September 2002.
[12] Mitali Sharma, Rajesh Mehra, " Design Analysis of Full Adder Using Cascade Voltage Switch Logic", IOSR Journal of VLSI and Signal Processing, Volume 6, Issue 3,pp. 18-23, May-June 2016.
[13] Hiroshi Hatano, "SET Immune Spaceborne CVSL and C^{2}VSL Circuits", Journal of Electrical and Control Engineering, Volume 3, Issue 5, pp. 43-48, 2013.
[14] Hiroshi Hatano, "Single Event Effects on Static and Clocked Cascade Voltage Switch Logic (CVSL) Circuits", IEEE Transactions On Nuclear Science, Volume 56, Issue 4, pp. 1987-1991, August 2009.
[15] Amin Vanak, Reza Sabbaghi Nadooshan, "Improvement of Power and Performance in NAND and D-Latch Gates using CNTFET Technology", Journal of Nano Research, Volume 33, pp. 126-136, 2015.
[16] M. Haykel Ben-Jamaa, Kartik Mohanram, Giovanni De Micheli, "An Efficient Gate Library for Ambipolar CNTFET Logic", IEEE Transactions on Computer-aided design of integrated circuits and systems, Volume 30, Number 2, pp. 242-255, February 2011.
[17] Dhananjay E. Upasani, Sandip B. Shrote, Pallavi S.Deshpande, "Analysis of Universal Logic Gates Using Carbon Nanotubes Field Effect Transistor", International Journal of Computer Applications, Volume 7, Issue 6, pp. 29-33, September 2011.

X. **AUTHORS**

Er. Mitali Sharma is currently pursuing M.E degree from National Institute of Technical Teachers Training and Research, Chandigarh India. She has completed her B. Tech from M.M. University, Mullana, India. She is having a total of six years of experience of industry and teaching experience. Her areas of interest include Advanced Digital Signal Processing, Wireless Networks and Image Processing.

Dr. Rajesh Mehra is currently associated with Electronics and Communication Engineering Department of National Institute of Technical Teachers' Training & Research, Chandigarh, India since 1996. He has received his Doctor of Philosophy in Engineering and Technology from Panjab University, Chandigarh, India in 2015. Dr. Mehra received his Master of Engineering from Panjab Univeristy, Chandigarh, India in 2008 and Bachelor of Technology from NIT, Jalandhar, India in 1994. Dr. Mehra has 20 years of academic and industry experience. He has more than 325 papers to his credit which are published in refereed International Journals and Conferences. Dr. Mehra has guided 75 ME thesis. He is also guiding 02 independent PhD scholars. He has also authored one book on PLC & SCADA. He has developed 06 video films in the area of VLSI Design. His research areas are Advanced Digital Signal Processing, VLSI Design, FPGA System Design, Embedded System Design, and Wireless & Mobile Communication. Dr. Mehra is member of IEEE and ISTE

Mitali Sharma. "Carbon Nanotube FET based high performance Universal logic using Cascade Voltage Switch Logic." IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) , vol. 7, no. 5, 2017, pp. 40–47.