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FPGA Implementation of High Speed Carry Select Adder Design Using Spartan

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Abstract: *The binary addition is the basic arithmetic operation in digital circuits and it became essential in most of the digital systems including ALU, microprocessors and DSP. Adders are the basic building blocks in digital integrated circuit based designs. Ripple Carry Adder (RCA) gives the most compact design but takes longer computation time. The time critical applications use Carry Look-ahead scheme (CLA) to derive fast results but they lead to increase in area.*
Carry Select Adder is a compromise between RCA and CLA in term of area and delay. This paper focuses on the FPGA implementation of carry select adder design using Spartan xc3s50pq208-4 based on Multiplexer using Verilog. The delay and power is minimized. The proposed architecture of carry select adder is synthesized in Xilinx ISE14.7and implemented in Xilinx ISE 10.1 on Spartan xc3s50pq208-4.

Keywords: *Carry select adder, Multiplexer, Full adder, Verilog, FPGA, Spartan, Power, delay, Xilinx ISE14.7, Xilinx ISE10.1.*

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I. Introduction

The addition is the most common and often used arithmetic operation on microprocessor, digital signal processor, especially digital computers. Also it serves as a building block for synthesis all other arithmetic operations. In digital adders, the speed of adders is limited by the required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The major speed limitation in any adder is in the production of carries. The carry select adder is used in many computational systems to moderate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. Power consumption is an important efficiency factor in designing very large scale integrated (VLSI) circuit. Moreover with the explosive growth of VLSI technology the demand and popularity of portable devices has driving designers to strive for smaller silicon area. The central electronic circuit used for addition is adder. Adders are fundamental for wide variety of digital system. Many adders exist but the fast adding with Low area and Power still challenging [1]. There are different types of adders such as Ripple carry adder, carry skip adder, carry look ahead adder, carry save adder, etc. among them RCA shows compact design but their computation time is longer. It has lowest speed amongst all adders because it has large propagation delay but occupy less area. Then, in CLA can derive fast result but it leads to increase in area, among these adders CSLA have small area but delay is increased due to ripple carry adder.

II. Proposed work

The carry-select adder generally consists of two ripple carry adder and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known. The number of bits in each carry select block can be uniform, or variable When variable, the block size should have a delay, from addition inputs ‘a’ and ‘b’ to the carry out, equal to that of the multiplexer chain leading into it, so that the carry out is calculated just in time. The delay is derived from uniform sizing, where the ideal number of full-adder elements per block is equal to the square root of the number of bits being added, since that will yield an equal number of Mux delays. However, the carry select adder is not area efficient because it uses multiple pairs of Ripple Carry Adders to generate partial sum and carry by considering carry input and then the

final sum and carry are selected by the multiplexers. This design has efficiently implemented on FPGA Spartan board xc3s50pq208-4.

The factors which are desirable in adders are as follows:

- High speed(Less delay 9.97ns)
- Low power consumption(24mW)

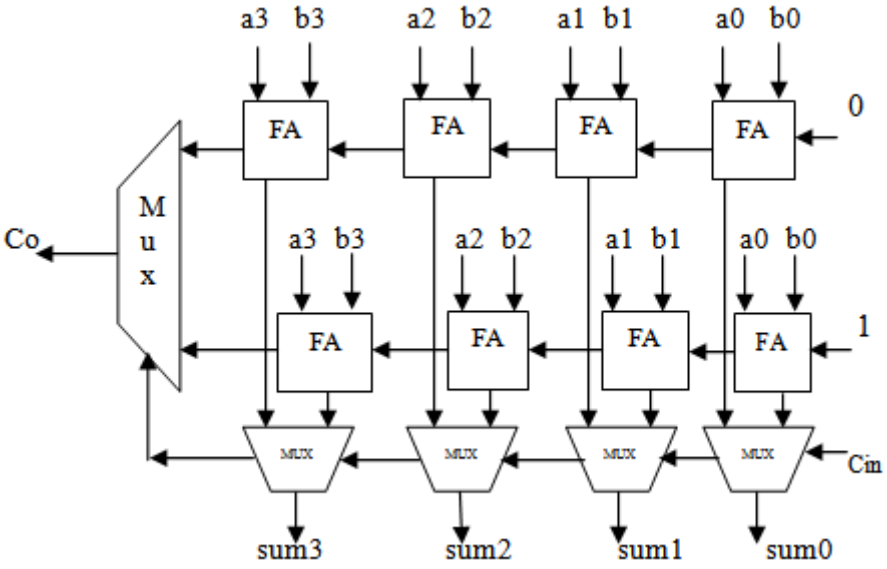

Figure1: Architecture of Carry select adder

III. Implementation Setup of Carry Select Adder

Figure 2: Complete setup of carry select adder

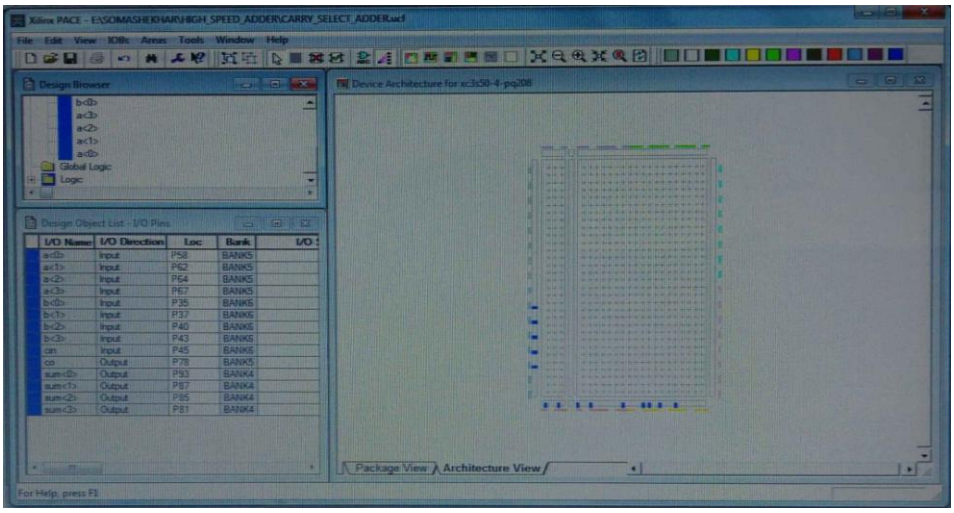

Figure 3: User constraints file (UCF) generation

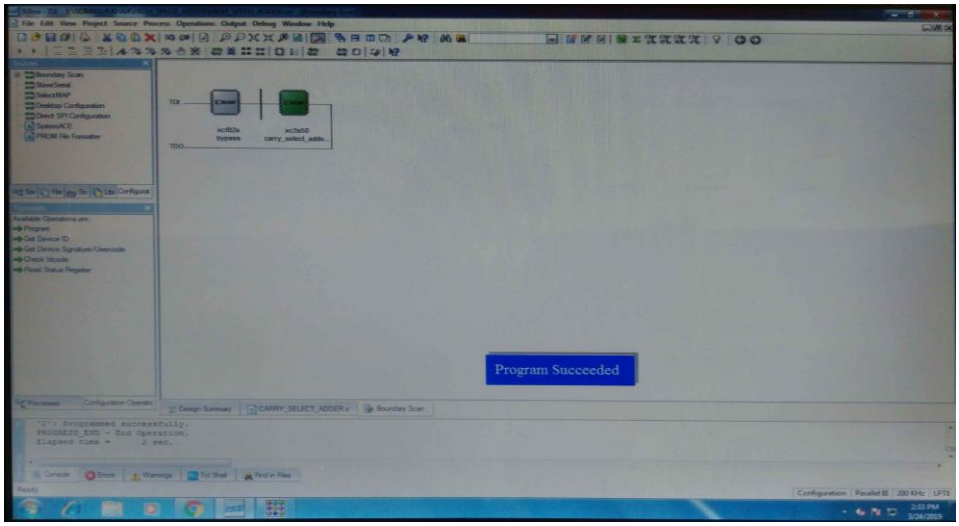

Figure 4: Boundary scan checking

IV. Results

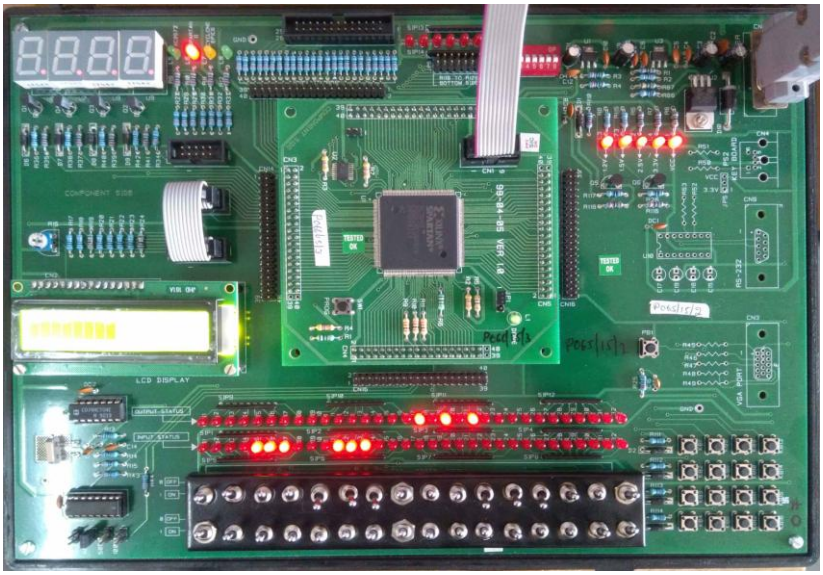

Figure 5: FPGA implementation results on SPARTAN xc3s50pq208-4

The figure 5 shows the output of carry select adder. Three inputs a, b and cin and two outputs sum and co. Here input a=0111, b=1110 and cin=0 then output sum=0101 and co=1.

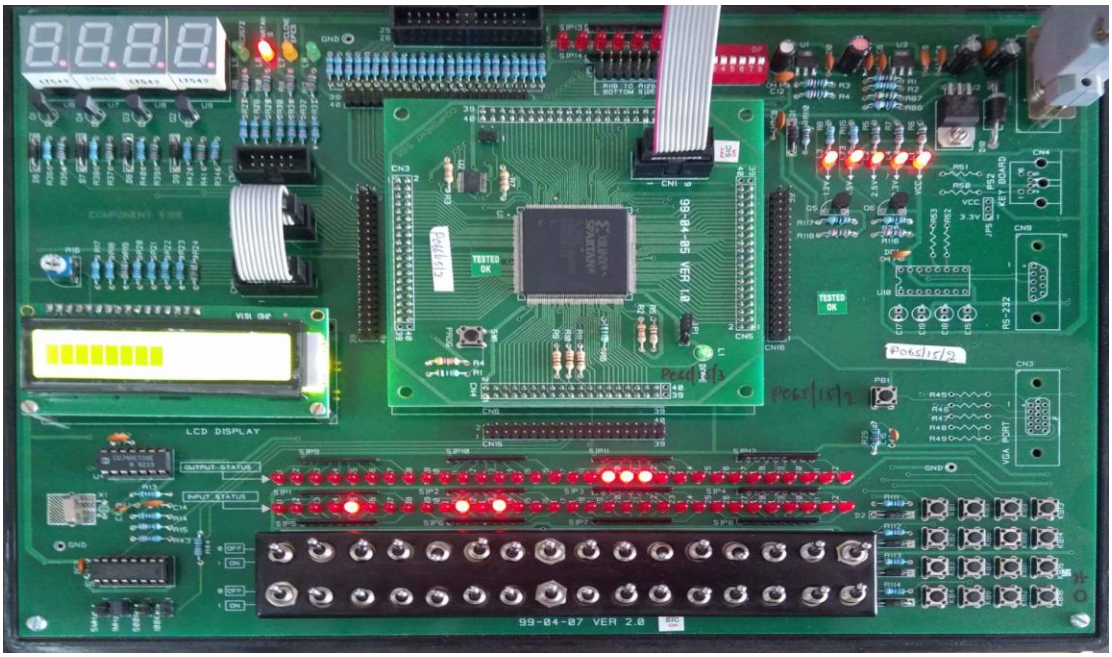

Figure 6: FPGA implementation results on SPARTAN xc3s50pq208-4

The above figure 6 shows the output of carry select adder. Three inputs a, b and cin and two outputs sum and co. Here input a=0100, b=1010 and cin=0 then output sum=1110 and co=0.

Synthesis results

Design	E:\SOMASHEKHAR\HIGH_SPEED_ADDER\CARRY_SELECT_ADDER.ncd		
Preferences	CARRY_SELECT_ADDER.pcf		
Part	3s50pq208-4		
Data version	ADVANCED,v1.0,11-03-03		
Power summary		I(mA)	P(mW)
Total estimated power consumption			24
Total Vccint	1.20V	5	6
Total Vccaux	2.50V	7	18
Total Vcco25	2.50V	0	0
Inputs		0	0
Logic		0	0
Outputs			
Vcco25		0	0
Signals		0	0
Quiescent Vccint	1.20V	5	6
Quiescent Vccaux	2.50V	7	18

Estimated power consumption: 24mW

Delay: 9.970ns (7.306ns logic, 2.664ns route) (73.3% logic, 26.7% route)

V. Conclusion

Delay, Power is the constituent factors in VLSI design that limits the performance of any circuit. This paper presents a implementation of Carry select adder architecture. The proposed design of carry select adder is synthesized in Xilinx ISE 14.7, FPGA implemented on Spartan xc3s50pq208-4 and the source code is written in Verilog. This proposed carry select adder has delay 9.970ns and power 24mw.

References

[1]. Somashekhar Malipatil, R. Basavaraju and Praveen kumar Nartam. "Low Power & High Speed Carry Select Adder Design Using Verilog", IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 6, Issue 6, Ver. II (Nov. - Dec. 2016), PP 77-81 e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197.

[2]. Bejagam Divya, Alekhya Bonkuri, Madhavi Bandi, Somashekhar Malipatil, "Design and verification of low power and high speed carry select adder using Verilog", International Journal of Creative Research Thoughts (IJCRT), ISSN:2320-2882, Volume.6, Issue 1, Page No pp.1786 - 1790, March 2018.

[3]. B. Ramkumarnd Harish M Kittur, "Low Power and Area Efficient Carry Select Adder" IEEE Transactions on Very Large Scale Integration (VLSI) Systems, VOL. 20, NO. 2, February 2012.

[4]. B. Ramkumar, Kittur, H.M. and Kannan, P. M. (2010) "ASIC Implementation of Modified Faster Carry Save Adder", Eur. J. Sci. Res., Vol.42, No.1, pp.53–58.

[5]. C.S.Manikandababu "An Efficient CSLA Architecture for VLSI Hardware Implementation" IJMIE, ISSN: 2249-0558, Volume 2, Issue 5, 2012, pp.610-622.

[6]. Arunprasath S et al., "VLSI Implementation and Analysis of Parallel Adders for Low Power Applications", International Journal of Computer Science and Mobile Computing, Vol.3 Issue.2, February- 2014, pg. 181-186.

[7]. Shivani Parmar and Kirat Pal Singh,"Design of High Speed Hybrid Carry Select Adder", IEEE's 3rd international advance Computing Conference Ghaziabad, ISBN: 978-1-4673-4527-9, 22-23 February2013.

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