

# High Speed and Area Efficient Carry Select Adder Using Carry Skip Logic

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**Abstract:** For any data processing unit, addition is the basic operation to be performed by the adder. But the speed is limited due to carry propagation delay of the adder. Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. Area of regular CSLA can be reduced by using CSLA BEC architecture. This paper presents uniform CSLA (UCSLA) with a modification in the first set of RCA with  $C_{in}=0$ , which can be replaced with carry skip adder (CSKPA) so that delay can be reduced much as compared to CSLA BEC. By considering equal number of input bits to each group of CSLA, the area and power can be reduced efficiently. This work estimates the performance of the proposed designs with the regular designs in terms of delay and area. The proposed design is implemented in Xilinx-14.6. The results analysis shows that the proposed uniform CSLA structure is better than the regular CSLA, CSLA BEC.

**Keywords**– Area, BEC, CSKPA, CSLA, Delay, MUX, Power, RCA, UCSLA.

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## I. Introduction

Any data path logic system needs fastest data processing processors. Speed of processor depends on the speed of arithmetic computational units. Basic operation of any computational unit is addition whose speed is restricted because of carry propagation delay of adder [1]. The digital adders suffer not only with the problem of carry propagation delay but also with power dissipation which is one of the most important design objectives in integrated circuits [2]. The very basic adder is ripple carry adder (RCA) which is slowest even though it is very compact in design and occupies less area. Whereas carry look-ahead adder (CLA) is the fastest one but consumes more area [3]. Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions [4]. While comparing the adders we found out that RCA had a smaller area while having lesser speed, in contrast to which CLA had high speed but possesses a larger area [5]. But CSLA is having a proper tradeoff between time and area complexities. The CSLA uses dual set of RCA to generate partial sum and carry by considering carry input  $C_{in}=0$  and  $C_{in}=1$ , then the final sum and carry are selected by the multiplexer [6]. The multiplexer is used to produce the final sum according to the carry propagated by the previous stage. The carry select adder achieves low power and area efficient with an increase in delay [7, 8]. CSLA BEC shows reduction in area and power consumption in comparison with conventional CSLA with a higher delay [9, 10]. In this paper, uniform CSLA (UCSLA) is proposed in which first set of RCA with  $C_{in}=0$  in CSLA BEC is replaced with carry skip adder (CSKPA) for further reduction in area and also delay. The result shows that the proposed uniform CSLA is better than CSLA BEC. In this paper uniform carry select adder (UCSLA) is proposed to reduce the area, power and delay.

This paper is structured as follows. Section II deals with carry skip adder (CSKPA). Section III explains the evaluation methodology of area and delay of basic blocks used in proposed UCSLA architecture. Section IV deals with structure of UCSLA. Section V explains the evaluation methodology of area and delay of UCSLA architecture. Comparison and simulation results are analyzed in Section VI. Section VII concludes the proposed work. Section VIII briefs about the future scope of the proposed work.

## II. CSKPA

Carry skip adder is designed to achieve minimum delay. A fast carry look-ahead logic using group propagate functions is used to speed up the performance of multiple stages of ripple carry adders. The group propagate functions are generated in parallel with the carry generation for each block by using full adder with propagate signal pin (p) as shown in Fig 1. The new architecture generates the sum and carry outputs with minimum delay are shown in Fig 2. The Fig 3 shows the 4-bit-carry-skip adder consists of a 4-bit-carry-ripple-chain, a 4-input AND-gate and one multiplexer. This greatly reduces the latency of the adder through its critical

path, since the carry bit for each block can now "skip" over blocks with a *group* propagate signal set to logic 1. The number of inputs of the AND-gate is equal to the width of the adder.

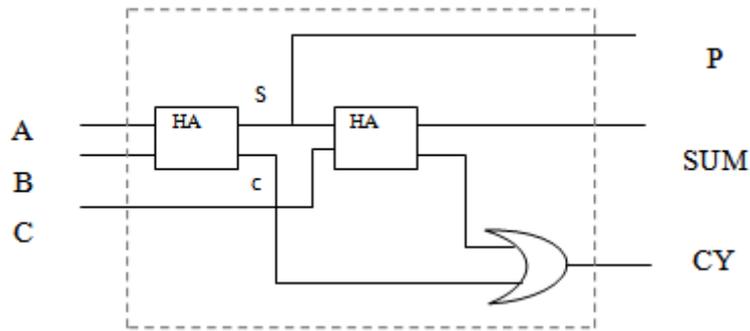


Fig 1: Full adder with propagate signal

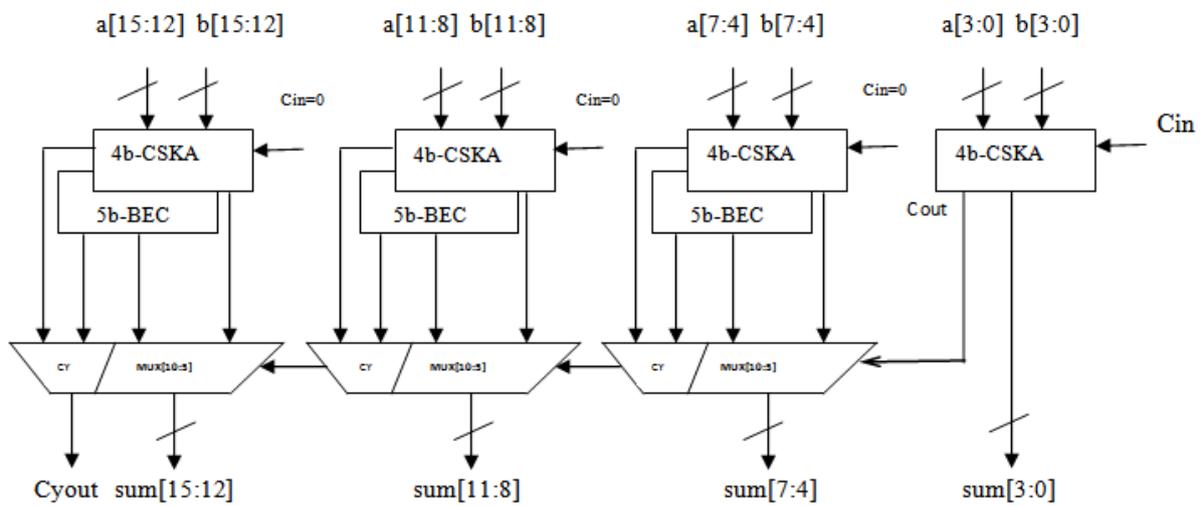


Fig 2: 16 bit uniform carry select adder(UCSLA)

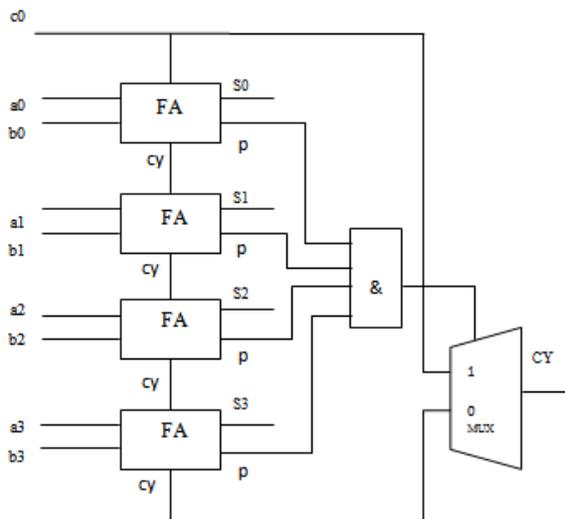


Fig 3: 4 bit carry skip adder

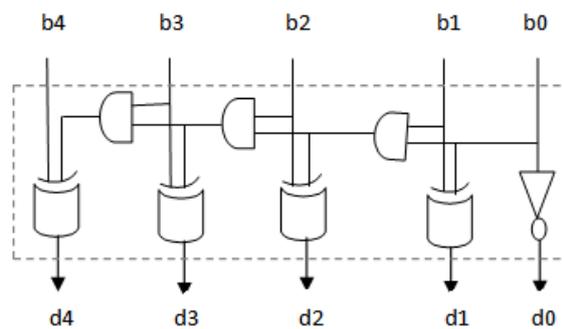


Fig 4: 5 bit BEC logic

**Table 2.** Estimated area and delay evaluation of basic blocks of UCSLA

Group	Max Delay	Area
Group 1	7	43
Group 2	10	82
Group 3	13	82
Group 4	16	82
total		<b>289</b>

### III. Area and Delay Evaluation of Basic Blocks

The consideration of area and delay evaluation can be done by basic logic gates each having delay equal to 1 unit and area equal to 1 unit. The longest path in the combinational logic block represents its maximum delay by considering total number of gates presented in that path. Area can be evaluated by counting total number of gates in the combinational logic blocks. AND, OR, and INVERTER implementation of 5 bit BEC logic block is shown in Fig. 4. Area delay evaluation of modified half adder (HA), full adder (FA), CSKPA and multiplexer is mentioned in table 1. This approach evolves the total area and delay of UCSLA adder blocks.

### IV. Uniform CSLA

The structure 16 bit UCSLA is proposed for optimization of delay and area is as shown in fig. 2. This structure is again split into four groups. Each group is having equal number of input bits. Group 1 consists of 4 bit CSKPA which is shown in fig 3. Remaining groups are designed CSKPA with  $C_{in} = 0$  is shown in fig 5 and BEC logic with  $C_{in} = 1$  is shown in fig 4 to produce partial sum and carry. Finally, multiplexers are used to produce final sum and carry

### V. Area And Delay Evaluation Methodology of UCSLA

The procedure of area and delay estimation of each group of the proposed UCSLA architecture is similar to the evaluation of CSLA BEC [6]. The proposed design uses CSKPA, 5 bit BEC to generate multiple partial sum and carries. Special feature of the proposed UCSLA is that, it is having less number of gates and produces minimum delay, hence area and delay reduced to a great extent.

Estimation of maximum delay of UCSLA architecture is similar to the delay estimation of 16 bit CSLA BEC [6]. Delay in UCSLA depends on the type of input bit stream applied. The estimated area and delay of each group of UCSLA is listed in table 2. Area and delay comparison of UCSLA with SQR CSLA and SQR CSLA BEC is mentioned in table 3. By referring Tables 2 and 3, it is clear that, the gate count and delay in proposed UCSLA architecture is reduced effectively.

Area evaluation has been determined as follows

**BEC5:-**

$$\text{Gate count} = (\text{XOR} * 4) + \text{AND}(3) + \text{NOT} + \text{MUX}(5)$$

$$= (5 * 4) + 3 + 1 + (4 * 5) = \mathbf{44}$$

**Group1:-**

$$\text{Gate count} = (\text{FA} * 4) + (\text{AND} * 3) + (\text{MUX} * 1)$$

$$= (9 * 4) + 3 + 4 = \mathbf{43}$$

**Group2, Group3, Group4:-**

$$\text{Gate count} = \text{HA} + (\text{FA} * 3) + (\text{AND} * 3) + (\text{MUX} * 1) + \text{BEC5}$$

$$= 4 + (9 * 3) + 3 + 4 + 44 = \mathbf{82}$$

$$\text{Total gate count} = 43 + (82 * 3) = \mathbf{289}$$

(Refer table II for individual gate areas of UCSLA architecture)

**Table 3.** Delay and area evaluation for basic blocks of UCSLA

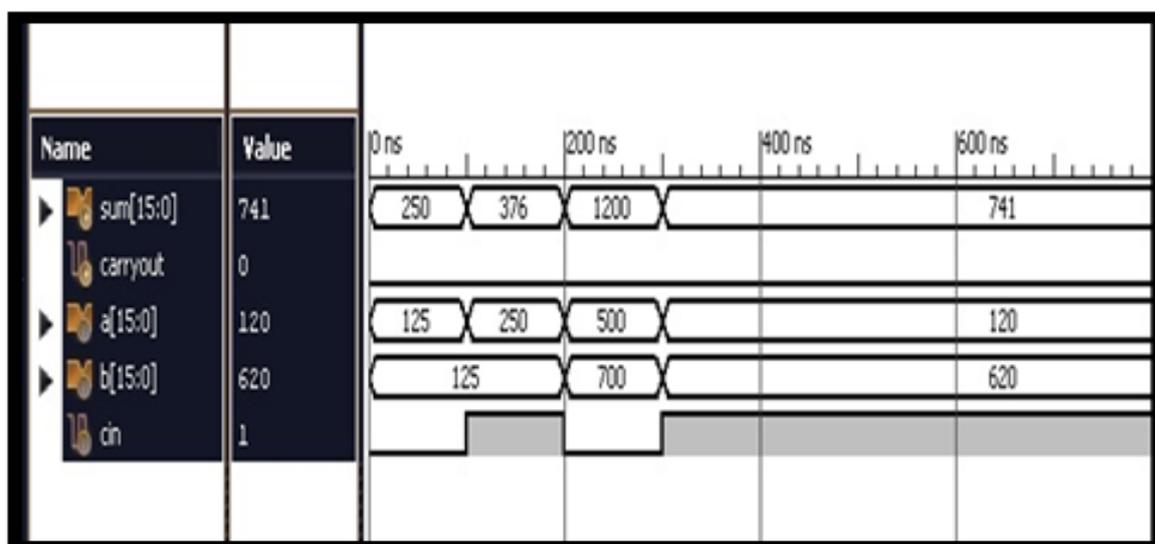
PARAMETER	CSLA2RCA	CSLA BEC	UCSLA
GATE AREA	434	336	289
DELAY(ns)	20.661	18.481	11.884
AREA DELAY PRODUCT	8966.874	6209.616	3434.476

### VI. Result Analysis

Efficiency evaluation of the UCSLA can be done by comparing different parameters like gate area, delay and area-delay product in the SQR CSLA, CSLA BEC and the proposed UCSLA architecture as shown in the table 3. From Table 3, it is clear that, the proposed *16-bit UCSLA saves 145, 47* gate area than SQR CSLA, CSLA BEC respectively. Delay of proposed UCSLA is reduced by 8.77 ns, 6.59 ns than SQR CSLA, CSLA BEC respectively. Area-delay product of proposed UCSLA is reduced by 5532.398, 2775.14 than SQR

CSLA, CSLA BEC respectively. So the proposed design has given better results as compared to existing designs.

For further evaluation of the UCSLA performance, we have resorted to ASIC implementation and simulation. The design proposed in this paper is implemented using VERILOG, simulated using *ISim* simulator completely synthesized using *XILINX XST* and successfully tested using *XILINX 14.6, SPARTAN 3E* series. Simulation result of proposed CSLA is shown in fig. 6.



**Fig.6.**simulation result

### VII. Conclusion

Simple carry skip logic is introduced in this paper which leads to change in the SQR CSLA architecture to reduce area and delay. This work offers the advantage of reduction in total cell area and total power. The proposed UCSLA is concluded as area and delay efficient design for VLSI implementation as compared with SQR CSLA, CSLA BEC.

### VIII. Future Scope

The proposed UCSLA design is implemented for 16 bit word size and parameters like area, delay and area delay product is evaluated. This work can be extended for increasing input bit length like 32 bit, 64 bit, 128 bit and so on.

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