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Fm0/Manchester/Miller Encoding for Intelligent Dsrc Transportation System

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Abstract *:* The dedicated short-range communication (DSRC) is an emerging technique and to push the intelligent transportation system into our daily life. The DSRC standards generally adopt FM0 and Manchester codes to reach dc-balance, enhancing the signal reliability. The codeword structure of FM0 and Manchester are different, thus limiting the hardware potential of existing DSRC systems. In this paper similarity oriented logic simplification (SOLS) technique is used for fully re-used architecture. In this paper we introduced another encoding type (i.e miller encoding) for DSRC application. The behavior of the Manchester encoder, FM0 encoder and Miller encoder architecture is realized by derivation of Verilog Hardware Description Language (HDL) code in Quartus II software. Utilizing the ModelSim Altera, the encoder architecture is simulated to observe its functionality. This encoding technique fully supports DSRC standards of America, Europe and Japan. This paper proposes the technique to improve reliable performance over existing DSRC systems.
Keywords: *FM0, MANCHESTER AND MILLER ENCODING, DSRC,SOLS*

I. INTRODUCTION

Dedicated short-range communications are one-way or two-way short-range to medium-range wireless communication channels specifically designed for automotive use and a corresponding set of protocols and standards. Dedicated Short Range Communications (DSRC) is a general purpose RF communications link between the vehicle and the roadside, or between two vehicles. The set of standards developed to support this interface provide a short to medium range communications service for a variety of applications, including public safety (obstacle detection, collision warnings and avoidance, intersection safety), commercial vehicle applications (weigh-in-motion/inspection clearances, border crossing), electronic toll collection, parking lot payment, in-vehicle signing, and many others

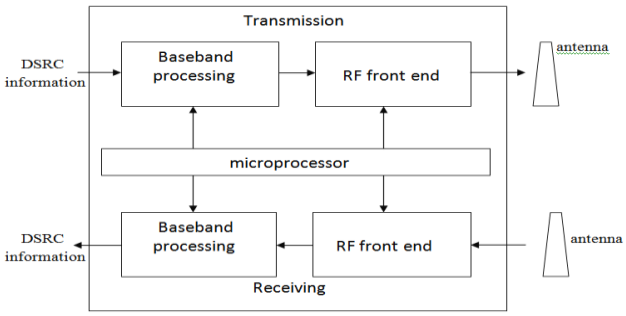

Figure1. System architecture of DSRC transceiver

The system architecture of DSRC transceiver is shown in Fig. 1. The upper and bottom parts are dedicated for transmission and receiving, respectively. This transceiver is classified into three basic modules: microprocessor, baseband processing, and RF front-end. The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end. The baseband processing is responsible for modulation, error correction, clock synchronization, and encoding. The RF frontend transmits and receives the wireless signal through the antenna

II. EXISTING SYSTEM

The purpose of SOLS technique is to design a fully reused VLSI architecture for FM0 and Manchester encodings. The SOLS technique is classified into two parts: area-compact retiming and balance logic-operation sharing. the architecture of SOLS based Fm0 Encoder and Manchester Encoder is shown in Fig. 2. The XOR in the logic for B(t)/X is translated into the XNOR with an inverter, and then this inverter is shared with that of the

logic for A(t)/X. This shared inverter is relocated backward to the output of MUX−1. Thus, the logic computation time between A(t)/X and B(t)/X is more balance to each other. The adoption of FM0 or Manchester code depends on Mode and CLR. In addition, the CLR further has another individual function of a hardware initialization

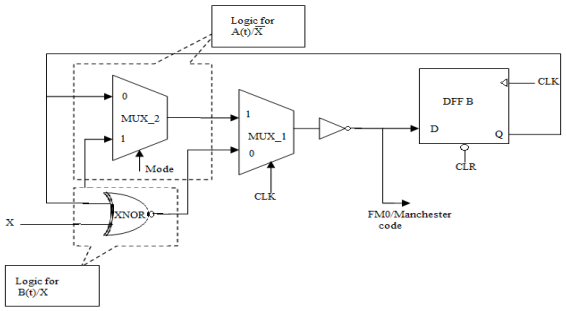

Fig 2: FMO/MANCHESTER ARCHITECTURE

FM0 Code: Mode=0 and CLR=1
Manchester Code: Mode=1 and CLR=0

Figure 2. VLSI Architecture Design of Existing Fm0 Encoder and Manchester Encoder using SOLS Technique

A(t) and B(t) represent the discrete-time state code of current-state at time instant t. Their previous-states are denoted as the A(t − 1) and the B(t − 1), respectively.A(t) and B(t) are given as With both A(t) and B(t), the Boolean function of FM0 code is denoted as

$$CLK\ A(t) + B(t)$$

As mentioned previously, the Manchester encoding can be derived from $X \oplus CLK$, and it is also equivalent to

$$X \oplus CLK = CLK + X$$

If the CLR is simply derived by inverting Mode without assigning an individual CLR control signal, this leads to a conflict between the coding mode selection and the hardware initialization. To avoid this conflict, both Mode and CLR are assumed to be separately allocated to this design from a system controller. Whether FM0 or Manchester code is adopted, no logic component of the proposed VLSI architecture is wasted. Every component is active in both FM0 and Manchester encodings. Therefore, the HUR of the proposed VLSI architecture is greatly improved

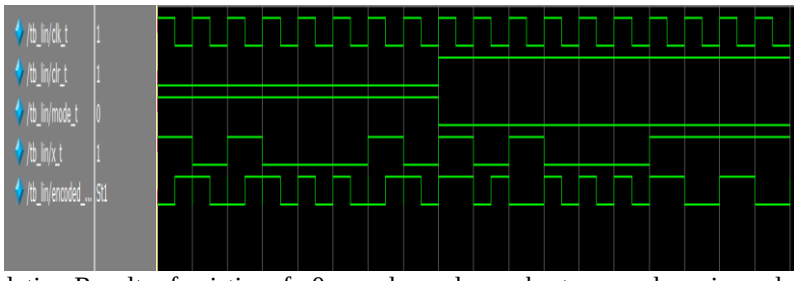

Figure 3.Simulation Result of existing fm0 encoder and manchester encoder using sols technique

III. PROPOSED SYSTEM

In our proposed system, Miller encoder is also implemented with FM0 and Manchester encoder. The characteristic of the Miller encoding is similar to that of FM0/Manchester encoding so we can use the Miller encoding for Dedicated Short Range Communication.

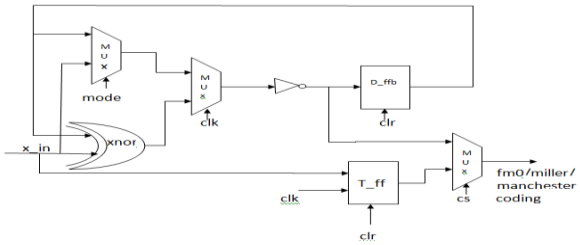

Fig 4: Proposed System Architecture

FM0 Code: Mode=0 , CLR=1 and CS=0
Manchester Code: Mode=1 , CLR=0 and CS=1
Miller Code : Mode=0,CLR=1 and CS=1
Figure 4. VLSI Architecture Design of Proposed Fm0 Encoder ,Manchester Encoder and Miller Encoder
This is the diagram for the FM0/Manchester and Miller encoding. Here the output of the proposed system is depend on the control signal (cs). If the control signal (cs) is 1 , output is FM0/Manchester encoding otherwise output is Miller encoding. For FM0 signals mode is 0 ,clr is 1 and cs is 1. For Manchester signal mode is 1 , clr is 0 and cs is 1. For Miller encoding , mode is 1 , clr is 0 and cs is 0.

In addition, the CLR further has another individual function of a hardware initialization. If the CLR is simply derived by inverting Mode without assigning an individual CLR control signal, this leads to a conflict between the coding mode selection and the hardware initialization. To avoid this conflict, both Mode and CLR are assumed to be separately allocated to this design from a system controller. Whether FM0 or Manchester code is adopted, no logic component of the proposed VLSI architecture is wasted. Every component is active in both FM0 and Manchester encodings. Therefore, the HUR of the proposed VLSI architecture is greatly improved

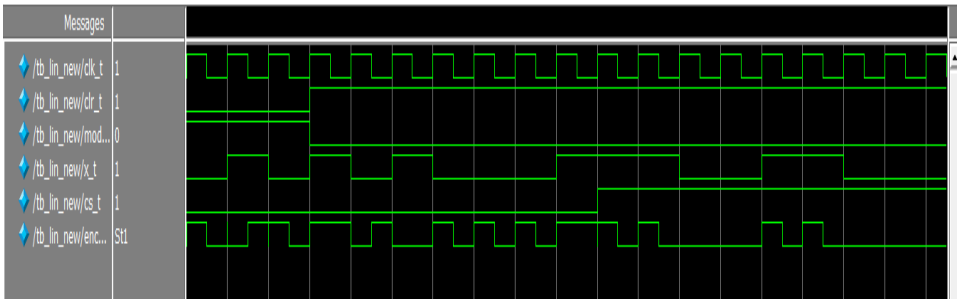

Figure 5.Simulation Result of proposed fm0 encoder manchester encoder and miller encoder using sols technique

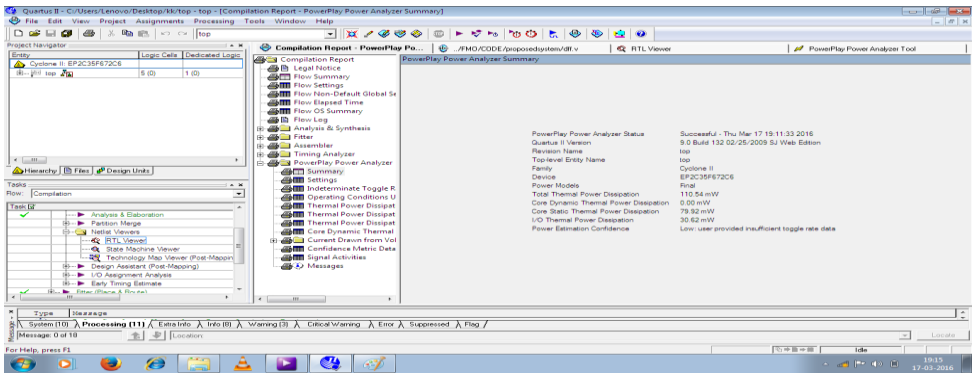

Figure 6. Power report of proposed fm0 encoder manchester encoder and miller encoder using sols technique

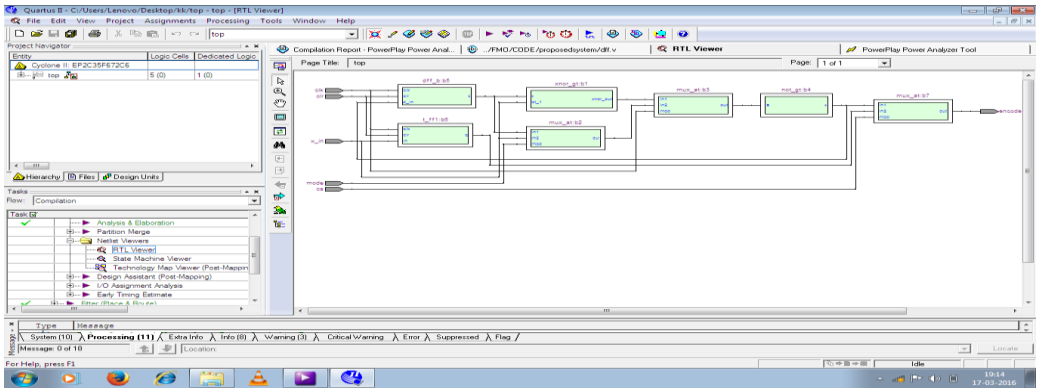

Figure 7. RTL View of proposed fm0 encoder manchester encoder and miller encoder using sols technique

IV. CONCLUSION

In this paper Miller encoding is integrated with FM0 and Manchester encoding architecture for the application of Dedicated Short Range Communication (DSRC). These three encodings have same similarities and clock rate embedded within the transmitted data. Using similarities in the FM0, Manchester and Miller techniques, hardware architecture is to be develop using SOLS technique. The encoding capability of this paper can fully support the DSRC standards of America, Europe, and Japan. This paper not only develops a fully reused VLSI architecture, but also exhibits a competitive performance compared with the existing works

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