IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)
e-ISSN: 2278-2834,p-ISSN: 2278-8735
PP 55-59
www.iosrjournals.org

Design And Implementation Of Reversible Logic Alu With 4 Operations

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Abstract: *Now days most of the circuits which are going to be designed to perform any specific or safety critical operations are mainly based upon the digital domain, where microprocessors and microcontrollers plays an important role to design these digital circuits. ALU is the heart of these processors. By optimizing this co-processor a highly efficient digital processor can be obtained. So this paper is totally devoted to design speed, area and power efficient Arithmetic Logic Unit. Speed of ALU is greatly depends upon the speed of multiplication unit. There are so many multiplication techniques have been devised at algorithmic and structural level. A new VLSI architecture for ALU using reversible logic gates is proposed. ALU is one of the most important components of CPU that can be part of a programmable reversible computing device such as a quantum computer. This paper presents design concept of 4-bit arithmetic and logic unit (ALU). Design methodology has been changing from schematic design to HDL based design.*

Keywords: *ALU, adders, multiplier, subtractor, logic gates and cadence tool.*

I. Introduction

The arithmetical operations are playing vital role in DS (digital system) like process controllers, image processing, signal processor, computers and computers graphics. Recent Technology advancement for IC's is making arithmetic suitable on large scale for implementation of VLSI [1]. In the digital electronics, arithmetic and logic operations are getting the delay, High Circuit complexity, and high power consumption problem.

The ALU, or the arithmetic and logic unit is the section of the processor that is involved with executing operations of an arithmetic or logical nature. Reversible are circuits (gates) that have the same number of inputs and outputs and there is a one-to-one mapping between vectors of inputs and outputs. Thus the vector of input states can be always uniquely reconstructed from the vector of output states. Because truly low power circuits cannot be built without the concepts of reversible logic, various technologies and circuits for reversible logic are recently being studied [2].

A simple ALU consists of two operands, one control signal to select the operation to be performed and one output signal to give the result of desired operation. Reversible ALU is designed for modular arithmetic operations apart from logical operations [3]. In this paper, we will perform the arithemetic functions like ADD, subtractor, multiplier and logical functions such as AND.

The Arithmetic Logic Unit (ALU) is essentially the heart of a CPU. This allows the computer to add, subtract, multiplier and to perform basic logical operations such as AND, OR etc. Since every computer needs to be able to do these simple functions, they are always included in a CPU. An ALU is a combinational logic circuit that can have one or more inputs and only one output. ALU's output is dependent only on inputs applied at that instant as a function of time, and not on past conditions. A simple ALU in its basic form consists of two inputs for the operands, one input for selecting the desired operation and one output for the result. The complexity of ALU may vary from processor to processor. In [4], a reversible ALU for one binary arithmetic and three logical operations is designed in Base paper. In present work 4 bit ALU with 4 operations is design.

The rest of paper is organized as follows: section II explains the related work. A background of reversible gates and circuits is given in Section III. In Section IV, a brief explanation of ALU and its design with Adder, subtractor, multiplier and logic gates are proposed. Finally Section V describes the performance of ALU and Section VI concludes the paper.

II. Related Work

Reversible Arithmetic logic unit [4] with 4-operation AND, OR, X-OR and ADD. 4-bit adder/subtractor [5], Design of a 4-bit 2's Complement Reversible Circuit [6], Design of Control Unit for Low Power ALU with a Barrel Shifter Using Reversible Logic [7], Design of 32 Bit Reversible ALU [8] with 7-operations and Arithmetic &

Logic Unit (ALU), Design using Reversible Control Unit [9] with 9-operations are related and recent work in the field reversible logic circuits.

III. Fundamental Of Reversible Logic

In Reversible logic circuits have the same number of inputs and outputs, and have one-to-one mapping between vectors of inputs and outputs; thus the vector of input states can be always reconstructed from the vector of output states. This is more advantages than the existing logic levels. Because of this property no information is lost. Each gate can be made reversible by adding some additional input and output wires if necessary [10].Two constraints for reversible logic syntheses are:

(1) Feedback is not allowed,

(2) Fan-out is not allowed (i.e., fan-out = 1).

A gate with k inputs and k outputs is called a k*k gate. Several reversible gates have been proposed over the last decades.

Reversible logic gates Used in Design of circuit in this paper are NOT gate [11], Reversible Gate, Toffoli gate [12],

NOT Gate [11]

It is a simplest Reversible gate and is a 1*1 gate. Not gate is shown in the Figure 1 and its quantum cost is Zero.

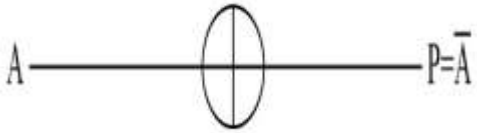

Figure1- NOT Gate

TOFFOLI GATE [12]

2 CNOT gates is 3*3 Reversible gates with three inputs and three outputs. Its quantum cost is 5 and is shown in Figure 2.

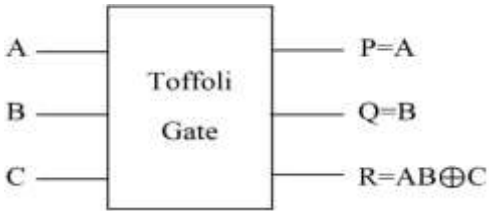

Figure2- Toffoli Gate

REVERSIBLE GATE [R2]

It is a new type of reversible gate and it is 4*4 gates. R2 gate is shown in the Figure.

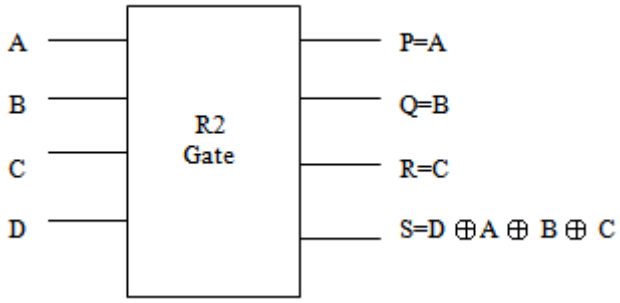

Figure3- Logic for R2 Gate

IV. Proposed Alu Design

The proposed ALU (Arithmetic and Logic Unit) has been designed using adder, subtractor, multiplier and logic gates like AND gate. Thus, the adder is designed with 4bit carry-look ahead adder circuit. Then carry-look ahead adder is designed with some reversible logic gates. They are feynman gate, fredkin gate, TSG gate, PGA gate and reversible gate. By using carry-look ahead adder circuit subtractor is designed. The proposed array multiplier has been designed using toffoli gate and 4-bit carry-look ahead adder circuit. The toffoli gate is used to generate partial product as well as for addition also. Then the 4-bit ALU operations are shown in table1.

S1	S0	OPERATIONS
0	0	Addition
0	1	Subtraction
1	0	Multiplier
1	1	And

Table-1 operations of 4-bit ALU

In this reversible ALU, four operations ADD, SUBTRACT, MULTIPLY, AND are performed depending upon the value of control lines S1 and S0. When S1, S0 = "00" then addition operation is performed, when S1, S0 = "01" then subtraction operation is performed, when S1, S0 = "10" then multiplier operation is performed and when S1, S0="11" then and operation is performed. In the reversible 4 bit ALU, 9 inputs and 9 outputs are used in which we have one constant inputs – Cin, eight inputs- A0,A1,A2,A3,B0,B1,B2,B3 and it have an selected line as an inputs S0 and S1, nine outputs – Y0,Y1,Y2,Y3,Y4,Y5,Y6,Y7,Cout is shown in Figure 4.

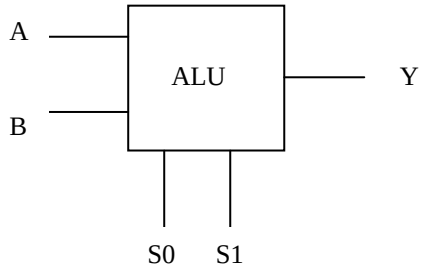

Figure4- Block of ALU

In 4-bit ALU it operates in 4 operations they are adder, subtractor, multiplier and logic operation such as AND gates. It shows in the Figure5.

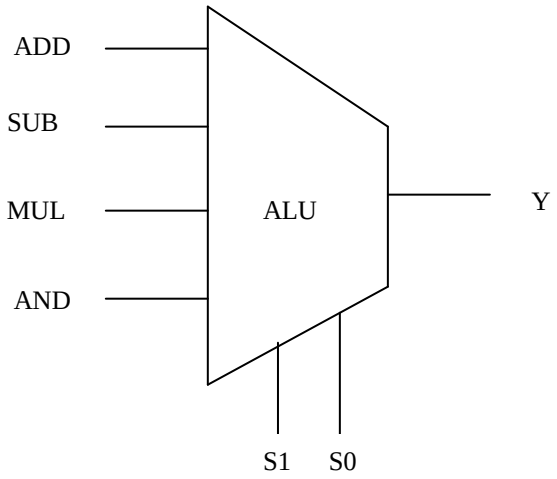

Figure5- Logic Diagram of 4-bit ALU

V. Results And Discussion

The proposed ALU circuit has been designed in verilog coding and implemented in Cadence tool using 180 nm technologies.

Figure6- Simulation Result for 4-bit Adder

This is the simulation result for 4-bit adder. It is a type of carry-look ahead adder.

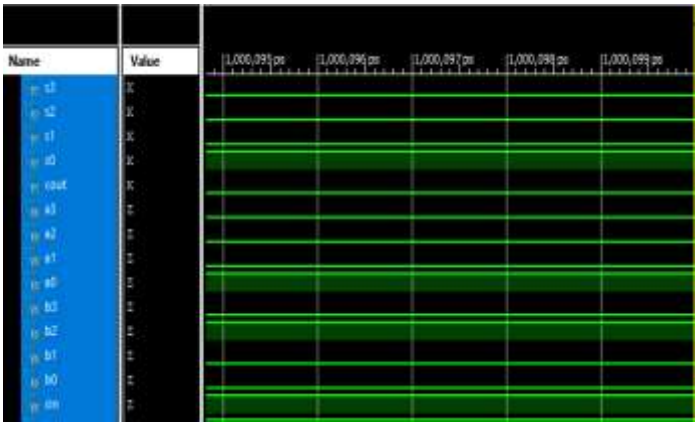

Figure7- Simulation result for Subtractor

This is a simulation results for subtractor. In this result Cin=1.

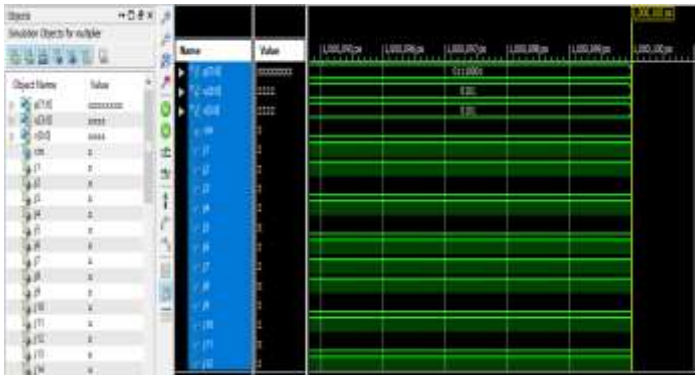

Figure8- Simulation result for Multiplier

This is a simulation result for multiplier. The proposed multiplier consumes less power and it operates on high speed.

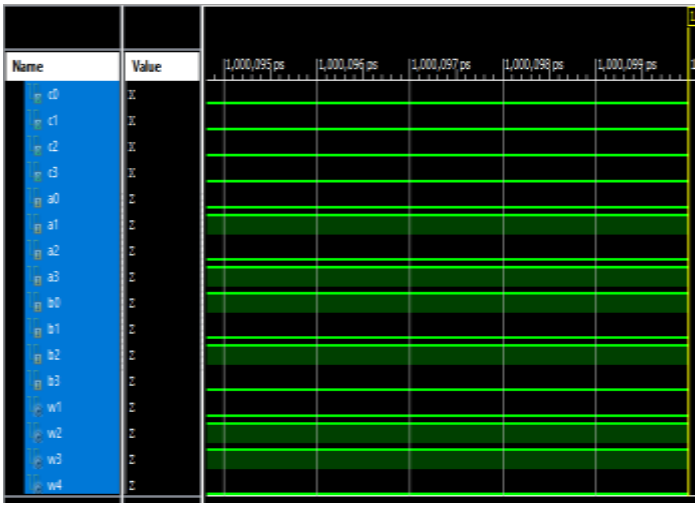

Figure9- Simulation result for AND logic

This is a simulation result for the logical function like (AND).

VI. Conclusions

In this paper, arithmetic and logic unit (ALU) has been designed using 4 operations adder, subtractor, multiplier and logical functions like AND. The proposed ALU has been designed using reversible gates in verilog coding and is implemented in Cadence 180nm technology. It consumes low power and occupies equal area. Hence, the proposed ALU consumes less power it is more suitable for all the DSP applications.

VII. Future Scope

In further by using these 4-operations, to get an simulation result for Arithmetic and Logic Unit (ALU).

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