

Design and Implementation of Modified Viterbi Decoder for a Wi-Fi Receiver

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Abstract: Wireless communication is the transfer of information between two or more points that are not connected by an electrical conductor. The convolutional codes are decoded using the algorithm that found in many universal applications like 802.11 wireless LANs. Viterbi Decoders are employed in digital wireless communication systems to decode the convolution codes which are used for error correction. The most popular communications decoding algorithm, the Viterbi Algorithm (VA), requires an exponential increase in hardware complexity to achieve greater decode accuracy. Convolution codes are deployed in many wireless communication systems to improve the limited capacity for the channels of communication. The Viterbi algorithm is the well employed decoding algorithm for convolutional codes. It is possible to reduce the constraint length using these universal algorithms. The main advantages of using these algorithms are lesser hardware requirements and lesser computations. Modified Viterbi Algorithm (MVA) is a new algorithm which can reduce the computation up to 50% and to reduce the hardware complexity. It shows plan ahead associated with the modified Viterbi decoder implementation using Xilinx tool in verilog language. An implementation is based on Field Programmable Gate Arrays (FPGA) which provides user flexibility to a programmable solutions and lowering the cost.

Keywords: computations reduction, constraint length, hardware reduction, maximum-likelihood path, Modified Viterbi Algorithm, plan ahead, threshold, trellis diagram, Viterbi Algorithm, Wi-Fi receiver

I. Introduction

Convolutional encoding with Viterbi decoding is a good forward error correction technique to reduce the noise. One type of Viterbi decoders called Fangled Viterbi decoders are to decodes quickly and takes less memory with no error detection capability. In this decoding technique it takes a step further by gaining one bit error correction and detection capability at the cost of doubling the computational complexity and the time for processing. A new efficient Viterbi algorithm is proposed here with less hardware complexity and processing time along with 2 bit and 1 bit error correction capabilities. For a 2 bit error correction, when compared with Modified fangled decoder computational complexity decreased by 22-36% [2].

One of the powerful method for the error correction is Convolution encoding. It has been using in many wireless communication systems to improve the limited capacity of the communication channels. The Viterbi algorithm is one of the most extensively employed decoding algorithm for decoding convolution codes. We also proposed One Pointer algorithm for Trace back Implementation of survivor sequence memory management for low power decoder design [3]. Today's data reconstruction in digital communication systems requires designs of highest throughput rate. The Viterbi Algorithm is a key element in such digital signal processing applications [3]. Convolutional codes are widely used in satellite communications. Convolutional encoding is a simple procedure. But decoding of a convolutional code is much more complex task. Many classes of algorithms exist for this purpose. Threshold decoding can be successfully applied only to the specific classes of convolutional codes. It is also far from optimal. Sequential decoding is a class of algorithms performing much better than threshold algorithms. Viterbi decoding is an optimal (in a maximum-likelihood sense) algorithm for decoding of a convolutional code [4]. The rest of this paper is organized as follows. Section II briefly explains the general Viterbi decoder Architecture and its functions. Section III describes the convolutional encoder architecture and its function. In Section IV, introduces the Viterbi algorithm. Section V explains about the Modified Algorithm for a decoder in Wi-Fi receivers, and estimates the computations required, hardware, memory requirement for implementation of Viterbi decoder Section VI describes the results. Finally, the concluding remarks are given in Section VII.

II. Viterbi Decoder

Branch metrics, Add compare select and Survivor management unit are the basic units of viterbi decoder. Figure 1 shows the general structure of a Viterbi decoder. It consist of three blocks: the branch metric unit (BMU), which computes metrics, the add-compare-select unit (ACSU), which selects the survivor paths, also finds the minimum path metric of the survivor paths and the survivor management unit (SMU), that is responsible for selecting the output based on the minimum path metric.

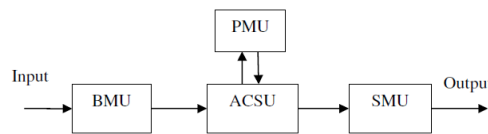


Figure 1: Block Diagram

III. Convolutional Encoder

Convolutional codes are used extensively in numerous applications mainly for data transfer, radio, mobile communication, and satellite communication. For encoding data, start with k memory registers, each holding 1 input bit. The encoder has $n \bmod 2$ adders (a modulo 2 adder can be implemented with a single Boolean XOR gate, where the logic is: $0+0=0$, $0+1=1$, $1+0=1$, $1+1=0$), and n generator polynomials — one for each adder (see figure below). An input bit m_1 moves into the next left register. Generator polynomials and the existing values are used in the remaining registers, the encoder outputs n bits. Then shift all register values to the right (m_1 moves to m_0 , m_0 moves to m_{-1}) and wait for the next input bit. If there are no remaining input bits, the encoder continues output until all registers have returned to the zero state. A convolutional encoder is a finite state machine. An encoder will have 2^n states. Several algorithms exist for decoding convolutional codes. The Viterbi algorithm is universally used as it provides maximum likelihood performance and is highly parallelizable. It is easy to implement Viterbi decoder in VLSI hardware and in software on CPUs with SIMD instruction sets.

Fano algorithm is the best known for longer constraint length codes which are more practically decoded with any of several sequential decoding algorithms. Sequential decoding is not maximum likelihood but its complexity increases only slightly with constraint length in the means of strong, long-constraint-length codes. These codes were used in the Pioneer program of the early 1970s to Jupiter and Saturn, but gave way to shorter, Viterbi-decoded codes, usually concatenated with large Reed-Solomon error correction codes that steepen the overall bit-error-rate curve and produce extremely low residual undetected error rates.

Both Viterbi and sequential decoding algorithms are different. But it return hard decisions. An approximate confidence measure can be added to each bit by use of the Soft output Viterbi algorithm. Maximum a posteriori (MAP) soft decisions for each bit can be obtained by use of the BCJR algorithm.

An popular Viterbi-decoded convolutional code, used at least since the Voyager program has a constraint length k of 7 and a rate r of $1/2$.

- The complexity of the Viterbi algorithm increases exponentially with constraint lengths, even though longer constraint lengths produce more powerful codes. By limiting these more powerful codes to deep space missions where the extra performance is easily worth the increased decoder complexity.

Convolutional Encoder shown in Fig.1 takes input data bit and gives out two bits. Convolutional encoding is a process of adding redundancy to a signal stream. It allows variable code rates ($1/2$), constraint lengths ($K=3, 9$) and generator polynomials. To convolve the encode data; start with 2 memory registers, each holding 1 input bit. Registers start with a value of 0. The encoder has 2 modulo-2 adders which are implemented with a XOR gate. It generates 2 bit polynomials, one for each adder. The convolutional encoder on the whole a finite state machine. The k bit input is move to the constraint length K shift register and the n outputs are calculated from the generator polynomials. The generator polynomial specify the connections of the encoder to the modulo-2 adder. The '1' in the generator polynomial indicates the connections and zero indicates no connections between the stage and modulo -2 adders.

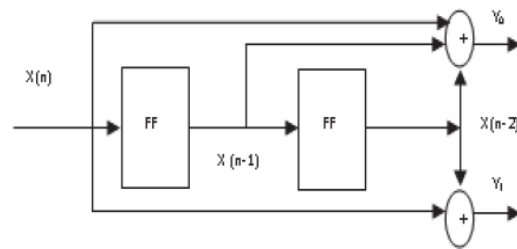


Figure 2: Encoder Diagram

Y_0, Y_1 - Encoder output bits,
 $X(n-1), X(n-2)$ - previous state of Encoder,
 $X(n)$ - input bit to Encoder.

For a rate 1/2 encoder with constraint length of 3, the code can correct up to 2 errors in 16 bits of transmitted data. Here it is assumed that errors do not occur consecutively. The code rate, is expressed as a ratio of the number of bits into the convolutional encoder (k) to the number of channel symbols output by the convolutional encoder (n) in a given encoder cycle. A rate 1/2 encoder is implemented in the design. The constraint length parameter, K , denotes the “length” of the convolution encoder. The parameter m is closely related to, which indicates how many encoder cycles an input bit is retained and used for encoding after it first appears at the input to the convolutional encoder. The following are the specifications of the encoder, $K = 3$, Rate = 1/2.

Encoder functions depending on the applied input, and then the corresponding state transition takes place. The function of encoder understood with the help of the following state diagram. These state diagrams generally implemented with the sequential circuits based on the constraint length used at the transmitter side.

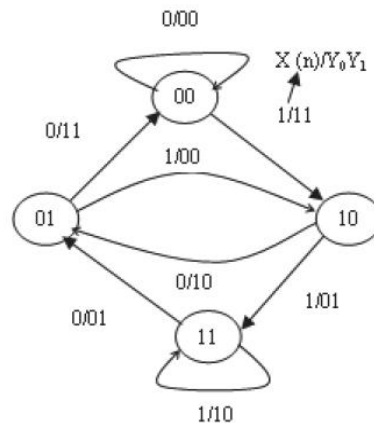


Figure 3: State Diagram

State diagram: This offers a complete description of the system. However, it shows only the instantaneous transitions. It does not illustrate how the states change in time. Trellis diagram: To include time in state transitions.

IV. Viterbi Algorithm

In 1967, Viterbi implemented Viterbi decoding algorithm, decoding process for convolutional codes in memory-less noise. The algorithm can be functional to a host of problems encountered in the design of communication systems. For a given sequence of symbols, the Viterbi Algorithm (VA) finds the most-likelihood path transition sequence in a state diagram. This algorithm consists of the following three major parts:

A. Branch metric calculation

Calculation of a distance between the input pair of bits and the four possible “ideal” pairs (“00”, “01”, “10”, “11”). encoder.

B. Path metric calculation

Calculate a metric for the survivor path ending in this state (a survivor path is a path with the minimum metric) for every encoder state.

C. Trace back

This step is necessary for hardware implementations that don't store full information about the survivor paths, but store only one bit decision every time when one survivor path is selected from the two.

V. Implementation

In the trellis diagram, horizontal direction circles shows the stages, vertical direction circles shows an ideal states and above which circles represents branch metric. Thick lines indicates encoding path for corresponding input data. 'T' indicates time slots for a clock.

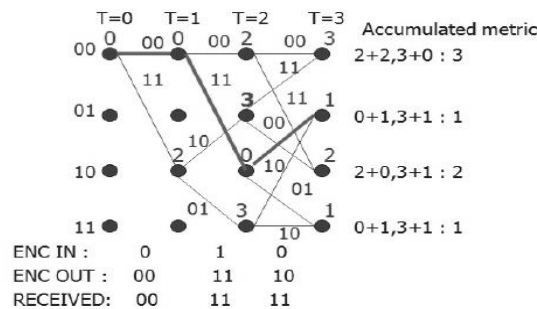


Figure 4: Viterbi Algorithm

Generally used the above trellis structure to decode the original data in the wireless communication receivers. The trellis used at the encoder and decoder same. But the hardware required for the decoding process is more, when constraint length becomes large. The average computation and path storage required by the MVA are reduced. Path retention is based on the following criteria. A threshold 'T' indicates that a path is retained if its path metric is less than $bm + T$, where 'bm' is the minimum cost among all surviving paths in the previous trellis stage. The total number of survivor paths per trellis stage is limited to a fixed number, K, which is pre-set prior to the start of communication. Path metrics are marked in bold on the nodes; dot lines indicate the least error path, upper branch indicates input bit '0', lower branch indicates input bit '1'. Output bits corresponding to the given input bit and state is shown on the branches. In Fig. 5 Shows that constraint length $k=3$. In which the process can be continued with the help of threshold value. In this case fixed the threshold value as one, hence the process determination is not difficult, computations that are no of XOR operations performed at each stage reduced. The computations reduced drastically as constraint length increasing. Generally the coding vectors used depending upon the code rate of encoder and constraint length associated with the input sequence. In the receiver side always consider the same process as transmitter, but in this process of decoding modified structure of decoder used. The following table shows the coding vectors associated with the corresponding constraint length.

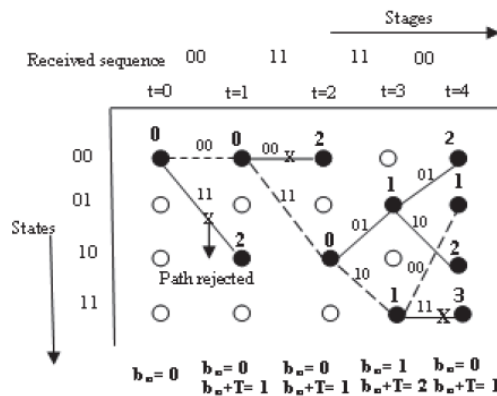


Figure 5: Modified Viterbi Algorithm

VI. Result Analysis

In the evaluation of function of Viterbi decoder can be observed by manually introduce the errors in the received data. Then process the data into all the blocks with modified structure of decoder. Finally decoder decodes the original data by choosing the maximum likely path. Finally compare the original data and decoded data, if both are same decoder output shows the output as low. Because it specifies the errors present in the decoder output. This could be done by using 'XOR' operation between the original data and decoded data. The memory specified by the Decoder depends on the addressing mode. If it is direct addressing mode then memory utilization associated with the decoder hardware less when compared to other addressing modes.

In the Xilinx ISE tool generating the UCF file for place and routing for decoder implementation. This file gives the specified hardware structure for decoder implementation. The simulation gives different types of colours in hexagonal shapes represent different blocks designed in the implementation. Finally simulation represents all combinational blocks mapped on the chip by using logic gates similarly sequential logic can be implemented by flip-flops.

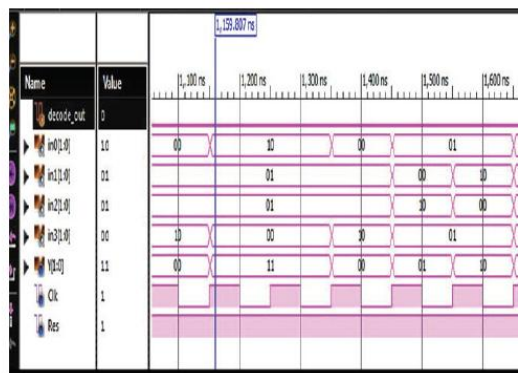


Figure 6: Result

In generally constraint length large case decoding logic does not work properly with general implementation of viterbi algorithm. But large constraint length application also implemented with MVA algorithm.

For constraint length $k=3$ memory utilization approximately 20%. In which the number of look up tables are less in the decoder implementation. The synthesis results in the hardware implementation and time constraints associated with the decoder is shown by using virtex tool.

VII. Conclusion

In this paper, modified Viterbi algorithm has been presented for a Wi-Fi receiver. The function of decoder with MVA determined through Xilinx ISE tool in verilog. This approach has shown computations at each stage reduced, hardware required for overall decoder reduced and plan ahead associated with the decoder by generating the UCF file in Xilinx and MVA decoder implemented by using FPGA technology by using virtex tool. We are currently exploring approaches to perform decoding operation. This allows for graceful degradation of performance under power constraint. The decoder implementation will improve with reference to power and delay constrains when we go for pipelined technique of operation in the decoding scheme.

According to the results, the superiorities of FPGA-based monitoring system over traditional monitoring systems can be summarized as follows;

It has a flexible structure.

It has an economic design.

It is field programmable.

References

- [1]. An efficient viterbi decoder, International journal Of advanced in formational technology vol.2, No.1, February 2012
- [2]. FPGA based design and implementation of modified Viterbi Decoder for a Wi-Fi receiver, proceeding of 2013 IEEE Conference on Information and Communication Technology

- [3]. T. Kalavathidevi and C. Venkatesh, "Area Efficient Low Power VLSI Architecture for A Viterbi Decoder Using Gate Diffusion Input(GDI) Logic Style", *European Journal of Scientific Research*, Vol. 49, no.4, pp. 521-532, March 2011
- [4]. Y. Shiau, P. Chen, H. Yang, Y. Lin and S. Huang, "An Efficient VLSI architecture for convolution code Decoding", *International Symposium Next Generation Electronics*, pp. 223-226, 2010.
- [5]. T. K. Trung, M. T. Shih, I. S Reed, and E. H. Satorius, "A VLSI design for a trace back viterbi decoder," *IEEE Trans. on Communications*, vol. 40, no.3, March 2009.
- [6]. S. Shaker, S. Elramly, and K. Shehata, "design and implementation of low-power viterbi decoder for software-defined WiMAX receiver," *International Conference on Microelectronics*, pp. 264 – 267, 2009.
- [7]. B. Pandita and S. K. Roy, "A Parallel Viterbi Decoder For Block Cyclic and Convolution Codes," *Department of Electronics and Computer Science University of Southampton*, April 2008.
- [8]. C. Arun and P. Rajamani, "Design and VLSI Implementation of a low probability of error viterbi decoder," *First international conference on Emerging trends in Engineering and technology*, pp. 418-423, 2008.
- [9]. B. Sklar, *Digital Communications - Fundamentals and Applications*, Prentice Hall, New Jersey, 2001.