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The Novel design method of 3 to 8 decoder

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Abstract:*One of the most sophisticated single electron devices (SED), single electron transistor (SET) is expected to be quite promising for future VLSI design due to its Nano scale feature size, ultra-low power dissipation and unique characteristics of Coulomb blockade oscillation. Circuits with SETs are also able to achieve a lot of new functionalities with less number of devices through novel design methodologies. However, pure SET based circuits have very limited applications due to SET's low current drivability, small voltage gain and extremely low temperature operation. Since CMOS devices have advantages that can compensate for the intrinsic drawbacks of SET, hybrid CMOS-SET architecture which combines the merits of both CMOS and SET devices promises to be a much practical implementation for nanometer scale circuit design.*
Keywords: *Single Electron Transistor (SET), Coulomb blockade oscillation, hybrid CMOS-SET*

I. Introduction:

The performance of many applications such as digital signal processing depends on the performance of the arithmetic circuits to execute complex algorithms. Usually, the performance of the integrated circuits is influenced by how the arithmetic operators are implemented in the cell library provided to the designer and used for synthesizing. As more complex arithmetic circuits are presented each day, the power consumption becomes more important.

The arithmetic circuits grows more complex with the increasing processor bus width, so energy consumption is becoming more important now than ever due to the increase in the number and density of transistors on a chip and faster clock increasing demand for fast growing technologies in mobile electronic devices such as cellular phones, laptop computers requires the use of a single electron transistor decoder in Nano Technology systems. Decreasing the power supply leads to power consumption reduction. However, lowering supply voltage also increases circuit delay and degrades drive ability of cells designed with certain logic styles. One way of consuming less power is that a circuit operates at extremely low frequency, but it may take a very long time to complete which is in contrast with high speed operation demands.

Single electron transistor (SET) is a new type of switching device that uses controlled electron tunneling to amplify current. SET is distinguished by a very small device size and ultra-low power dissipation and based on controlling the transport of an individual electron. In 1987, Likharev has proposed a single electron transistor in which the tunneling of the electrons is controlled by a bias applied at the center electrode [1]. Since then, various solutions have been developed on logic circuits, memory and other circuits. The first single electron inverter, made from two complementary SETs was proposed by Tucker et al. in 1992 [2]. This work explains the design of 3 to 8 decoder SET-CMOS design style.

II. Single Electron Transistor (SET):

Single Electron Transistor are three-terminal devices. The two junctions create a Coulomb island or Quantum dot that electrons can only enter by tunneling through one of the tunnel junctions. The gate terminal is capacitively coupled to the node between the two tunnel junctions. The capacitor may seem like a third tunnel junction, but it is much thicker than the others so that no electrons can tunnel through it. The capacitor simply serves as a way of setting the electric charge on the coulomb island. The SET can transfer electrons from source to drain one by one and therefore can be used as a switching device. Electrons have to tunnel through the junction from the source to the drain via the central island for normal operation of the SET. For tunneling, the charging energy E_c, should be greater than the thermal energy and also the tunneling resistance $R_T > h/e^2$. Therefore the phenomenon of SET is expressed as $Ec = e^2 / 2C_\Sigma >> K_BT$ and $R_T >> h/e^2$ where C_Σ is the total island capacitance with respect to the ground, K_B is the Boltzmann's constant, T is the temperature and h is the Planck's constant. The SETs may also have an optional 2nd gate connected to the island that can be used for controlling the phase shift of coulomb oscillation.

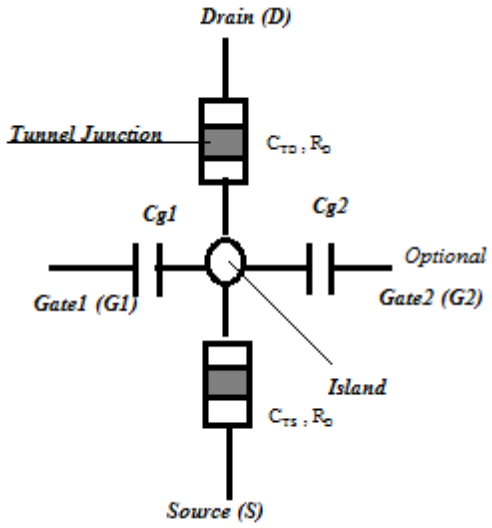

Fig 1 Schematic structure of the SET

The figure (1) shows the schematic structure of an SET, where C_{TD} is the drain tunnel junction, C_{TS} is the source tunnel junction capacitance, R_D is the drain tunnel junction resistance, R_S is the source tunnel junction resistance, $C_{G1}$is the gate capacitance and C_{G2} is the optional 2nd gate capacitance. The MIB model is physically based compact analytical model for SET[3]. The model based on the assumptions that it obeys the orthodox theory of single electron tunneling and the interconnect capacitances associated with the source, drain and gate are much larger than the device capacitances so that the total capacitance of the island with respect to ground will be equal to the summation of all device capacitances i.e. $C_\Sigma = C_{TD} + C_{TS} + C_{G1} + C_{G2}$. The drain current in the MIB model for analog application is expressed as [3].

Considering only $0 \leftrightarrow 1$, transitions, the MIB model for digital application is expressed as [1]

$$I_D = \frac{\lambda \{ I_{TS}(0) I_{TD}(1) - I_{TS}(1) I_{TD}(0) \}}{(I_{TS}(1) + I_{TD}(1)) + (I_{TS}(0) + I_{TD}(0))}$$

$$I_{TS}(n) = \frac{-\lambda V_{island} + (2n-1)\alpha}{\left[1 - \exp\left(-\frac{-\lambda V_{island} + (2n-1)\alpha}{V_T}\right)\right] R_{TS}}$$

$$I_{TD}(n) = \frac{-\lambda V_{DS} + \lambda V_{island} - (2n+1)\alpha}{\left[1 - \exp\left(-\frac{-\lambda V_{DS} + \lambda V_{island} - (2n+1)\alpha}{V_T}\right)\right] R_{TD}}$$

Where n is the number of electron in the island $\alpha = e/2C_\Sigma$ and λ holds the sign of V_{DS}

The decoder uses all AND gates, and therefore, the outputs are active-high. For active low outputs, NAND gates are used. It has 3 input lines and 8 output lines. It is also called binary to octal decoder. It takes a 3 bit binary input code and activates one of the 8(octal) outputs corresponding to that code.

The circuit of a hybrid SET-CMOS Inverter proposed which is formed by a PMOS transistor as the load resistance of an SET. Although it resembles a CMOS inverter, there are two difference in the pull down transistor is a SET and the VDD is defined by the SET device parameters. Throughout the work, MIB analytical model is used for SETs and all simulations are conducted using SPICE simulation at room temperature.

Since the MIB model is valid for $|VDD| \leq 3e / C\varepsilon$ [9] for single / multiple gate (s) and symmetric (or) asymmetric SET devices, the bias Voltage is taken as 800mv. The values of the tunnel junction capacitors are C_{TD} and C_{TS} have be designed to prevent tunneling due to thermal energy. Based on the idea that serial connection is AND and Parallel connection is OR, the circuit of 3 input XOR is realized using the hybrid CMOS-SET inverter. The circuits of inverter and 3 input XOR are shown in Fig 2(a), 2(b). Using the structure of CMOS counterparts, the Circuit of 3 to 8 decoder is designed and implemented using the hybrid logic gates are shown in fig 3. The simulation results are shown in fig.4.

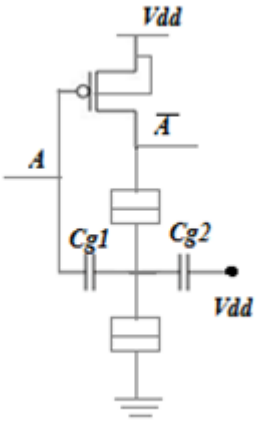

Fig 2 (a) shows the SET-CMOS Inverter Circuit

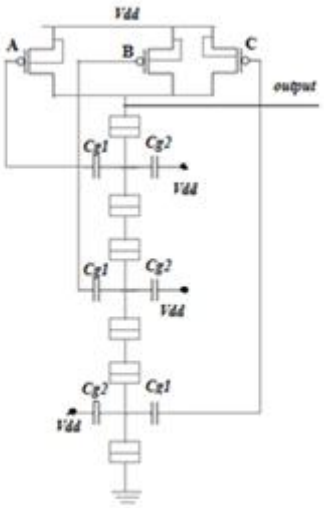

Fig 2(b) shows the circuit of 3 input NAND gate

The island, gate and tunnel capacitors of SET designed for room temperature operation and the supply voltage V_{dd} is taken to 0.8V [4,5]. Design parameters of the SET transistor are $C_{TD} = C_{TS} = 0.15aF$, $C_{g1} = C_{g2} = 0.2aF$ and $R_{TD} = R_{TS} = 1M\Omega$.The BSIM4.6.1 predictive model is examined the behavior of CMOS transistor through SPICE simulations. Design parameters of CMOS transistor are W/L = 64/54nm, $V_{th} = -0.3V$ for PMOS and $V_{th} = 0.47V$ for NMOS.

III. Conclusion:

Modern era that demands superiority in consumer electronics can be achieved only if a clear and concise representation of digital functions can be obtained using SET logical synthesis which is obviously advantages in power consumption technique and also be adopted and if the size can be absolutely reduced for easy portability. In this Scenario, SET is a fascinating technology, which explores new physical effects of charge transport. The logical operations create greater scope in future SET based logic circuits. Thus this novel approach is intended to acquire attraction in future applications.

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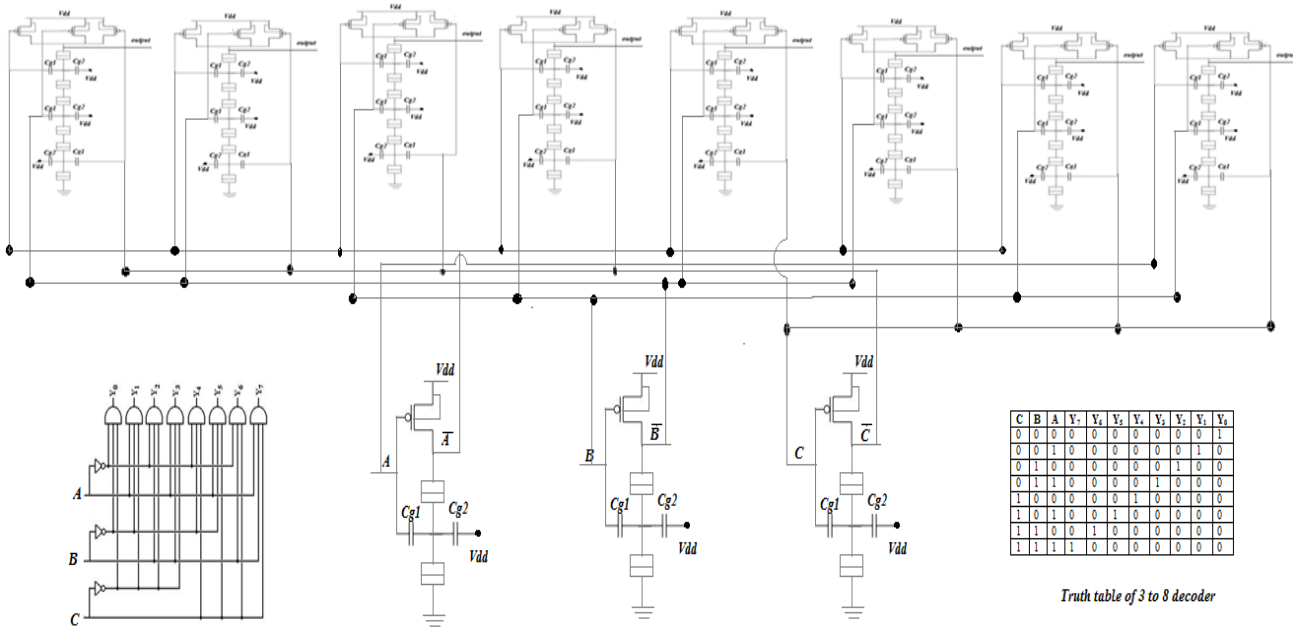

Logic circuit of 3 to 8 decoder

Fig. (3) shows the SET-CMOS circuit of 3 to 8 decoder

C	B	A	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

Truth table of 3 to 8 decoder

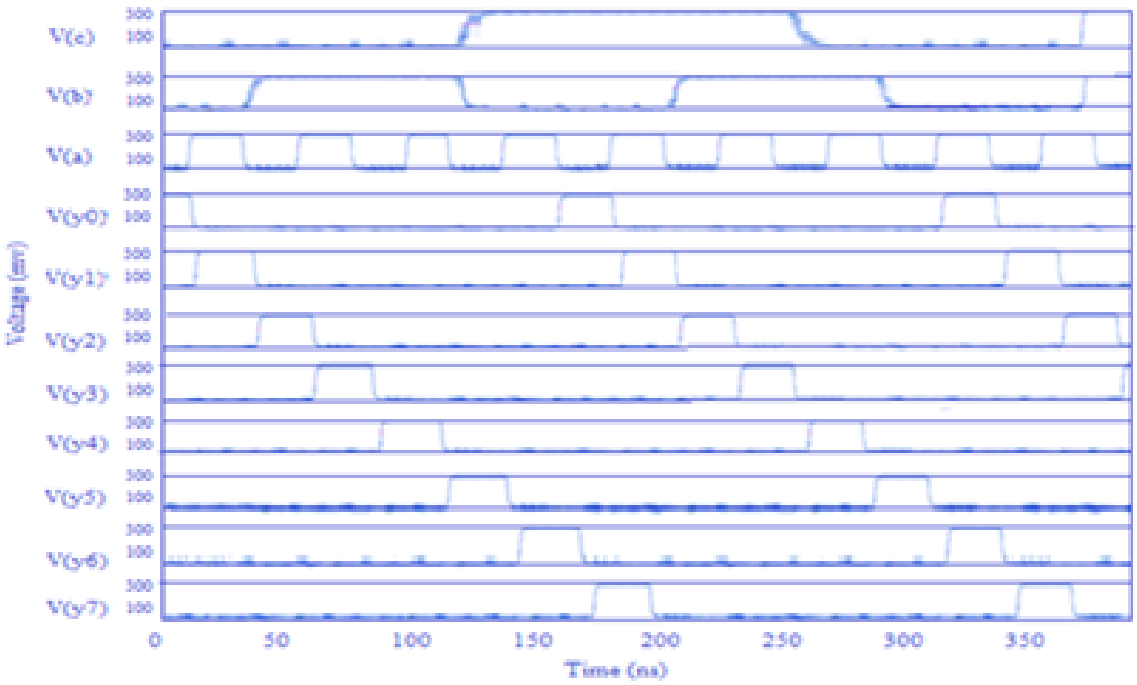

Fig. 4 shows the Simulation output for SET-CMOS 3 to 8 decoder : a,b,c are inputs and y0,y1,y2,y3,y4,y5,y6,y7 are outputs